# LOGIC
# DATABOOK

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NATIONAL
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# LOGIC DATABOOK

This is the *Logic* databook from National Semiconductor Corporation. It contains complete information on the extensive National bipolar logic families. The series of logic families presented in this book are TTL (54/74), Schottky (54S/74S), low power Schottky (54LS/74LS), high speed (54H/74H) and low power (54L/74L).

National is also introducing the advanced Schottky (54AS/74AS) and low power Schottky families (54ALS/74ALS). Data sheets will be available as products become available during 1981. Contact your National representative for more detail on these next generation logic families.

Product selection guides and a complete product applications section are also included. For information on products that become available after this databook goes to print, contact your local National office.


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**National Semiconductor Corporation** 2900 Semiconductor Drive, Santa Clara, California 95051 Tel: (408) 737-5000 TWX: (910) 339-9240



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**Note:** When there are two set of page numbers, the first designates the connection diagram page; the second indicates electrical tables.

All flat packages are W-type unless otherwise noted as F-types. All cavity DIPs are J-types. All molded DIPs are N-types.

| Device Type | | Package/Temperature Combinations | | | Availability | |
|---|---|---|---|---|---|---|
| | | Flat Pack W-Type MIL | Cavity DIP J-Type MIL | Molded DIP N-Type COML | In Production | Future Product |
| **Series 54/74** | | | | | | |
| DM5400/DM7400 | Quad 2-Input NAND Gate | ● | ● | ● | ● | |
| DM5401/DM7401 | Quad 2-Input NAND Gate (Open Collector) | ● | ● | ● | ● | |
| DM5402/DM7402 | Quad 2-Input NOR Gate | ● | ● | ● | ● | |
| DM5403/DM7403 | Quad 2-Input NAND Gate (Open Collector) | | ● | ● | ● | |
| DM5404/DM7404 | Hex Inverter | ● | ● | ● | ● | |
| DM5405/DM7405 | Hex Inverter (Open Collector) | ● | ● | ● | ● | |
| DM5406/DM7406 | 30 mA 30 V Hex Inverting Buffer (Open Collector) | ● | ● | ● | ● | |
| DM5407/DM7407 | 30 mA 30 V Hex Buffer (Open Collector) | ● | ● | ● | ● | |
| DM5408/DM7408 | Quad 2-Input AND Gate | ● | ● | ● | ● | |
| DM5409/DM7409 | Quad 2-Input AND Gate (Open Collector) | ● | ● | ● | ● | |
| DM5410/DM7410 | Triple 3-Input NAND Gate | ● | ● | ● | ● | |
| DM5411/DM7411 | Triple 3-Input AND Gate | | ● | ● | ● | |
| DM5413/DM7413 | Dual Schmitt Trigger | ● | ● | ● | ● | |
| DM5414/DM7414 | Hex Schmitt Trigger | | ● | ● | ● | |
| DM5416/DM7416 | 30 mA 15 V Hex Inverting Buffer (Open Collector) | ● | ● | ● | ● | |
| DM5417/DM7417 | 30 mA 15 V Hex Buffer (Open Collector) | ● | ● | ● | ● | |
| DM5420/DM7420 | Dual 4-Input NAND Gate | ● | ● | ● | ● | |
| DM5423/DM7423 | Exp. Dual-4 NOR Gate | ● | ● | ● | ● | |
| DM5425/DM7425 | Dual-4-Input NOR Gate | ● | ● | ● | ● | |
| DM5426/DM7426 | Quad 2-Input NAND Gate (15 V, O.C.) | | ● | ● | ● | |
| DM5427/DM7427 | Triple-3-Input NOR Gate | | ● | ● | ● | |
| DM5430/DM7430 | 8-Input NAND Gate | ● | ● | ● | ● | |
| DM5432/DM7432 | Quad 2-Input OR Gate | ● | ● | ● | ● | |
| DM5437/DM7437 | Quad-2-Input NAND Buffer | ● | ● | ● | ● | |
| DM5438/DM7438 | Quad-2-Input NAND Buffer (Open Collector) | ● | ● | ● | ● | |
| DM5440/DM7440 | Dual 4-Input NAND Buffer | ● | ● | ● | ● | |
| DM5441A/DM7441A | NIXIE Driver | ● | ● | ● | ● | |
| DM5442/DM7442 | BCD-to-Decimal Decoder | ● | ● | ● | ● | |
| DM5445/DM7445 | BCD-to-Decimal Decoder/Driver (30 V, 80 mA) | ● | ● | ● | ● | |
| DM5446A/DM7446A | BCD-to-7 Segment Decoder/Driver (40 mA, 30 V) | ● | ● | ● | ● | |
| DM5447A/DM7447A | BCD-to-7 Segment Decoder/Driver (40 mA, 15 V) | ● | ● | ● | ● | |
| DM5448/DM7448 | BCD-to-7 Segment Decoder/Driver (Active High) | ● | ● | ● | ● | |
| DM5450/DM7450 | Expandable Dual 2-Input AND-OR-INVERT Gate | ● | ● | ● | ● | |
| DM5451/DM7451 | Dual 2-Input AND-OR-INVERT Gate | ● | ● | ● | ● | |
| DM5453/DM7453 | Expandable 2-Input AND-OR-INVERT Gate | ● | ● | ● | ● | |
| DM5454/DM7454 | 2-Input AND-OR-INVERT Gate | ● | ● | ● | ● | |
| DM5460/DM7460 | Dual 4-Input Expander | ● | ● | ● | ● | |
| DM5470/DM7470 | Gated Edge-Triggered JK Flip-Flop | ● | ● | ● | ● | |
| DM5472/DM7472 | Gated JK M/S Flip-Flop | ● | ● | ● | ● | |
| DM5473/DM7473 | Dual JK M/S Flip-Flop (Clear) | ● | ● | ● | ● | |
| DM5474/DM7474 | Dual D-Type Flip-Flop (Preset and Clear) | ● | ● | ● | ● | |
| DM5475/DM7475 | Quad Latch | ● | ● | ● | ● | |
| DM5476/DM7476 | Dual JK M/S Flip-Flop (Preset and Clear) | ● | ● | ● | ● | |
| DM5483/DM7483 | 4-Bit Binary Full Adder | ● | ● | ● | ● | |
| DM5485/DM7485 | 4-Bit Comparator | ● | ● | ● | ● | |
| DM5486/DM7486 | Quad 2-Input Exclusive-OR Gate | ● | ● | ● | ● | |
| DM5490A/DM7490A | Decade Counter | ● | ● | ● | ● | |
| DM5492A/DM7492A | Binary Counter | ● | ● | ● | ● | |
| DM5493A/DM7493A | 4-Bit Binary Counter | ● | ● | ● | ● | |
| DM5495/DM7495 | 4-Bit Parallel Access Shift Register | ● | ● | ● | ● | |
| DM5496/DM7496 | 5-Bit Parallel-In, Parallel-Out Shift Register | ● | ● | ● | ● | |
| DM54107/DM74107 | Dual JK Flip-Flop (Clear) | | ● | ● | ● | |
| DM54109/DM74109 | Dual JK Flip-Flop (FSC 9024) (Preset and Clear) | ● | ● | ● | ● | |
| DM54121/DM74121 | Monostable Multivibrator | ● | ● | ● | ● | |
| DM54123/DM74123 | Dual Monostable Multivibrator | ● | ● | ● | ● | |
| DM54125/DM74125 | TRI-STATE* Quad 2-Input Buffer (DM8093) | ● | ● | ● | ● | |
| DM54126/DM74126 | TRI-STATE Quad 2-Input Buffer (DM8094) | ● | ● | ● | ● | |
| DM54132/DM74132 | Quad Schmitt Trigger | ● | ● | ● | ● | |
| DM54141/DM74141 | NIXIE Driver | ● | ● | ● | ● | |
| DM54145/DM74145 | BCD-to-Decimal Decoder/Driver (15 V, 80 mA) | ● | ● | ● | ● | |
| DM54147/DM74147 | Priority Encoder | ● | ● | ● | ● | |
| DM54148/DM74148 | Priority Encoder (FSC9318) | ● | ● | ● | ● | |
| DM54150/DM74150 | 16:1 Multiplexer | F | ● | ● | ● | |
| DM54151A/DM74151A | Data Selector/Multiplexer | ● | ● | ● | ● | |
| DM54153/DM74153 | Dual 4:1 Multiplexer | ● | ● | ● | ● | |
| DM54154/DM74154 | 4:16 Decoder/Demultiplexer (FSC9311) | F | ● | ● | ● | |
| DM54155/DM74155 | Dual 2:4 Demultiplexer | ● | ● | ● | ● | |
| DM54156/DM74156 | Dual 2:4 Demultiplexer (Open Collector) | ● | ● | ● | ● | |
| DM54157/DM74157 | Quad 2-Input Multiplexer (FSC 9322) | ● | ● | ● | ● | |
| DM54160A/DM74160A | Presettable Decade Counter (FSC 9310) | ● | ● | ● | ● | |
| DM54161A/DM74161A | Presettable Binary Counter (FSC 9316) | ● | ● | ● | ● | |
| DM54162A/DM74162A | Presettable Decade Counter (Sync. Clear) | ● | ● | ● | ● | |
| DM54163A/DM74163A | Presettable Binary Counter (Sync. Clear) | ● | ● | ● | ● | |
| DM54164/DM74164 | 8-Bit Serial-In, Parallel-Out Shift Reg. (DM8570) | ● | ● | ● | ● | |
| DM54165/DM74165 | 8-Bit Parallel-In, Serial-Out Shift Reg. (DM8590) | ● | ● | ● | ● | |
| DM54166/DM74166 | 8-Bit Parallel-In, Serial-Out Shift Register | | ● | ● | ● | |
| DM54170/DM74170 | 4 x 4 Register File | | ● | ● | ● | |
| DM54173/DM74173 | TRI-STATE* Quad D Register (DM8551) | ● | ● | ● | ● | |
| DM54174/DM74174 | Hex D Flip-Flop | ● | ● | ● | ● | |
| DM54175/DM74175 | Quad D Flip-Flop | ● | ● | ● | ● | |
| DM54176/DM74176 | Presettable Decade Counter (SIG8280) | | ● | ● | ● | |
| DM54177/DM74177 | Presettable Binary Counter (SIG8281) | | ● | ● | ● | |
| DM54180/DM74180 | Parity Generator/Checker | ● | ● | ● | ● | |

# Logic Package/Temperature Selection Guide

| Device Type | | Package/Temperature Combinations | | | Availability | |
|---|---|---|---|---|---|---|
| | | Flat Pack W-Type MIL | Cavity DIP J-Type MIL | Molded DIP N-Type COML | In Production | Future Product |
| **Series 54/74 (Cont'd)** | | | | | | |
| DM54181/DM74181 | Arithmetic Logic Unit | | ● | ● | ● | |
| DM54184/DM74184 | BCD-to-Binary Converter | ● | ● | ● | ● | |
| DM54185A/DM74185A | Binary-to-BCD Converter | ● | ● | ● | ● | |
| DM54190/DM74190 | Sync Up/Down Decade Counter (Mode Control) | ● | ● | ● | ● | |
| DM54191/DM74191 | Sync Up/Down Binary Counter (Mode Control) | ● | ● | ● | ● | |
| DM54192/DM74192 | Sync Up/Down Decade Ctr. (DM8560) | ● | ● | ● | ● | |
| DM54193/DM74193 | Sync Up/Down Binary Ctr. (DM8563) | ● | ● | ● | ● | |
| DM54194/DM74194 | 4-Bit Bi-Directional Shift Register | ● | ● | ● | ● | |
| DM54195/DM74195 | 4-Bit Parallel Shift Register | ● | ● | ● | ● | |
| DM54196/DM74196 | Presettable Decade Counter (SIG 8290) | | ● | ● | ● | |
| DM54197/DM74197 | Presettable Binary Counter (SIG 8291) | | ● | ● | ● | |
| DM54198/DM74198 | 8-Bit Parallel-In, Parallel-Out Shift Register | | ● | ● | ● | |
| DM54199/DM74199 | 8-Bit Parallel-In, Parallel-Out Shift Register | | ● | ● | ● | |
| DM54251/DM74251 | TRI-STATE® 8-Channel Multiplexer (DM8121) | ● | ● | ● | ● | |
| DM54259/DM74259 | 8-Bit Addressable Latch (DM9334) | ● | ● | ● | ● | |
| DM54365/DM74365 | TRI-STATE Hex Buffer (DM8095) | ● | ● | ● | ● | |
| DM54366/DM74366 | TRI-STATE Hex Inverting Buffer (DM8096) | ● | ● | ● | ● | |
| DM54367/DM74367 | TRI-STATE Hex Buffer (4-2) (DM8097) | ● | ● | ● | ● | |
| DM54368/DM74368 | TRI-STATE Hex Inverting Buffer (4-2) (DM8098) | ● | ● | ● | ● | |
| DM7092/DM8092 | Dual 5-Input NAND Gate | ● | ● | ● | ● | |
| DM7093/DM8093 | TRI-STATE Quad 2-Input Buffer (DM74125) | ● | ● | ● | ● | |
| DM7094/DM8094 | TRI-STATE Quad 2-Input Buffer (DM74126) | ● | ● | ● | ● | |
| DM7095/DM8095 | TRI-STATE Hex Buffer (DM74365) | ● | ● | ● | ● | |
| DM7096/DM8096 | TRI-STATE Hex Inverting Buffer (DM74366) | ● | ● | ● | ● | |
| DM7097/DM8097 | TRI-STATE Hex Buffer (4-2) (DM74367) | ● | ● | ● | ● | |
| DM7098/DM8098 | TRI-STATE Hex Inverting Buffer (4-2) (DM74365) | ● | ● | ● | ● | |
| DM7121/DM8121 | TRI-STATE DM74151 (DM74251) | ● | ● | ● | ● | |
| DM7123/DM8123 | TRI-STATE 9322 | ● | ● | ● | ● | |
| DM7130/DM8130 | 10-Bit Comparator | F | ● | ● | ● | |
| DM7131/DM8131 | 6-Bit Comparator with Hi-Z Inputs | ● | ● | ● | ● | |
| DM7136/DM8136 | 6-Bit Comparator with Hi-Z Inputs (Open Collector) | ● | ● | ● | ● | |
| DM7160/DM8160 | 6-Bit Comparator | ● | ● | ● | ● | |
| DM7200/DM8200 | 4-Bit Digital Comparator | ● | ● | ● | ● | |
| DM7214/DM8214 | TRI-STATE DM74153 | ● | ● | ● | ● | |
| DM7219/DM8219 | TRI-STATE DM74150 | F | ● | ● | ● | |
| DM7220/DM8220 | Parity Generator/Checker | ● | ● | ● | ● | |
| DM7223/DM8223 | 1:8 Demultiplexer | | ● | ● | ● | |
| DM7511/DM8511 | Dual Gated D Flip-Flop | ● | ● | ● | ● | |
| DM7512/DM8512 | Dual Gated Flip-Flop | ● | ● | ● | ● | |
| DM7520/DM8520 | Modulo-N-Divider | ● | ● | ● | ● | |
| DM7542/DM8542 | TRI-STATE Quad I-O Register | ● | ● | ● | ● | |
| DM7544/DM8544 | Contact Bounce Eliminator | ● | ● | ● | ● | |
| DM7546/DM8546 | TRI-STATE 8-Bit Universal Shift Register | ● | ● | ● | ● | |
| DM7551/DM8551 | TRI-STATE Quad D Register (DM74173) | ● | ● | ● | ● | |
| DM7552/DM8552 | TRI-STATE Decade Counter/Latch | ● | ● | ● | ● | |
| DM7553/DM8553 | TRI-STATE 8-Bit Latch | ● | ● | ● | ● | |
| DM7554/DM8554 | TRI-STATE Binary Counter/Latch | ● | ● | ● | ● | |
| DM7555/DM8555 | TRI-STATE Presettable Decade Counter | ● | ● | ● | ● | |
| DM7556/DM8556 | TRI-STATE Presettable Binary Counter | ● | ● | ● | ● | |
| DM7560/DM8560 | Up/Down Decade Counter (DM74192) | ● | ● | ● | ● | |
| DM7563/DM8563 | Up/Down Binary Counter (DM74193) | ● | ● | ● | ● | |
| DM7570/DM8570 | 8-Bit Serial-In, Parallel-Out Shift Reg. (DM74164) | ● | ● | ● | ● | |
| DM7590/DM8590 | 8-Bit Parallel-In, Serial-Out Shift Reg. (DM74165) | ● | ● | ● | ● | |
| DM7613/DM8613 | Quad Gated D Flip-Flop | ● | ● | ● | ● | |
| DM7853/DM8853 | Dual Monostable Multivibrator (Double-Edge) | ● | ● | ● | ● | |
| DM7875A/DM8875A | TRI-STATE 4-Bit Multiplier | | ● | ● | ● | |
| DM7875B/DM8875B | TRI-STATE 4-Bit Multiplier | | ● | ● | ● | |
| DM8898 | TRI-STATE DM74184 | N/A | N/A | ● | ● | |
| DM8899 | TRI-STATE DM74185A | N/A | N/A | ● | ● | |
| **Fairchild TTL** | | | | | | |
| DM9002C | Quad 2-Input NAND Gate | N/A | N/A | ● | ● | |
| DM9003C | Triple 3-Input NAND Gate | N/A | N/A | ● | ● | |
| DM9004C | Dual 4-Input NAND Gate | N/A | N/A | ● | ● | |
| DM9012C | Quad 2-Input NAND Gate (Open Collector) | N/A | N/A | ● | ● | |
| DM9016C | Hex Inverter | N/A | N/A | ● | ● | |
| DM9024/DM8024 | Dual JK Flip-Flop (DM74109) | ● | ● | ● | ● | |
| DM9300/DM8300 | 4-Bit Parallel Shift Register | ● | ● | ● | ● | |
| DM9301/DM8301 | 1-of-10 Decoder | ● | ● | ● | ● | |
| DM9309/DM8309 | Dual 4-Input Multiplexer | ● | ● | ● | ● | |
| DM9310/DM8310 | Synchronous 4-Bit Decade Counter (DM74160A) | ● | ● | ● | ● | |
| DM9311/DM8311 | 4:16 Decoder/Demultiplexer (DM74154) | ● | ● | ● | ● | |
| DM9312/DM8312 | 8-Input Multiplexer | ● | ● | ● | ● | |
| DM9316/DM8316 | Synchronous 4-Bit Binary Counter (DM74161A) | ● | ● | ● | ● | |
| DM9318/DM8318 | Priority Encoder (DM74148) | ● | ● | ● | ● | |
| DM9322/DM8322 | Quad 2-Input Multiplexer (DM74157) | ● | ● | ● | ● | |
| DM9334/DM8334 | 8-Bit Addressable Latch (DM74259) | ● | ● | ● | ● | |
| DM9601/DM8601 | Monostable Multivibrator | ● | ● | ● | ● | |
| DM9602/DM8602 | Dual Monostable Multivibrator (with Reset) | ● | ● | ● | ● | |
| **AMD TTL** | | | | | | |
| DM2502/DM2502C | Successive Approximation Register | ● | ● | ● | ● | |
| DM2503/DM2503C | Successive Approximation Register | ● | ● | ● | ● | |
| DM2504/DM2504C | Successive Approximation Register | F | ● | ● | ● | |

# Logic Package/Temperature Selection Guide

| Device Type | | Package/Temperature Combinations | | | Availability | |
|---|---|---|---|---|---|---|
| | | Flat Pack W-Type MIL | Cavity DIP J-Type MIL | Molded DIP N-Type COML | In Production | Future Product |
| **Series 54LS/74LS** | | | | | | |
| DM54LS00/DM74LS00 | Quad 2-Input NAND Gate | | ● | ● | ● | |
| DM54LS01/DM74LS01 | Quad 2-Input NAND Gate (Open Collector) | | ● | ● | ● | |
| DM54LS02/DM74LS02 | Quad 2-Input NOR Gate | | ● | ● | ● | |
| DM54LS03/DM74LS03 | Quad 2-Input NAND Gate (Open Collector) | | ● | ● | ● | |
| DM54LS04/DM74LS04 | Hex Inverter | | ● | ● | ● | |
| DM54LS05/DM74LS05 | Hex Inverter (Open Collector) | | ● | ● | ● | |
| DM54LS08/DM74LS08 | Quad 2-Input AND Gate | | ● | ● | ● | |
| DM54LS09/DM74LS09 | Quad 2-Input AND Gate (Open Collector) | | ● | ● | ● | |
| DM54LS10/DM74LS10 | Triple 3-Input NAND Gate | | ● | | ● | |
| DM54LS11/DM74LS11 | Triple 3-Input AND Gate | | ● | ● | ● | |
| DM54LS12/DM74LS12 | Triple 3-Input NAND Gate (Open Collector) | | ● | ● | ● | |
| DM54LS13/DM74LS13 | Dual 4-Input NAND Schmitt Trigger | | ● | ● | ● | |
| DM54LS14/DM74LS14 | Hex Schmitt Trigger | | ● | ● | ● | |
| DM54LS15/DM74LS15 | Triple 3-Input AND Gate (Open Collector) | | ● | ● | ● | |
| DM54LS20/DM74LS20 | Dual 4-Input NAND Gate | | ● | | ● | |
| DM54LS21/DM74LS21 | Dual 4-Input AND Gate | | ● | ● | ● | |
| DM54LS22/DM74LS22 | Dual 4-Input NAND Gate (Open Collector) | | ● | ● | ● | |
| DM54LS26/DM74LS26 | Quad 2-Input High Voltage NAND Gate | | ● | ● | ● | |
| DM54LS27/DM74LS27 | Triple-3 NOR Gate | | ● | ● | ● | |
| DM54LS30/DM74LS30 | 8-Input NAND Gate | | ● | ● | ● | |
| DM54LS32/DM74LS32 | Quad 2-Input OR Gate | | ● | ● | ● | |
| DM54LS37/DM74LS37 | Quad 2-Input NAND Buffer | | ● | ● | ● | |
| DM54LS38/DM74LS38 | Quad 2-Input NAND Buffer (Open Collector) | | ● | ● | ● | |
| DM54LS40/DM74LS40 | Dual 4-Input NAND Buffer | | ● | | ● | |
| DM54LS42/DM74LS42 | BCD-to-Decimal Decoder | | ● | ● | ● | |
| DM54LS47/DM74LS47 | BCD/7-Segment Decoder/Driver | | ● | ● | ● | |
| DM54LS48/DM74LS48 | BCD/7-Segment Decoder/Driver | | ● | ● | ● | |
| DM54LS49/DM74LS49 | BCD/7-Segment Decoder/Driver | | ● | | ● | |
| DM54LS51/DM74LS51 | Dual 2-Input AND-OR-INVERT Gate | | ● | ● | ● | |
| DM54LS54/DM74LS54 | 2-Input AND-OR-INVERT Gate | | ● | | ● | |
| DM54LS55/DM74LS55 | Dual 4-Input AOI Gate | | ● | ● | ● | |
| DM54LS73A/DM74LS73A | Dual JK M/S Flip-Flop (Clear) | | ● | ● | ● | |
| DM54LS74A/DM74LS74A | Dual D-Type Flip-Flop (Preset and Clear) | | ● | ● | ● | |
| DM54LS75/DM74LS75 | Quad Latch | | ● | ● | ● | |
| DM54LS76A/DM74LS76A | Dual JK M/S Flip-Flop (Preset and Clear) | | ● | ● | ● | |
| DM54LS77/DM74LS77 | Quad Latch, No $\overline{Q}$ Output | | ● | | | |
| DM54LS78A/DM74LS78A | Dual JK Flip-Flop (Pre., Comm. Clk., Comm. Clr.) | | ● | | | |
| DM54LS83A/DM74LS83A | 4-Bit Binary Fll Adder | | ● | ● | ● | |
| DM54LS85/DM74LS85 | 4-Bit Magnitude Comparator | | ● | ● | ● | |
| DM54LS86/DM74LS86 | Quad 2-Input Exclusive-OR Gate | | ● | ● | ● | |
| DM54LS90/DM74LS90 | Decade Counter | | ● | ● | ● | |
| DM54LS92/DM74LS92 | Divide-by-12 Counter | | ● | | | |
| DM54LS93/DM74LS93 | 4-Bit Binary Counter | | ● | ● | ● | |
| DM54LS107A/DM74LS107A | Dual JK Flip-Flop | | ● | ● | ● | |
| DM54LS109A/DM74LS109A | Dual JK Flip-Flop | | ● | ● | ● | |
| DM54LS112A/DM74LS112A | Dual JK Flip-Flop (Preset and Clear) | | ● | ● | ● | |
| DM54LS113A/DM74LS113A | Dual JK Flip-Flop (Preset) | | ● | ● | ● | |
| DM54LS114A/DM74LS114A | Dual JK Flip-Flop (Pre., Comm. Clk., Comm. Clr.) | | ● | ● | ● | |
| DM54LS122/DM74LS122 | Retriggerable One Shot (Clear) | | | | ● | |
| DM54LS123/DM74LS123 | Dual Monostable Multivibrator | | | | ● | |
| DM54LS125/DM74LS125 | TRI-STATE® Quad Buffer | | | | ● | |
| DM54LS126/DM74LS126 | TRI-STATE Quad Buffer | | ● | ● | ● | |
| DM54LS132/DM74LS132 | Quad 2-Input NAND Schmitt Trigger | | ● | ● | ● | |
| DM54LS136/DM74LS136 | Quad Exclusive-OR Gate (Open Collector) | | ● | ● | ● | |
| DM54LS138/DM74LS138 | Expandable 3/8 Decoder | | ● | ● | ● | |
| DM54LS139/DM74LS139 | Expandable Dual 2/4 Decoder | | ● | ● | ● | |
| DM54LS151/DM74LS151 | 8-Channel Multiplexer | | ● | ● | ● | |
| DM54LS153/DM74LS153 | Dual 4:1 Multiplexer | | ● | ● | ● | |
| DM54LS154/DM74LS154 | 4:16 Decoder/Demultiplexer | F | ● | ● | ● | |
| DM54LS155/DM74LS155 | Dual 2-Line to 4-Line Decoder/Demultiplexer | | ● | ● | ● | |
| DM54LS156/DM74LS156 | Dual 2-Line to 4-Line Decoder/Demultiplexer | | ● | ● | ● | |
| DM54LS157/DM74LS157 | Quad 2-Input Multiplexer | | ● | ● | ● | |
| DM54LS158/DM74LS158 | Quad 2-Input Multiplexer | | ● | ● | ● | |
| DM54LS160A/DM74LS160A | Presettable Decade Counter | | ● | ● | ● | |
| DM54LS161A/DM74LS161A | Presettable Binary Counter | | ● | ● | ● | |
| DM54LS162A/DM74LS162A | Presettable Decade Counter (Sync. Clear) | | ● | ● | ● | |
| DM54LS163A/DM74LS163A | Presettable Binary Counter (Sync. Clear) | | ● | ● | ● | |
| DM54LS164/DM74LS164 | 8-Bit Serial-In, Parallel-Out Shift Register | | ● | ● | ● | |
| DM54LS165/DM74LS165 | 8-Bit PISO Shift Register | | | | | |
| DM54LS166/DM74LS166 | 8 Bit SIPO | | | | | ● |
| DM54LS168A/DM74LS168A | Sync. Up/Down Decade Counter | | ● | ● | ● | ● |
| DM54LS169A/DM74LS169A | Sync. Up/Down Binary Counter | | ● | ● | ● | |
| DM54LS170/DM74LS170 | 4 By 4 Register File | | ● | ● | ● | |
| DM54LS173/DM74LS173 | TRI-STATE Quad D Register | | ● | ● | ● | |
| DM54LS174/DM74LS174 | Hex D Flip-Flop | | ● | ● | ● | |
| DM54LS175/DM74LS175 | Quad D Flip-Flop | | ● | ● | ● | |
| DM54LS190/DM74LS190 | Sync. Up/Dn Decade Cntr (Mode Control) | | ● | ● | ● | |
| DM54LS191/DM74LS191 | Sync. Up/Dn Binary Cntr (Mode Control) | | ● | ● | ● | |
| DM54LS192/DM74LS192 | Sync. Up/Down Decade Counter (2 Clocks) | | ● | ● | ● | |
| DM54LS193/DM74LS193 | Sync. Up/Down Binary Counter (2 Clocks) | | ● | ● | ● | |
| DM54LS194A/DM74LS194A | 4-Bit Bi-Direct Shift Register | | | | | |
| DM54LS195A/DM74LS195A | 4-Bit Parallel Access Shift Register | | | | | ● |
| DM54LS196/DM74LS196 | Presettable Decade Counter | | ● | ● | ● | ● |

| Device Type | | Package/Temperature Combinations | | | Availability | |
|---|---|---|---|---|---|---|
| | | Flat Pack W-Type MIL | Cavity DIP J-Type MIL | Molded DIP N-Type COML | In Production | Future Product |
| **Series 54LS/74LS (Cont'd)** | | | | | | |
| DM54LS197/DM74LS197 | Presettable Binary Counter | • | • | • | • | |
| DM54LS221/DM74LS221 | Dual One Shot with Schmitt Trigger Inputs | | | • | • | |
| DM54LS240/DM74LS240 | TRI-STATE® Octal Line Driver | • | • | • | • | |
| DM54LS241/DM74LS241 | TRI-STATE Octal Line Driver | • | • | • | • | |
| DM54LS242/DM74LS242 | Quadruple Bus Transceiver | • | • | • | • | |
| DM54LS243/DM74LS243 | Quadruple Bus Transceiver | • | • | • | • | |
| DM54LS244/DM74LS244 | TRI-STATE Octal Line Driver | • | • | • | • | |
| DM54LS245/DM74LS245 | TRI-STATE Octal Transcender | • | • | • | • | |
| DM54LS247/DM74LS247 | BCD-7 Segment Decoder/Driver (O.C.) | • | • | • | • | |
| DM54LS248/DM74LS248 | BCD-7 Segment Decoder/Driver | • | • | • | • | |
| DM54LS249/DM74LS249 | BCD-7-Segment Decoder/Driver (O.C.) | • | • | • | • | |
| DM54LS251/DM74LS251 | TRI-STATE LS151 Multiplexer | | | | | • |
| DM54LS253/DM74LS253 | TRI-STATE DM74LS153 | • | • | • | • | |
| DM54LS257B/DM74LS257B | TRI-STATE DM74LS157 | • | • | • | • | |
| DM54LS258B/DM74LS258B | TRI-STATE DM74LS158 | • | • | • | • | |
| DM54LS259/DM74LS259 | Addressable Latch | • | • | • | • | |
| DM54LS266/DM74LS266 | Quad Exclusive NOR Gate (O.C.) | • | • | • | • | |
| DM54LS279/DM74LS279 | Quad S-R Latch | • | • | • | • | |
| DM54LS283/DM74LS283 | 4-Bit Binary Adder with Fast Carry | • | • | • | • | |
| DM54LS290/DM74LS290 | DM74LS90 with Corner Power Pins | • | • | • | • | |
| DM54LS293/DM74LS293 | DM74LS93 with Corner Power Pins | • | • | • | • | |
| DM54LS298/DM74LS298 | Quad 2-Input Mux W/Storage | | | | | • |
| DM54LS352/DM74LS352 | Inverting Version of DM74LS153 | • | • | • | • | |
| DM54LS353/DM74LS353 | Inverting Version of DM74LS253 | • | • | • | • | |
| DM54LS365/DM74LS365 | TRI-STATE Hex Buffer | • | • | • | • | |
| DM54LS366/DM74LS366 | TRI-STATE Hex Buffer | • | • | • | • | |
| DM54LS367/DM74LS367 | TRI-STATE Hex Buffer | • | • | • | • | |
| DM54LS368/DM74LS368 | TRI-STATE Hex Buffer | • | • | • | • | |
| DM54LS373/DM74LS373 | TRI-STATE Octal Latch | • | • | • | • | |
| DM54LS374/DM74LS374 | TRI-STATE Octal D Flip-Flop | | | | • | |
| DM54LS386/DM74LS386 | Quad Exclusive OR Gate | • | • | • | • | |
| DM54LS390/DM74LS390 | Dual 4-Bit Binary Counter | | | | | |
| DM54LS393/DM74LS393 | Dual 4-Bit Decade Counter | | | | | |
| DM54LS670/DM74LS670 | TRI-STATE 4 By 4 Register File | • | • | • | • | |
| DM71LS95/DM81LS95 | TRI-STATE Octal Buffer | | | • | • | |
| DM71LS96/DM81LS96 | TRI-STATE Octal Buffer | | | • | • | |
| DM71LS97/DM81LS97 | TRI-STATE Octal Buffer | | | • | • | |
| DM71LS98/DM81LS98 | TRI-STATE Octal Buffer | | | • | • | |
| DM54LS952/DM74LS952 | 8-Bit Universal I/O Register | • | • | • | • | |
| DM54LS962/MD74LS962 | 8-Bit Universal I/O Register | • | • | • | • | |
| **Series 54L/74L** | | | | | | |
| DM54L00/DM74L00 | Quad 2-Input NAND Gate | • | • | • | • | |
| DM54L01/DM74L01 | Quad 2-Input NAND Gate (Open Collector) | • | | | • | |
| DM54L02/DM74L02 | Quad 2-Input NOR Gate | • | • | • | • | |
| DM54L03/DM74L03 | Quad 2-Input NAND Gate (Open Collector) | | • | • | • | |
| DM54L04/DM74L04 | Hex Inverter | • | • | • | • | |
| DM54L05/DM74L05 | Hex Inverter (Open Collector) | • | • | • | • | |
| DM54L08/DM74L08 | Quad 2-Input AND Gate | • | • | • | • | |
| DM54L09/DM4L09 | Quad 2-Input AND Gate (Open Collector) | • | • | • | • | |
| DM54L10/DM74L10 | Triple 3-Input NAND Gate | • | • | • | • | |
| DM54L11/DM74L11 | Triple 3-Input AND Gate | • | • | • | • | |
| DM54L20/DM74L20 | Dual 4-Input NAND Gate | • | • | • | • | |
| DM54L26/DM74L26 | Quad 2-Input NAND Gate (O.C., 15 V) | | • | • | • | |
| DM54L30/DM74L30 | 8-Input NAND Gate | • | • | • | • | |
| DM54L32/DM74L32 | Quad 2-Input OR Gate | • | • | • | • | |
| DM54L42A/DM74L42A | BCD-to-Decimal Decoder (1/10 power) | • | • | • | • | |
| DM54L51/DM74L51 | Dual-AND-OR-INVERT Gate | • | • | • | • | |
| DM54L54/DM74L54 | 2-2-3-3 Input AND-OR-INVERT Gate | • | • | • | • | |
| DM54L55/DM74L55 | 4-Input AND-OR-INVERT Gate | • | • | • | • | |
| DM54L71/DM74L71 | R-S M/S Flip-Flop | • | • | • | • | |
| DM54L72/DM74L72 | JK M/S Flip-Flop | • | • | • | • | |
| DM54L73/DM74L73 | Dual JK M/S Flip-Flop (Clear) | • | • | • | • | |
| DM54L74/DM74L74 | Dual-D Flip-Flop (Preset and Clear) | • | • | • | • | |
| DM54L75A/DM74L75A | Quad Latch (1/10 power) | • | • | • | • | |
| DM54L78/DM74L78 | Dual JK Flip-Flop (Pie., Comm. Clk. Comm. Clr) | • | • | • | • | |
| DM54L85/DM74L85 | 4-Bit Comparator | • | • | • | • | |
| DM54L86/DM74L86 | Quad Exclusive OR Gate | • | • | • | • | |
| DM54L90/DM74L90 | Decade Counter | • | • | • | • | |
| DM54L91/DM74L91 | 8-Bit Serial Shift Register | • | • | • | • | |
| DM54L93/DM74L93 | Binary Counter | • | • | • | • | |
| DM54L95/DM74L95 | 4-Bit Parallel Shift Register | • | • | • | • | |
| DM54L98/DM74L98 | 4-Bit Storage Register | • | • | • | • | |
| DM54L123A/DM74L123A | Dual Mono, Multivibrator (1/10 power) | • | • | • | • | |
| DM54L154A/DM74L154A | 4:16 Decoder (1/10 power) | F | • | • | • | |
| DM54L157A/DM74L157A | Quad 2 Mux. (93L22 Pinout, 1/10 power) | • | • | • | • | |
| DM54L164A/DM74L164A | 8-Bit Ser. In. Par. Out Shift Reg. (1/10 power) | • | • | • | • | |
| DM54L165A/DM74L165A | 8-Bit Par. In. Ser. Out Shift Reg. (1/10 power) | • | • | • | • | |
| DM54L192/DM74L192 | Sync. 4-Bit Up-Down Ctr. (DM85L60) | • | • | • | • | |
| DM54L193/DM74L193 | Sync. 4-Bit Up-Down Ctr. (DM85L63) | • | • | • | • | |
| DM80L06 | Quad 2-Input NAND Gate (Passive Pull-Up) | N/A | N/A | • | • | |
| DM70L95/DM80L95 | TRI-STATE Hex Buffer | • | • | • | • | |
| DM70L96/DM80L96 | TRI-STATE Hex Inverter | • | • | • | • | |

# Logic Package/Temperature Selection Guide

| Device Type | | Package/Temperature Combinations | | | Availability | |
|---|---|---|---|---|---|---|
| | | Flat Pack W-Type MIL | Cavity DIP J-Type MIL | Molded DIP N-Type COML | In Production | Future Product |
| **Series 54L/74L (Cont'd)** | | | | | | |
| DM70L97/DM80L97 | TRI-STATE® Hex Buffer (4-2) | ● | ● | ● | ● | |
| DM70L98/DM80L98 | TRI-STATE Hex Inverter (4-2) | ● | ● | ● | ● | |
| DM71L22/DM81L22 | Quad 2-Input Multiplexer (DM74L157A) | ● | ● | ● | ● | |
| DM71L23/DM81L23 | TRI-STATE 93L22 (1/10 power) | ● | ● | ● | ● | |
| DM75L11/DM85L11 | Dual Gated JK Flip-Flop | ● | ● | ● | ● | |
| DM75L12/DM85L12 | Dual Gated JK Flip-Flop | ● | ● | ● | ● | |
| DM75L51/DM85L51 | TRI-STATE® Quad D Register | ● | ● | ● | ● | |
| DM75L52/DM85L52 | TRI-STATE Decade Ctr/Latch | ● | ● | ● | ● | |
| DM75L54/DM85L54 | TRI-STATE Binary Ctr/Latch | ● | ● | ● | ● | |
| DM75L60/DM85L60 | Up/Down Decade Counter (DM74L192) | ● | ● | ● | ● | |
| DM75L63/DM85L63 | Up/Down Binary Counter (DM74L193) | ● | ● | ● | ● | |
| DM76L13/DM86L13 | Quad Gated D Flip-Flop | ● | ● | ● | ● | |
| DM76L24/DM86L24 | 4-Bit Magnitude Comparator | ● | ● | ● | ● | |
| DM76L25/DM86L25 | 7-Segment-to-BCD Converter | ● | ● | ● | ● | |
| DM76L70F/DM86L70F | DM54L164A with Clr. Pwr. Pins (F.P. Only) | ● | ● | ● | ● | |
| DM76L75/DM86L75 | Presettable Decade Counter (93L10 Pinout) | ● | | | ● | |
| DM76L76/DM86L76 | Presettable Binary Counter (93L16 Pinout) | ● | ● | ● | ● | |
| DM76L90/DM86L90 | 8-Bit Par. In, Ser. Out Shift Reg. (DM74L165A) | ● | ● | ● | ● | |
| DM76L93/DM86L93 | Binary Counter (DM7493 Pin-Out) | ● | ● | ● | ● | |
| **Series 54H/74H** | | | | | | |
| DM54H00/DM74H00 | Quad 2-Input NAND Gate | | | | | |
| DM54H01/DM74H01 | Quad 2-Input NAND Gate (Open Collector) | N/A | ● | ● | ● | |
| DM54H04/DM74H04 | Hex Inverter | N/A | ● | ● | ● | |
| DM54H08/DM74H08 | Quad 2-Input AND Gate | N/A | ● | ● | ● | |
| DM54H10/DM74H10 | Triple 3-Input NAND Gate | N/A | ● | ● | ● | |
| DM54H11/DM74H11 | Triple 3-Input AND Gate | N/A | ● | ● | ● | |
| DM54H20/DM74H20 | Dual 4-Input NAND Gate | N/A | ● | ● | ● | |
| DM54H21/DM74H21 | Dual 4-Input AND Gate | N/A | ● | ● | ● | |
| DM54H30/DM74H30 | 8-Input NAND Buffer | N/A | ● | ● | ● | |
| DM54H40/DM74H40 | Dual 4-Input NAND Buffer | N/A | ● | ● | ● | |
| DM54H50/DM74H50 | Expandable Dual 2-Input AND-OR-INVERT Gate | N/A | ● | ● | ● | |
| DM54H62/DM74H62 | 3-2-2-3 Input Expander | N/A | ● | ● | ● | |
| DM54H74/DM74H74 | Dual D Flip-Flop (Preset and Clear) | N/A | ● | ● | ● | |
| DM54H103/DM74H103 | Dual JK Flip-Flop (Clear) | N/A | ● | ● | ● | |
| DM54H106/DM74H106 | Dual JK Flip-Flop (Preset and Clear) | N/A | ● | ● | ● | |
| DM54H108/DM74H108 | Dual JK Flip-Flop (Common Clock) | N/A | ● | ● | ● | |
| **Series 54S/74S** | | | | | | |
| DM54S00/DM74S00 | Quad 2-Input NAND Gate | ● | ● | ● | ● | |
| DM54S02/DM74S02 | Quad 2-Input NOR Gate | ● | ● | ● | ● | |
| DM54S03/DM74S03 | Quad 2-Input NAND Gate (Open Collector) | ● | ● | ● | ● | |
| DM54S04/DM74S04 | Hex Inverter | ● | ● | ● | ● | |
| DM54S05/DM74S05 | Hex Inverter (Open Collector) | ● | ● | ● | ● | |
| DM54S08/DM74S08 | Quad 2-Input AND Gates (Open Collector) | ● | ● | ● | ● | |
| DM54S09/DM74S09 | Quad 2-Input AND Gates (Open Collector) | ● | ● | ● | ● | |
| DM54S10/DM74S10 | Triple 3-Input NAND Gate | ● | ● | ● | ● | |
| DM54S11/DM74S11 | Triple 3-Input AND Gate | ● | ● | ● | ● | |
| DM54S15/DM74S15 | Triple 3-Input AND Gate (Open Collector) | ● | ● | ● | ● | |
| DM54S20/DM74S20 | Dual 4-Input NAND Gate | ● | ● | ● | ● | |
| DM54S22/DM74S22 | Dual 4-Input NAND Gate (Open Collector) | ● | ● | ● | ● | |
| DM54S30/DM74S30 | 8-Input NAND Gate | ● | ● | ● | ● | |
| DM54S40/DM74S40 | Dual 4-Input NAND Buffer | ● | ● | ● | ● | |
| DM54S51/DM74S51 | Dual 2-Input AOI Gate | ● | ● | ● | ● | |
| DM54S64/DM74S64 | 4-2-2-3 AND-OR-INVERT Gate | ● | ● | ● | ● | |
| DM54S65/DM74S65 | AND-OR-INVERT Gate (Open Collector) | ● | ● | ● | ● | |
| DM54S74/DM74S74 | Dual D Flip-Flop (Preset and Clear) | ● | ● | ● | ● | |
| DM54S86/DM74S86 | Quad Exclusive-OR Gate | ● | ● | ● | ● | |
| DM54S112/DM74S112 | Dual JK Flip-Flop (Preset and Clear) | ● | ● | ● | ● | |
| DM54S113/DM74S113 | Dual JK Flip-Flop (Preset) | ● | ● | ● | ● | |
| DM54S114/DM74S114 | Dual JK Flip-Flop (Preset, Comm. Clock, Comm. Clear) | ● | ● | ● | ● | |
| DM54S133/DM74S133 | 13-Input NAND Gate | ● | ● | ● | ● | |
| DM54S134/DM74S134 | TRI-STATE 12-Input NAND Gate | ● | ● | ● | ● | |
| DM54S135/DM74S135 | Quad Exclusive-OR/NOR Gate | ● | ● | ● | ● | |
| DM54S136/DM74S136 | Quad Exclusive-OR Gate (Open Collector) | ● | ● | ● | ● | |
| DM54S138/DM74S138 | Expandable 3/8 Decoder | ● | ● | ● | ● | |
| DM54S139/DM74S139 | Expandable 2/4 Decoder | ● | ● | ● | ● | |
| DM54S140/DM74S140 | Dual 4-Input NAND Driver | ● | ● | ● | ● | |
| DM54S151/DM74S151 | 8-Input Multiplexer | ● | ● | ● | ● | |
| DM54S153/DM74S153 | Dual 4-Multiplexer | ● | ● | ● | ● | |
| DM54S157DM74S157 | Quad 2-Input Multiplexer | ● | ● | ● | ● | |
| DM54S158/DM74S158 | Quad 2-Input Multiplexer (Inverted Outputs) | ● | ● | ● | ● | |
| DM54S160/DM74S160 | Presettable Decade Counter | ● | ● | ● | ● | |
| DM54S161/DM74S161 | Presettable Binary Counter | ● | ● | ● | ● | |
| DM54S162/DM74S162 | Presettable Decade Counter Sync Clear | ● | ● | ● | ● | |
| DM54S163/DM74S163 | Presettable Binary Counter Sync Clear | ● | ● | ● | ● | |
| DM54S174/DM74S174 | Hex D Flip-Flop | ● | ● | ● | ● | |
| DM54S175/DM74S175 | Quad D Flip-Flop | ● | ● | ● | ● | |
| DM54S181/DM74S181 | Arithmetic Logic Unit | ● | ● | ● | ● | |
| DM54S182/DM74S182 | Carry/Look Ahead for ALU | ● | ● | ● | ● | |
| DM54S194/DM74S194 | 4-Bit Bidirectional Shift Register | ● | ● | ● | ● | |
| DM74S195/DM74S195 | 4-Bit Parallel Shift Register | ● | ● | ● | ● | |
| DM54S196/DM74S196 | Presettable Decade Counter | ● | ● | ● | ● | |
| DM54S197/DM74S197 | Presettable Binary Counter | ● | ● | ● | ● | |
| DM54S240/DM74S240 | TRI-STATE Octal Line Driver | ● | ● | ● | ● | |

| Device Type | | Package/Temperature Combinations | | | Availability | |
|---|---|---|---|---|---|---|
| | | Flat Pack W-Type MIL | Cavity DIP J-Type MIL | Molded DIP N-Type COML | In Production | Future Product |
| **Series 74S (Cont'd)** | | | | | | |
| DM54S241/DM74S241 | TRI-STATE® Octal Line Driver | • | • | • | • | |
| DM54S242/DM74S242 | Quad Bus Transceiver | • | • | • | • | |
| DM54S243/DM74S243 | Quad Bus Transceiver | • | • | • | • | |
| DM54S244/DM74S244 | TRI-STATE Octal Line Driver | • | • | • | • | |
| DM54S251/DM74S251 | TRI-STATE DM74S151 | • | • | • | • | |
| DM54S253/DM74S253 | TRI-STATE DM74S153 | • | • | • | • | |
| DM54S257/DM74S257 | TRI-STATE DM74S157 | • | • | • | • | |
| DM54S258/DM74S258 | TRI-STATE DM74S158 | • | • | • | • | |
| DM54S280/DM74S280 | 9-Bit Parity Generator | N/A | N/A | • | • | |
| DM54S283/DM74S283 | Full Adder W/ Fast Carry | • | • | • | • | |
| DM54S299/DM74S299 | 8-Bit Universal Shift Register | • | • | • | • | |
| DM54S373/DM74S373 | TRI-STATE Octal Latch | • | • | • | • | |
| DM54S374/DM74S374 | TRI-STATE Octal Latch | • | • | • | • | |
| DM54S381/DM74S381 | Arithmetic Logic Unit | • | • | • | • | |
| DM54S940/DM74S940 | TRI-STATE Octal Line Driver | • | • | • | • | |
| DM54S941/DM74S941 | TRI-STATE Octal Line Driver | • | • | • | • | |

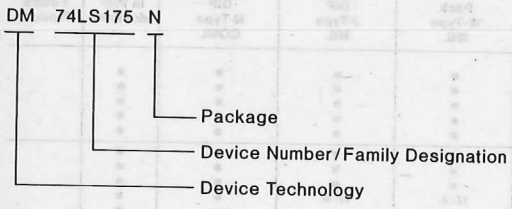
**Note:** When low power device type has "A" on end, indicates T.I. device *not* one-tenth power.

**Note:** All products available with A+/B+ processing.

**Note:** An additional part types should be put into chart in *alphanumeric sequence*.

**Note:** All N pkg. also available in "J" pkg.

Ordering information for National Devices covered in this catalogue is as follows




## Device Technology

- *DM*—Digital Monolithic

## Device Number

- 4 to 8 digit number
- 1st two digits denote temperature selection
  54—denotes full mil range specification −55°C to +125°C
  74—denotes commercial specification 0°C to 70°C

## Family Designation

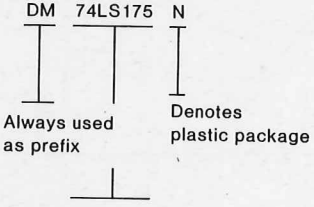
- 54/74XX(X)—TTL
- 54/74LSXX(X)—Low Power Schottky
- 54/74SXX(X)—Schottky
- 54/74LXX(X)—Low Power
- 54/74HXX(X)—High Speed
- Additional Device Designations—72/82XX, 73/83XX, 75/85XX, 76/86XX, 71LS/81LSXX

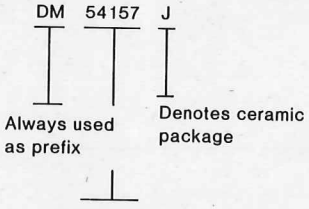
National Semiconductor manufactures a complete line of industry standard logic products. The industry standard number identifying a particular function is used in marking the product with the only difference being prefixes and suffixes noted above.

When ordering a particular product, please specify the entire number, including the *DM prefix* and appropriate *package* suffix. This will help in processing your order more quickly.

Note: Although the *part* number is generally uniform throughout the industry, competitors vary in terms of denoting package type and temperature selection. Please refer to the industry cross reference guide in the back of this data book for properly cross referencing competitor products.

Example: How to order



# Section 1
# SSI Functional Index/ Selection Guide

1

The following pages contain functional indexes and selection guides designed to simplify the choice of a particular function to fit a specific application. Essential characteristics of similar or like functions are grouped for comparative analysis, and the electrical specifications are referenced by page number. The following categories of functions are covered:


| DESCRIPTION | PAGE NUMBER |
|---|---|
| **SSI Functions** | |
| AND Gates with Totem-Pole Outputs | 1-2 |
| AND Gates with Open-Collector Outputs | 1-2 |
| AND-OR-INVERT Gates with Totem-Pole Outputs | 1-2 |
| AND-OR-INVERT Gates with Open-Collector Outputs | 1-2 |
| Buffers/Clock Drivers with Totem-Pole Outputs | 1-2 |
| Buffer and Interface Gates with Open-Collector Outputs | 1-3 |
| Bus Interface Gates with TRI-STATE® Totem-Pole Outputs | 1-3 |
| Expandable Gates | 1-3 |
| Expanders | 1-3 |
| Flip-Flops, Gated | 1-4 |
| Flip-Flops, Single and Dual J-K Edge-Triggered | 1-4 |
| Flip-Flops, Dual D-Type | 1-5 |
| Flip-Flops, Single and Dual Pulse-Triggered | 1-5 |
| Latches, $\overline{S}$-$\overline{R}$ | 1-6 |
| Line Drivers, 50-Ohm/75-Ohm | 1-6 |
| NAND Gates and Inverters with Open-Collector Outputs | 1-6 |
| Gates, Buffers, Drivers and Bus Transceivers with TRI-STATE Outputs | 1-7 |
| NAND Gates and Inverters with Totem-Pole Outputs | 1-7 |
| NOR, OR Gates with Open-Collector Outputs | 1-8 |
| NOR Gates with Totem-Pole Outputs | 1-8 |
| One Shots, Retriggerable | 1-8 |
| One Shots with Schmitt-Trigger Inputs | 1-8 |
| OR Gates with Totem-Pole Outputs | 1-8 |
| Schmitt-Triggers with Totem-Pole Outputs | 1-8 |

## AND Gates With Totem-Pole Outputs

| Description | Typ. Propagation Delay Time | Typ. Power Dissipation Per Gate | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|
| | | | Mil. | | Coml. | | | |
| Dual 4-Input AND Gates | 7.8 ns | 4.25 mW | 54LS21 | J,W | 74LS21 | N | 3-8 | 5-12 |
| | 8.2 ns | 40 mW | 54H21 | J | 74H21 | N | 3-8 | 5-12 |
| Triple 3-Input AND Gates | 4.75 ns | 31 mW | 54S11 | J,W | 74S11 | N | 3-6 | 5-12 |
| | 7.8 ns | 4.25 mW | 54LS11 | J,W | 74LS11 | N | 3-6 | 5-12 |
| | 8.2 ns | 40 mW | 54H11 | J,W | 74H11 | N | 3-6 | 5-12 |
| | 11 ns | 18 mW | 5411 | J,W | 7411 | N | 3-6 | 5-12 |
| | 42.5 ns | 2 mW | 54L11 | J,W | 74L11 | N | 3-6 | 5-12 |
| Quad 2-Input AND Gates | 4.75 ns | 31 mW | 54S08 | J,W | 74S08 | N | 3-5 | 5-12 |
| | 8.2 ns | 44 mW | 54H08 | J,W | 74H08 | N | 3-5 | 5-12 |
| | 45 ns | 2 mW | 54L08 | J,W | 74L08 | N | 3-5 | 5-12 |
| | 7.8 ns | 4.25 mW | 54LS08 | J,W | 74LS08 | N | 3-5 | 5-12 |
| | 15 ns | 19 mW | 5408 | J,W | 7408 | N | 3-5 | 5-12 |

## AND Gates With Open-Collector Outputs

| Description | Typ. Propagation Delay Time | Typ. Power Dissipation Per Gate | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|
| | | | Mil. | | Coml. | | | |
| Triple 3-Input AND Gates | 6 ns | 28 mW | 54S15 | J,W | 74S15 | N | 3-7 | 5-14 |
| | 19 ns | 4.25 mW | 54LS15 | J,W | 74LS15 | N | 3-7 | 5-14 |
| Quad 2-Input AND Gates | 6.5 ns | 31 mW | 54S09 | J,W | 74S09 | N | 3-5 | 5-14 |
| | 18.5 ns | 19.4 mW | 5409 | J,W | 7409 | N | 3-5 | 5-14 |
| | 19 ns | 4.25 mW | 54LS09 | J,W | 74LS09 | N | 3-5 | 5-14 |
| | 50 ns | 2 mW | 54L09 | J,W | 74L09 | N | 3-5 | 5-14 |

## AND-OR-Invert Gates With Totem-Pole Outputs

| Description | Typ. Propagation Delay Time | Typ. Power Dissipation Per Gate | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|
| | | | Mil. | | Coml. | | | |
| 2-Wide 4-Input | 7.5 ns | 2.75 mW | 54LS55 | J,W | 74LS55 | N | 3-18 | 5-24 |
| | 43 ns | 1.5 mW | 54L55 | J,W | 74L55 | N | 3-18 | 5-24 |
| Dual 2-Wide 2-Input | 3.5 ns | 28 mW | 54S51 | J,W | 74S51 | N | 3-15 | 5-24 |
| | 7.5 ns | 2.75 mW | 54LS51 | J,W | 74LS51 | N | 3-15 | 5-24 |
| | 10.5 ns | 14 mW | 5451 | J,W | 7451 | N | 3-15 | 5-24 |
| | 43 ns | 1.5 mW | 54L51 | J,W | 74L51 | N | 3-15 | 5-24 |
| 4-Wide 4-2-3-2-Input | 3.5 ns | 29 mW | 54S64 | J,W | 74S64 | N | 3-19 | 5-24 |
| 4-Wide 2-Input | 10.5 ns | 23 mW | 5454 | J,W | 7454 | N | 3-17 | 5-24 |
| 4-Wide 2-3-3-2-Input | 11 ns | 4.5 mW | 54LS54 | J,W | 74LS54 | N | 3-17 | 5-24 |
| | 43 ns | 1.5 mW | 54L54 | J,W | 74L54 | N | 3-17 | 5-24 |

## AND-OR-Invert Gates With Open-Collector Outputs

| Description | Typ. Propagation Delay Time | Typ. Power Dissipation Per Gate | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|
| | | | Mil. | | Coml. | | | |
| 4-Wide 4-2-3-2-Input | 5.5 ns | 36 mW | 54S65 | J,W | 74S65 | N | 3-20 | 5-28 |

## Buffers/Clock Drivers With Totem-Pole Outputs

| Description | Low-Level Output Current | High-Level Output Current | Typ. Delay Time | Typ. Power Per Gate | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Mil. | | Coml. | | | |
| Dual 4-Input NAND Buffers | 60 mA | −3 mA | 4 ns | 44 mW | 54S40 | J,W | 74S40 | N | 3-12 | 5-22 |
| | 60 mA | −1.5 mA | 7.5 ns | 44 mW | 54H40 | J,W | 74H40 | N | 3-12 | 5-22 |
| | 48 mA | −1.2 mA | 10.5 ns | 26 mW | 5440 | J,W | 7440 | N | 3-12 | 5-22 |
| | 24 mA | −1.2 mA | 10 ns | 4.3 mW | | | 74LS40 | N | 3-12 | 5-22 |
| | 12 mA | −1.2 mA | 10 ns | 4.3 mW | 54LS40 | J,W | | | 3-12 | 5-22 |
| Quad 2-Input NAND Buffers | 48 mA | −1.2 mA | 10.5 ns | 27 mW | 5437 | J,W | 7437 | N | 3-11 | 5-22 |
| | 24 mA | −1.2 mA | 10 ns | 4.3 mW | | | 74LS37 | N | 3-11 | 5-22 |
| | 12 mA | −1.2 mA | 10 ns | 4.3 mW | 54LS37 | J,W | | | 3-11 | 5-22 |

## Buffer And Interface Gates With Open-Collector Outputs

| Description | High-Level Output Voltage | Low-Level Output Current | Typ. Delay Time | Typ. Power Per Gate | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Mil. | | Coml. | | | |
| Quad 2-Input NAND Buffers | 15 V | 16 mA | 13.5 ns | 10 mW | 5426 | J,W | 7426 | N | 3-10 | 5-10 |
| | 15 V | 8 mA | 16 ns | 2 mW | | | 74LS26 | N | 3-10 | 5-10 |
| | 15 V | 4 mA | 16 ns | 2 mW | 54LS26 | J,W | | | 3-10 | 5-10 |
| | 15 V | 3.6 mA | 33 ns | 1 mW | | | 74L26 | N | 3-10 | 5-10 |
| | 15 V | 2 mA | 33 ns | 1 mW | 54L26 | J,W | | | 3-10 | 5-10 |
| | 5.5 V | 48 mA | 12.5 ns | 24.4 mW | 5438 | J,W | 7438 | N | 3-11 | 5-10 |
| | 5.5 V | 24 mA | 13 ns | 4.3 mW | | | 74LS38 | N | 3-11 | 5-10 |
| | 5.5 V | 12 mA | 13 ns | 4.3 mW | 54LS38 | J,W | | | 3-11 | 5-10 |
| Hex Buffers/Drivers | 30 V | 40 mA | 13 ns | 21 mW | | | 7407 | N | 3-4 | 5-10 |
| | 30 V | 30 mA | 13 ns | 21 mW | 5407 | J,W | | | 3-4 | 5-10 |
| | 15 V | 40 mA | 13 ns | 21 mW | | | 7417 | N | 3-8 | 5-10 |
| | 15 V | 30 mA | 13 ns | 21 mW | 5417 | J,W | | | 3-8 | 5-10 |
| Hex Inverter Buffers/Drivers | 30 V | 40 mA | 12.5 ns | 26 mW | | | 7406 | N | 3-4 | 5-10 |
| | 30 V | 30 mA | 12.5 ns | 26 mW | 5406 | J,W | | | 3-4 | 5-10 |
| | 15 V | 40 mA | 12.5 ns | 26 mW | | | 7416 | N | 3-7 | 5-10 |
| | 15 V | 30 mA | 12.5 ns | 26 mW | 5416 | J,W | | | 3-7 | 5-10 |

## Bus Interface Gates With TRI-STATE® Totem-Pole Outputs

| Description | Typ. Propagation Delay Time | Typ. Power Dissipation Per Gate | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|
| | | | Mil. | | Coml. | | | |
| Quad-Bus Buffers | 10 ns | 40 mW | 54125 | J,W | 74125 | N | 3-35 | 5-48 |
| | 10 ns | 45 mW | 54126 | J,W | 74126 | N | 3-36 | 5-48 |
| | 10 ns | 14.4 mW | 54LS125A | J,W | 74LS125A | N | 3-35 | 5-48 |
| | 10 ns | 14.4 mW | 54LS126A | J,W | 74LS126A | N | 3-36 | 5-48 |
| | 10 ns | 40 mW | 7093 | J,W | 8093 | N | 7-16 | 7-17 |
| | 10 ns | 45 mW | 7094 | J,W | 8094 | N | 7-16 | 7-17 |
| Hex Bus Drivers | 10 ns | 13 mW | 54LS365A | J,W | 74LS365A | N | 3-62 | 5-64 |
| | 10 ns | 13 mW | 54LS367A | J,W | 74LS367A | N | 3-63 | 5-64 |
| | 12 ns | 54 mW | 54365 | J,W | 74365 | N | 3-62 | 5-64 |
| | 12 ns | 54 mW | 54367 | J,W | 74367 | N | 3-63 | 5-64 |
| | 12 ns | 54 mW | 7095 | J,W | 8095 | N | 7-18 | 7-19 |
| | 12 ns | 54 mW | 7097 | J,W | 8097 | N | 7-18 | 7-19 |
| | 33 ns | 3.3 mW | 70L95 | J,W | 80L95 | N | 7-18 | 7-19 |
| | 33 ns | 3.3 mW | 70L97 | J,W | 80L97 | N | 7-18 | 7-19 |
| Hex Inverter Bus Drivers | 10 ns | 13 mW | 54LS366A | J,W | 74LS366A | N | 3-63 | 5-64 |
| | 10 ns | 13 mW | 54LS368A | J,W | 74LS368A | N | 3-63 | 5-64 |
| | 11 ns | 49 mW | 54366 | J,W | 74366 | N | 3-63 | 5-64 |
| | 11 ns | 49 mW | 54368 | J,W | 74368 | N | 3-63 | 5-64 |
| | 11 ns | 49 mW | 7096 | J,W | 8096 | N | 7-18 | 7-19 |
| | 11 ns | 49 mW | 7098 | J,W | 8098 | N | 7-18 | 7-19 |
| | 30 ns | 2.5 mW | 70L96 | J,W | 80L96 | N | 7-18 | 7-19 |
| | 30 ns | 2.5 mW | 70L98 | J,W | 80L98 | N | 7-18 | 7-19 |
| Octal Drivers | 14.5 ns | 10 mW | 71LS95A | J,W | 81LS95A | N | 3-6 | 7-33 |
| | 14.5 ns | 10 mW | 71LS97A | J,W | 81LS97A | N | 3-6 | 7-33 |
| Octal Inverter Drivers | 9.5 ns | 8 mW | 71LS96A | J,W | 81LS96A | N | 3-6 | 7-33 |
| | 9.5 ns | 8 mW | 71LS98A | J,W | 81LS98A | N | 3-6 | 7-33 |
| 12-Input NAND Gates | 4.5 ns | 45 mW | 54S134 | J,W | 74S134 | N | 3-37 | 5-48 |

## Expandable Gates

| Description | Typ. Propagation Delay Time | Typ. Power Dissipation Per Gate | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|
| | | | Mil. | | Coml. | | | |
| Dual 2-Wide AND-OR-INVERT Gates | 6.5 ns | 29 mW | 54H50 | J | 74H50 | N | 3-14 | 5-18 |
| | 10.5 ns | 14 mW | 5450 | J,W | 7450 | N | 3-14 | 5-18 |
| 4-Wide AND-OR-INVERT Gates | 10.5 ns | 23 mW | 5453 | J,W | 7453 | N | 3-16 | 5-18 |
| Dual 4-Input NOR Gates With Strobe | 10.5 ns | 23 mW | 5423 | J,W | 7423 | N | 3-9 | 5-18 |

## Expanders

| Description | Typ. Total Power Dissipation | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|
| | | Mil. | | Coml. | | | |
| Dual 4-Input Expanders | 4 mW | 5460 | J,W | 7460 | N | 3-18 | 5-26 |
| 3-2-2-3-Input AND-OR Expanders | 25 mW | 54H62 | J | 74H62 | N | 3-19 | 5-27 |

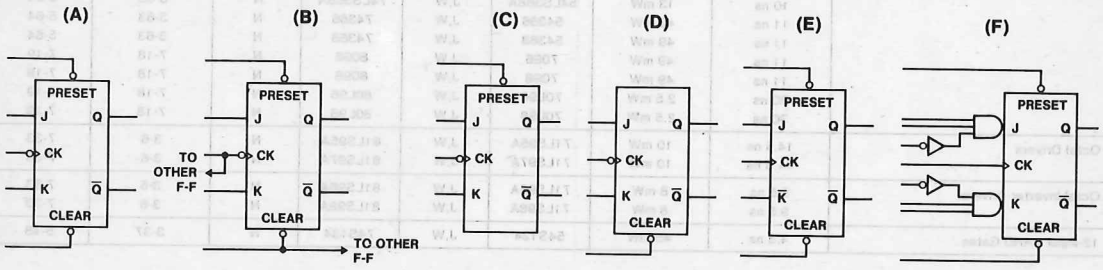
## Flip-Flops, Gated

| Typ. Characteristics | | Data Times | | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Mil. | | Coml. | | | |
| $f_{MAX}$ (MHz) | Pwr/F-F (mW) | Setup (ns) | Hold (ns) | | | | | | |
| 45 | 105 | 15 | 0 | 7511 | J,W | 8511 | N | 3-6 | 7-47 |
| 30 | 73 | 24 | 0 | 7613 | J,W | 8613 | N | 3-6 | 7-47 |
| 10 | 8.0 | 110 | 0 | 75L12 | J,W | 85L12 | N | 3-6 | 7-47 |
| 9 | 9.3 | 80 | 0 | 75L11 | J,W | 85L11 | N | 3-6 | 7-47 |
| 7 | 7.3 | 100 | 0 | 76L13 | J,W | 86L13 | N | 3-6 | 7-47 |

## Flip-Flops, Single and Dual J-K Edge Triggered

| Dwg. Ref. | Typ. Characteristics | | Data Times | | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Mil. | | Coml. | | | |
| | $f_{MAX}$ (MHz) | Pwr/F-F (mW) | Setup (ns) | Hold (ns) | | | | | | |
| A | 125 | 75 | 6↓ | 0↓ | 54S112 | J,W | 74S112 | N | 3-33 | 5-35 |
| | 50 | 100 | 13↓ | 0↓ | 54H106 | J,W | 74H106 | N | 3-31 | 5-42 |
| | 45 | 10 | 20↓ | 0↓ | 54LS76A | J,W | 74LS76A | N | 3-24 | 5-33 |
| | 45 | 10 | 20↓ | 0↓ | 54LS112A | J,W | 74LS112A | N | 3-33 | 5-33 |
| B | 125 | 75 | 6↓ | 0↓ | 54S114 | J,W | 74S114 | N | 3-33 | 5-35 |
| | 50 | 100 | 13↓ | 0↓ | 54H108 | J,W | 74H108 | N | 3-32 | 5-42 |
| | 45 | 10 | 20↓ | 0↓ | 54LS78A | J,W | 74LS78A | N | 3-25 | 5-33 |
| | 45 | 10 | 20↓ | 0↓ | 54LS114A | J,W | 74LS114A | N | 3-33 | 5-33 |
| C | 125 | 75 | 6↓ | 0↓ | 54S113 | J,W | 74S113 | N | 3-33 | 5-35 |
| | 45 | 10 | 20↓ | 0↓ | 54LS113A | J,W | 74LS113A | N | 3-33 | 5-33 |
| D | 50 | 100 | 13↓ | 0↓ | 54H103 | J,W | 74H103 | N | 3-31 | 5-42 |
| | 45 | 10 | 20↓ | 0↓ | 54LS73A | J,W | 74LS73A | N | 3-22 | 5-33 |
| | 45 | 10 | 20↓ | 0↓ | 54LS107A | J,W | 74LS107A | N | 3-31 | 5-33 |
| E | 40 | 45 | 15↑ | 10↑ | 9024 | J,W | 8024 | N | 7-140 | 7-141 |
| | 33 | 10 | 25↑ | 0↑ | 54LS109A | J,W | 74LS109A | N | 3-32 | 5-33 |
| | 33 | 45 | 10↑ | 6↑ | 54109 | J,W | 74109 | N | 3-32 | 5-29 |
| F | 35 | 65 | 20↑ | 5↑ | 5470 | J,W | 7470 | N | 3-20 | 5-29 |

↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for rising edge, ↓ for the falling edge.

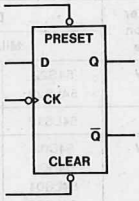


## Flip-Flops, Dual D-Type

| Dwg. Ref. | Typ. Characteristics | | Data Times | | Device Type and Package | | | | Connection Diagram | Electrical Tables |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Mil. | | Coml. | | | |
| | $f_{MAX}$ (MHz) | Pwr/F-F (mW) | Setup (ns) | Hold (ns) | | | | | Page No. | Page No. |
| G | 110 | 75 | 3↑ | 2↑ | 54S74 | J,W | 74S74 | N | 3-23 | 5-35 |
| | 43 | 75 | 15↑ | 5↑ | 54H74 | J,W | 74H74 | N | 3-23 | 5-38 |
| | 33 | 10 | 20↑ | 0↑ | 54LS74A | J,W | 74LS74A | N | 3-23 | 5-29 |
| | 25 | 43 | 20↑ | 5↑ | 5474 | J,W | 7474 | N | 3-23 | 5-29 |
| | 6 | 4 | 50↑ | 15↑ | 54L74 | J,W | 74L74 | N | 3-23 | 5-31 |

↑↑ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

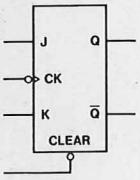
(G)



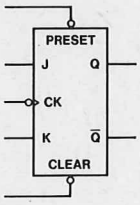

## Flip-Flops, Single and Dual Pulse-Triggered

| Dwg. Ref. | Typ. Characteristics | | Data Times | | Device Type and Package | | | | Connection Diagram | Electrical Tables |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Mil. | | Coml. | | | |
| | $f_{MAX}$ (MHz) | Pwr/F-F (mW) | Setup (ns) | Hold (ns) | | | | | Page No. | Page No. |
| H | 20 | 50 | 0↑ | 0↓ | 5473 | J,W | 7473 | N | 3-22 | 5-29 |
| | 20 | 50 | 0↑ | 0↓ | 54107 | J,W | 74107 | N | 3-31 | 5-29 |
| | 6 | 3.8 | 0↑ | 0↓ | 54L73 | J,W | 74L73 | N | 3-22 | 5-31 |
| I | 20 | 50 | 0↑ | 0↓ | 5476 | J,W | 7476 | N | 3-24 | 5-29 |
| J | 6 | 3.8 | 0↑ | 0↓ | 54L78 | J,W | 74L78 | N | 3-25 | 5-31 |
| K | 20 | 50 | 0↑ | 0↓ | 5472 | J,W | 7472 | N | 3-22 | 5-29 |
| | 6 | 3.8 | 0↑ | 0↓ | 54L72 | J,W | 74L72 | N | 3-22 | 5-31 |
| L | 6 | 3.8 | 0↑ | 0↓ | 54L71 | J,W | 74L71 | N | 3-21 | 5-31 |

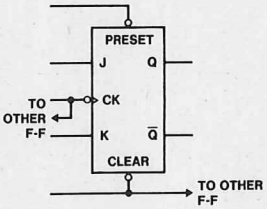
(H)



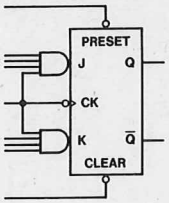

(I)



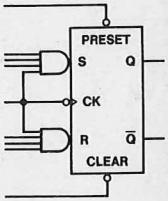

(J)




(K)




(L)



## Latches, $\overline{S}$-$\overline{R}$

| Description | Typ. Propagation Delay Time | Typ. Total Power Dissipation | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|
| | | | Mil. | | Coml. | | | |
| Quad $\overline{S}$-$\overline{R}$ Latches | 10 ns | 19 mW | 54LS279 | J,W | 74LS279 | N | 3-59 | 5-63 |

## Line Drivers, 50-OHM/75-OHM

| Description | Low-Level Output Current | High-Level Output Current | Typ. Delay Time | Typ. Power Per Gate | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Mil. | | Coml. | | | |
| Dual 4-Input NAND Line Drivers | 60 mA | −40 mA | 4 ns | 44 mW | 54S140 | J,W | 74S140 | N | 3-38 | 5-22 |

## NAND Gates and Inverters with Open-Collector Outputs

| Description | Typ. Propagation Delay Time | Typ. Power Dissipation Per Gate | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|
| | | | Mil. | | Coml. | | | |
| Dual 4-Input NAND Gates | 5 ns | 17.5 mW | 54S22 | J,W | 74S22 | N | 3-9 | 5-6 |
| | 10 ns | 2 mW | 54LS22 | J,W | 74LS22 | N | 3-9 | 5-6 |
| Triple 3-Input NAND Gates | 10 ns | 2 mW | 54LS12 | J,W | 74LS12 | N | 3-6 | 5-6 |
| Quad 2-Input NAND Gates | 5 ns | 17.5 mW | 54S03 | J,W | 74S03 | N | 3-3 | 5-6 |
| | 8 ns | 22 mW | 54H01 | J,W | 74H01 | N | 3-2 | 5-6 |
| | 10 ns | 2 mW | 54LS01 | J,W | 74LS01 | N | 3-2 | 5-6 |
| | 10 ns | 2 mW | 54LS03 | J,W | 74LS03 | N | 3-3 | 5-6 |
| | 22 ns | 10 mW | 5401 | J,W | 7401 | N | 3-2 | 5-6 |
| | 22 ns | 10 mW | 5403 | J,W | 7403 | N | 3-3 | 5-6 |
| | 41 ns | 1 mW | 54L01 | J,W | 74L01 | N | 3-2 | 5-6 |
| | 41 ns | 1 mW | 54L03 | J,W | 74L03 | N | 3-3 | 5-6 |
| | 115 ns | 1.8 mW | | | 80L06 | N | 7-12 | 7-13 |
| | | 11 mW | 9012C | J,W | 8012C | N | 7-140 | 7-141 |
| Hex Inverters | 5 ns | 17.5 mW | 54S05 | J,W | 74S05 | N | 3-4 | 5-6 |
| | 10 ns | 2 mW | 54LS05 | J,W | 74LS05 | N | 3-4 | 5-6 |
| | 22 ns | 10 mW | 5405 | J,W | 7405 | N | 3-4 | 5-6 |
| | 46 ns | 1.2 mW | 54L05 | J,W | 74L05 | N | 3-4 | 5-6 |

## Gates, Buffers, Drivers, and Bus Transceivers With TRI-STATE® Outputs

| Description | Typ. Propagation Delay Time | Maximum Source Current | Maximum Sink Current | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Mil. | | Coml. | | | |
| Octal Bus Buffers/Drivers | 5 ns | −15 mA | 64 mA | | | 74S240 | N | 3-54 | 5-53 |
| | 5 ns | −12 mA | 48 mA | 54S240 | J,W | | | 3-54 | 5-53 |
| | 5 ns | −15 mA | 64 mA | | | 74S940 | N | 3-66 | 5-53 |
| | 5 ns | −12 mA | 48 mA | 54S940 | J,W | | | 3-66 | 5-53 |
| | 5 ns | −15 mA | 64 mA | | | 74S241 | N | 3-54 | 5-53 |
| | 5 ns | −12 mA | 48 mA | 54S241 | J,W | | | 3-54 | 5-53 |
| | 5 ns | −15 mA | 64 mA | | | 74S941 | N | 3-66 | 5-53 |
| | 5 ns | −12 mA | 48 mA | 54S941 | J,W | | | 3-66 | 5-53 |
| | 5 ns | −15 mA | 64 mA | | | 74S244 | N | 3-55 | 5-53 |
| | 5 ns | −12 mA | 48 mA | 54S244 | J,W | | | 3-55 | 5-53 |
| | 10 ns | −15 mA | 24 mA | | | 74LS240 | N | 3-54 | 5-53 |
| | 10 ns | −12 mA | 12 mA | 54LS240 | J,W | | | 3-54 | 5-53 |
| | 10 ns | −15 mA | 24 mA | | | 74LS241 | N | 3-54 | 5-53 |
| | 10 ns | −12 mA | 12 mA | 54LS241 | J,W | | | 3-54 | 5-53 |
| | 10 ns | −15 mA | 24 mA | | | 74LS244 | N | 3-55 | 5-53 |
| | 10 ns | −12 mA | 12 mA | 54LS244 | J,W | | | 3-55 | 5-53 |
| Quadruple Transceivers | 5 ns | −15 mA | 64 mA | | | 74S242 | N | 3-55 | 5-57 |
| | 5 ns | −12 mA | 48 mA | 54S242 | J,W | | | 3-55 | 5-57 |
| | 5 ns | −15 mA | 64 mA | | | 74S243 | N | 3-55 | 5-57 |
| | 5 ns | −12 mA | 48 mA | 54S243 | J,W | | | 3-55 | 5-57 |
| | 11 ns | −15 mA | 24 mA | | | 74LS242 | N | 3-55 | 5-57 |
| | 11 ns | −12 mA | 12 mA | 54LS242 | J, W | | | 3-55 | 5-57 |
| | 12 ns | −15 mA | 24 mA | | | 74LS243 | N | 3-55 | 5-57 |
| | 12 ns | −15 mA | 12 mA | 54LS243 | J, W | | | 3-55 | 5-57 |
| Octal Transceivers (MSI) | 12 ns | −15 mA | 24 mA | | | 74LS245 | N | 3-56 | 5-60 |
| | 12 ns | −12 mA | 12 mA | 54LS245 | J,W | | | 3-56 | 5-60 |

## NAND Gates and Inverters with Totem-Pole Outputs

| Description | Typ. Propagation Delay Time | Typ. Power Dissipation Per Gate | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|
| | | | Mil. | | Coml. | | | |
| Dual 4-Input NAND Gates | 3 ns | 19 mW | 54S20 | J,W | 74S20 | N | 3-8 | 5-4 |
| | 6 ns | 22 mW | 54H20 | J,W | 74H20 | N | 3-8 | 5-4 |
| | 5 ns | 2 mW | 54LS20 | J,W | 74LS20 | N | 3-8 | 5-4 |
| | 10 ns | 10 mW | 5420 | J,W | 7420 | N | 3-8 | 5-4 |
| | 33 ns | 1 mW | 54L20 | J,W | 74L20 | N | 3-8 | 5-4 |
| | | 11 mW | 9004C | J,W | 8004C | N | 7-140 | 7-141 |
| Dual 5-Input NAND Gates | 10 ns | 20 mW | 7092 | J,W | 8092 | N | 7-14 | 7-15 |
| Triple 3-Input NAND Gates | 3 ns | 19 mW | 54S10 | J,W | 74S10 | N | 3-5 | 5-4 |
| | 5 ns | 2 mW | 54LS10 | J,W | 74LS10 | N | 3-5 | 5-4 |
| | 6 ns | 22 mW | 54H10 | J,W | 74H10 | N | 3-5 | 5-4 |
| | 10 ns | 10 mW | 5410 | J,W | 7410 | N | 3-5 | 5-4 |
| | 33 ns | 1 mW | 54L10 | J,W | 74L10 | N | 3-5 | 5-4 |
| | | 11 mW | 9003C | J,W | 8003C | N | 7-140 | 7-141 |
| Quad 2-Input NAND Gates | 3 ns | 19 mW | 54S00 | J,W | 74S00 | N | 3-2 | 5-4 |
| | 5 ns | 2 mW | 54LS00 | J,W | 74LS00 | N | 3-2 | 5-4 |
| | 6 ns | 22 mW | 54H00 | J,W | 74H00 | N | 3-2 | 5-4 |
| | 10 ns | 10 mW | 5400 | J,W | 7400 | N | 3-2 | 5-4 |
| | 33 ns | 1 mW | 54L00 | J,W | 74L00 | N | 3-2 | 5-4 |
| | | 11 mW | 9002C | J,W | 8002C | N | 7-140 | 7-141 |
| Hex Inverters | 3 ns | 19 mW | 54S04 | J,W | 74S04 | N | 3-3 | 5-4 |
| | 5 ns | 2 mW | 54LS04 | J,W | 74LS04 | N | 3-3 | 5-4 |
| | 6 ns | 22 mW | 54H04 | J,W | 74H04 | N | 3-3 | 5-4 |
| | 10 ns | 10 mW | 5404 | J,W | 7404 | N | 3-3 | 5-4 |
| | 33 ns | 1 mW | 54L04 | J,W | 74L04 | N | 3-3 | 5-4 |
| | | 11 mW | 9016C | J,W | 8016C | N | 7-140 | 7-141 |
| 8-Input NAND Gates | 3 ns | 19 mW | 54S30 | J,W | 74S30 | N | 3-10 | 5-4 |
| | 6 ns | 22 mW | 54H30 | J,W | 74H30 | N | 3-10 | 5-4 |
| | 7 ns | 2.4 mW | 54LS30 | J,W | 74LS30 | N | 3-10 | 5-4 |
| | 10 ns | 10 mW | 5430 | J,W | 7430 | N | 3-10 | 5-4 |
| | 33 ns | 1 mW | 54L30 | J,W | 74L30 | N | 3-10 | 5-4 |
| 13-Input NAND Gates | 3 ns | 19 mW | 54S133 | J,W | 74S133 | N | 3-26 | 5-4 |

## NOR, OR Gates with Open-Collector Outputs

| Description | Typ. Propagation Delay Time | Typ. Power Dissipation Per Gate | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|
| | | | Mil. | | Coml. | | | |
| Quad 2-Input Exclusive NOR Gates | 18 ns | 10 mW | 54LS266 | J,W | 74LS266 | N | 3-59 | 5-52 |
| Quad 2-Input Exclusive OR Gates | 18 ns | 7.6 mW | 54LS136 | J,W | 74LS136 | N | 3-37 | 5-52 |
| | 12 ns | 63 mW | 54S136 | J,W | 74S136 | N | 3-37 | 5-52 |

## NOR Gates with Totem-Pole Outputs

| Description | Typ. Propagation Delay Time | Typ. Power Dissipation Per Gate | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|
| | | | Mil. | | Coml. | | | |
| Dual 4-Input NOR Gates With Strobe | 10.5 ns | 23 mW | 5425 | J,W | 7425 | N | 3-9 | 5-8 |
| Triple 3-Input NOR Gates | 8.5 ns | 22 mW | 5427 | J,W | 7427 | N | 3-10 | 5-8 |
| | 7 ns | 4.5 mW | 54LS27 | J,W | 74LS27 | N | 3-10 | 5-8 |
| Quad 2-Input NOR Gates | 3.5 ns | 29 mW | 54S02 | J,W | 74S02 | N | 3-3 | 5-8 |
| | 5.5 ns | 2.75 mW | 54LS02 | J,W | 74LS02 | N | 3-3 | 5-8 |
| | 10 ns | 14 mW | 5402 | J,W | 7402 | N | 3-3 | 5-8 |
| | 33 ns | 1.5 mW | 54L02 | J,W | 74L02 | N | 3-3 | 5-8 |

## One Shots, Retriggerable

| Description | No. of Inputs | | Direct Clear | Output Pulse Range | Typ. Total Power | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Positive | Negative | | | | Mil. | | Coml. | | | |
| Single | 2 | 2 | Yes | 45 ns—∞ | 30 mW | 54LS122 | J,W | 74LS122 | N | 3-34 | 5-46 |
| | 2 | 2 | Yes | 50 ns—∞ | 90 mW | 9601 | J,W | 8601 | N | 7-173 | 7-174 |
| Dual | 1 | 1 | Yes | 45 ns—∞ | 230 mW | 54123 | J,W | 74123 | N | 3-35 | 5-46 |
| | 1 | 1 | Yes | 90 ns—∞ | 25 mW | 54L123A | J,W | 74L123A | N | 3-35 | 5-46 |
| | 1 | 1 | Yes | 45 ns—∞ | 60 mW | 54LS123 | J,W | 74LS123 | N | 3-35 | 5-46 |
| | 1 | 1 | Yes | 72 ns—∞ | 195 mW | 9602 | J,W | 8602 | N | 7-173 | 7-174 |
| | 2 | 2 | Yes | 72 ns—∞ | 275 mW | 7853 | J,W | 8853 | N | 7-130 | 7-131 |

## One Shots with Schmitt-Trigger Inputs

| Description | No. of Inputs | | Output Pulse Range | Typ. Total Power | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|---|
| | Positive | Negative | | | Mil. | | Coml. | | | |
| Single | 1 | 2 | 40 ns—28 s | 90 mW | 54121 | J,W | 74121 | N | 3-34 | 5-44 |
| Dual | 1 | 1 | 20 ns—70 s | 23 mW | | | 74LS221 | N | 3-54 | 5-44 |
| | 1 | 1 | 20 ns—49 s | 23 mW | 54LS221 | J,W | | | 3-54 | 5-44 |

## OR Gates with Totem-Pole Outputs

| Description | Typ. Propagaton Delay Time | Typ Power Dissipation Per Gate | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|
| | | | Mil. | | Coml. | | | |
| Quad 2-Input OR Gates | 4 ns | 35mW | 54S32 | J,W | 74S32 | N | 3-11 | 5-20 |
| | 10 ns | 5 mW | 54LS32 | J,W | 74LS32 | N | 3-11 | 5-20 |
| | 12 ns | 24 mW | 5432 | J,W | 7432 | N | 3-11 | 5-20 |
| | 45 ns | 2.4 mW | 54L32 | J,W | 74L32 | N | 3-11 | 5-20 |
| Quad 2-Input Exclus. OR Gates | 6.75 ns | 62.5 mW | 54S86 | J,W | 74S86 | N | 3-26 | 5-40 |
| | 9 ns | 7.5 mW | 54LS86 | J,W | 74LS86 | N | 3-26 | 5-40 |
| | 9 ns | 7.5 mW | 54LS386 | J,W | 74LS386 | N | 3-65 | 5-40 |
| | 14 ns | 41 mW | 5486 | J,W | 7486 | N | 3-26 | 5-40 |
| | 30 ns | 7.5 mW | 54L86 | J,W | 74L86 | N | 3-26 | 5-40 |
| Quad Exclus. OR/NOR Gate | 8.5 | 82 mW | 54S135 | J,W | 74S135 | N | 3-37 | 5-50 |

## Schmitt-Triggers with Totem-Pole Outputs

| Description | Typ. Hysteresis | Typ. Delay Time | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|
| | | | Mil. | | Coml. | | | |
| Dual 4-Input NAND Schmitt Triggers | 0.8 V | 16.5 ns | 5413 | J,W | 7413 | N | 3-6 | 5-16 |
| | 0.8 V | 15 ns | 54LS13 | J,W | 74LS13 | N | 3-6 | 5-16 |
| Quad 2-Input NAND Schmitt Triggers | 0.8 V | 15 ns | 54132 | J,W | 74132 | N | 3-36 | 5-16 |
| | 0.8 V | 15 ns | 54LS132 | J,W | 74LS132 | N | 3-36 | 5-16 |
| Hex Schmitt Trigger Inverters | 0.8 V | 15 ns | 5414 | J,W | 7414 | N | 3-7 | 5-16 |
| | 0.8 V | 15 ns | 54LS14 | J,W | 74LS14 | N | 3-6 | 5-16 |

# Section 2
# MSI Functional Index/ Selection Guide

2

The following pages contain functional indexes and selection guides designed to simplify the choice of a particular function to fit a specific application. Essential characteristics of similar or like functions are grouped for comparative analysis, and the electrical specifications are referenced by page number. The following categories of functions are covered:


| DESCRIPTION | PAGE NUMBER |
|---|---|
| **MSI Functions** | |
| Adders | 2-2 |
| Arithmetic Logic Units, Look-Ahead Carry Generators | 2-2 |
| Arithmetic Operators | 2-2 |
| Code Converters | 2-2 |
| Comparators | 2-2 |
| Counters, Asynchronous (Ripple Clock)—Negative-Edge Triggered | 2-3 |
| Counters, Synchronous—Positive-Edge Triggered | 2-3 |
| Data Selectors/Multiplexers | 2-4 |
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| Display Decoders/Drivers | 2-5 |
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| Parity Generators/Checkers | 2-6 |
| Priority Encoders | 2-6 |
| Register Files | 2-6 |
| Registers, Other | 2-6 |
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## Adders

| Description | Typ. Carry Time | Typ. Add Time | Typ. Power Dissipation Per Bit | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Mil. | | Coml. | | | |
| Single 4-Bit Full Adders | 11 ns | 11 ns | 110 mW | 54S283 | J,W | 74S283 | N | 3-25 | 6-22 |
| | 10 ns | 15 ns | 24 mW | 54LS83A | J,W | 74LS83A | N | 3-25 | 6-22 |
| | 10 ns | 15 ns | 24 mW | 54LS283 | J,W | 74LS283 | N | 3-25 | 6-22 |
| | 10 ns | 16 ns | 76 mW | 5483 | J,W | 7483 | N | 3-25 | 6-22 |

## Arithmetic Logic Units, Look-Ahead Carry Generators

| Description | Typ. Carry Time | Typ. Add Time | Typ. Total Power Dissipation | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Mil. | | Coml. | | | |
| 4-Bit Arithmetic Logic Units/Function Generators | 7 ns | 17.5 ns | 600 mW | 54S181 | J,W | 74S181 | N | 3-49 | 6-138 |
| | 10 ns | 12 ns | 525 mW | 54S381 | J,W | 74S381 | N | 3-49 | 6-231 |
| | 12.5 ns | 24 ns | 455 mW | 54181 | J,W | 74181 | N | 3-49 | 6-138 |
| Look-Ahead Carry Generators | 7 ns | | 260 mW | 54S182 | J,W | 74S182 | N | 3-49 | 6-145 |

## Arithmetic Operators

| Description | Typ. Delay Time | Typ. Total Power Dissipation | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|
| | | | Mil. | | Coml. | | | |
| Quad 2-Input EXCLUSIVE-NOR Gates | 18 ns | 40 mW | 54LS266 | J,W | 74LS266 | N | 3-59 | 5-52 |
| Quad 2-Input EXCLUSIVE-OR Gates With Open Collector Outputs | 18 ns | 30 mW | 54LS136 | J,W | 74LS136 | N | 3-37 | 5-52 |
| Quad 2-Input EXCLUSIVE-OR Gates with Totem-Pole Outputs | 7 ns | 250 mW | 54S86 | J,W | 74S86 | N | 3-26 | 5-40 |
| | 9 ns | 30 mW | 54LS86 | J,W | 74LS86 | N | 3-26 | 5-40 |
| | 9 ns | 30 mW | 54LS386 | J,W | 74LS386 | N | 3-65 | 5-64 |
| | 14 ns | 150 mW | 5486 | J,W | 7486 | N | 3-26 | 5-40 |
| | 29 ns | 15 mW | 54L86 | J,W | 74L86 | N | 3-26 | 5-40 |
| Quad EXCLUSIVE-OR/NOR Gates | 8 ns | 325 mW | 54S135 | J,W | 74S135 | N | 3-37 | 5-50 |

## Code Converters

| Description | Typ. Delay Time Per Package Level | Typ. Total Power Dissipation | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|
| | | | Mil. | | Coml. | | | |
| 6-Bit Binary to 6-Bit BCD Converters | 25 ns | 280 mW | 54185A | J,W | 74185A | N | 3-50 | 6-151 |
| | 31 ns | 350 mW | | | 8899 | N | 7-136 | 7-137 |
| 6-Line BCD to 6-Line Binary, or 4-Line to 4-Line BCD 9's/BCD 10's Converters | 25 ns | 280 mW | 54184 | J,W | 74184 | N | 3-50 | 6-151 |
| | 31 ns | 350 mW | | | 8898 | N | 7-136 | 7-137 |
| 7 by 9 Character Generators (ASCII to Dot Matrix) | | 500 mW | 7678 | J,W | 8678 | N | 7-117 | 7-117 |
| | | 500 mW | 7679 | J,W | 8679 | N | 7-117 | 7-117 |

## Comparators

| Description | Typ. Compare Time | Typ. Total Power Dissipation | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|
| | | | Mil. | | Coml. | | | |
| 4-Bit Magnitude Comparators | 20 ns | 175 mW | 7200 | J,W | 8200 | N | 7-35 | 7-36 |
| | 20 ns | 52 mW | 54LS85 | J,W | 74LS85 | N | 3-26 | 6-29 |
| | 21 ns | 275 mW | 5485 | J,W | 7485 | N | 3-26 | 6-29 |
| | 70 ns | 20 mW | 54L85 | J,W | 74L85 | N | 3-26 | 6-29 |
| | 70 ns | 75 mW | 76L24 | J,W | 86L24 | N | 7-108 | 7-109 |
| 6-Bit Magnitude Comparators | 20 ns | 250 mW | 7131 | J,W | 8131 | N | 7-29 | 7-30 |
| | 20 ns | 250 mW | 7136 | J,W | 8136 | N | 7-29 | 7-30 |
| | 21 ns | 205 mW | 7160 | J,W | 8160 | N | 7-27 | 7-28 |
| 10-Bit Magnitude Comparators | 21 ns | 240 mW | 7130 | J,W | 8130 | N | 7-27 | 7-28 |

## Counters, Asynchronous (Ripple Clock)—Negative-Edge Triggered

| Description | Count Freq. | Parallel Load | Clear | Typ. Total Power Dissipation | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Mil. | | Coml. | | | |
| 4-Bit Binary | 100 MHz | Yes | Low | 375 mW | 54S197 | J,W | 74S197 | N | 3-52 | 6-127 |
| | 40 MHz | Yes | Low | 240 mW | 54197 | J,W | 74197 | N | 3-52 | 6-127 |
| | 35 MHz | Yes | Low | 150 mW | 54177 | J,W | 74177 | N | 3-48 | 6-127 |
| | 32 MHz | None | High | 39 mW | 54LS93 | J,W | 74LS93 | N | 3-29 | 6-37 |
| | 32 MHz | None | High | 160 mW | 5493A | J,W | 7493A | N | 3-29 | 6-36 |
| | 32 MHz | None | High | 45 mW | 54LS293 | J,W | 74LS293 | N | 3-61 | 6-209 |
| | 30 MHz | Yes | Low | 60 mW | 54LS197 | J,W | 74LS197 | N | 3-52 | 6-127 |
| | 6 MHz | None | High | 20 mW | 54L93 | J,W | 74L93 | N | 3-29 | 6-37 |
| | 6 MHz | None | High | 20 mW | 76L93 | J,W | 86L93 | N | 7-120 | 7-121 |
| Decade | 100 MHz | Yes | Low | 375 mW | 54S196 | J,W | 74S196 | N | 3-52 | 6-127 |
| | 50 MHz | Yes | Low | 240 mW | 54196 | J,W | 74196 | N | 3-52 | 6-127 |
| | 35 MHz | Yes | Low | 150 mW | 54176 | J,W | 74176 | N | 3-48 | 6-127 |
| | 32 MHz | None | High | 45 mW | 54LS290 | J,W | 74LS290 | N | 3-60 | 6-209 |
| | 32 MHz | Set-to-9 | High | 40 mW | 54LS90 | J,W | 74LS90 | N | 3-27 | 6-37 |
| | 32 MHz | Set-to-9 | High | 160 mW | 5490A | J,W | 7490A | N | 3-27 | 6-37 |
| | 30 MHz | Yes | Low | 60 mW | 54LS196 | J,W | 74LS196 | N | 3-52 | 6-127 |
| | 6 MHz | Set-to-9 | High | 20 mW | 54L90 | J,W | 74L90 | N | 3-27 | 6-37 |
| Divide by 12 | 32 MHz | None | High | 39 mW | 54LS92 | J,W | 74LS92 | N | 3-28 | 6-37 |
| | 32 MHz | None | High | 160 mW | 5492A | J,W | 7492A | N | 3-28 | 6-37 |
| Dual 4-Bit Binary/Decade | 25 MHz | None | High | 75 mW | 54LS390 | J,W | 74LS390 | N | 3-65 | 6-236 |
| | 25 MHz | None | High | 75 mW | 54LS393 | J,W | 74LS393 | N | 3-65 | 6-236 |

## Counters, Synchronous—Positive-Edge Triggered

| Description | Count Freq. | Parallel Load | Clear | Typ. Total Power Dissipation | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Mil. | | Coml. | | | |
| 4-Bit Binary | 40 MHz | Sync | Async-L | 475 mW | 54S161 | J,W | 74S161 | N | 3-43 | 6-83 |
| | 40 MHz | Sync | Sync-L | 475 mW | 54S163 | J,W | 74S163 | N | 3-43 | 6-83 |
| | 25 MHz | Sync | Sync-L | 93 mW | 54LS163A | J,W | 74LS163A | N | 3-43 | 6-83 |
| | 25 MHz | Sync | Async-L | 93 mW | 54LS161A | J,W | 74LS161A | N | 3-43 | 6-83 |
| | 25 MHz | Sync | Sync-L | 305 mW | 54163A | J,W | 74163A | N | 3-43 | 6-83 |
| | 25 MHz | Sync | Async-L | 305 mW | 54161A | J,W | 74161A | N | 3-43 | 6-83 |
| | 25 MHz | Sync | Async-L | 305 mW | 9316 | J,W | 8316 | N | 7-153 | 7-154 |
| | 25 MHz | Sync | Sync-L | 375 mW | 7556 | J,W | 8556 | N | 7-81 | 7-82 |
| | 6 MHz | Sync | Async-L | 33 mW | 76L76 | J,W | 86L76 | N | 7-114 | 7-115 |
| 4-Bit Binary Up/Down | 25 MHz | Sync | None | 100 mW | 54LS169A | J,W | 74LS169A | N | 3-45 | 6-107 |
| | 25 MHz | Async | Async-H | 85 mW | 54LS193 | J,W | 74LS193 | N | 3-51 | 6-162 |
| | 20 MHz | Async | Async-H | 325 mW | 54193 | J,W | 74193 | N | 3-51 | 6-162 |
| | 20 MHz | Async | Async-H | 325 mW | 7563 | J,W | 8563 | N | 7-89 | 7-90 |
| | 20 MHz | Async | None | 90 mW | 54LS191 | J,W | 74LS191 | N | 3-50 | 6-155 |
| | 20 MHz | Async | None | 325 mW | 54191 | J,W | 74191 | N | 3-50 | 6-155 |
| | 6 MHz | Async | Async-H | 40 mW | 54L193 | J,W | 74193 | N | 3-51 | 6-162 |
| | 6 MHz | Async | Async-H | 40 mW | 75L63 | J,W | 85L63 | N | 7-89 | 7-90 |
| Decade | 40 MHz | Sync | Sync-L | 475 mW | 54S162 | J,W | 74S162 | N | 3-43 | 6-83 |
| | 40 MHz | Sync | Async-L | 475 mW | 54S160 | J,W | 74S160 | N | 3-43 | 6-83 |
| | 25 MHz | Sync | Sync-L | 93 mW | 54LS162A | J,W | 74LS162A | N | 3-43 | 6-83 |
| | 25 MHz | Sync | Async-L | 93 mW | 54LS160A | J,W | 74LS160A | N | 3-43 | 6-83 |
| | 25 MHz | Sync | Sync-L | 305 mW | 54162A | J,W | 74162A | N | 3-43 | 6-83 |
| | 25 MHz | Sync | Async-L | 305 mW | 54160A | J,W | 74160A | N | 3-43 | 6-83 |
| | 25 MHz | Sync | Async-L | 305 mW | 9310 | J,W | 8310 | N | 7-153 | 7-154 |
| | 25 MHz | Sync | Sync-L | 400 mW | 7555 | J,W | 8555 | N | 7-81 | 7-82 |
| | 6 MHz | Sync | Async-L | 33 mW | 76L75 | J,W | 86L75 | N | 7-114 | 7-115 |
| Decade Up/Down | 25 MHz | Sync | None | 100 mW | 54LS168A | J,W | 74LS168A | N | 3-45 | 6-107 |
| | 25 MHz | Async | Async-H | 85 mW | 54LS192 | J,W | 74LS192 | N | 3-51 | 6-162 |
| | 20 MHz | Async | Async-H | 325 mW | 54192 | J,W | 74192 | N | 3-51 | 6-162 |
| | 20 MHz | Async | None | 100 mW | 54LS190 | J,W | 74LS190 | N | 3-50 | 6-155 |
| | 20 MHz | Async | None | 325 mW | 54190 | J,W | 74190 | N | 3-50 | 6-155 |
| | 20 MHz | Async | Async-H | 325 mW | 7560 | J,W | 8560 | N | 7-89 | 7-90 |
| | 6 MHz | Async | Async-H | 40 mW | 54L192 | J,W | 74L192 | N | 3-51 | 6-162 |
| | 6 MHz | Async | Async-H | 40 mW | 75L60 | J,W | 85L60 | N | 7-89 | 7-90 |
| Modulo-N Divider | 15 MHz | Sync | None | 250 mW | 7520 | J,W | 8520 | N | 7-51 | 7-54 |

## Data Selectors/Multiplexers

| Description | Type of Output | Typ. Delay Times: Data to Inv. Output | Typ. Delay Times: Data to Non-Inv. Output | Typ. Delay Times: From Enable | Type Total Power Dissipation | Device Type and Package: Mil. | | Device Type and Package: Coml | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Quad 2-Line to 1-Line | TRI-STATE* | 4 ns | N/A | 14 ns | 280 mW | 54S258 | J,W | 74S258 | N | 3-58 | 6-198 |
| | TRI-STATE | N/A | 5 ns | 14 ns | 320 mW | 54S257 | J,W | 74S257 | N | 3-57 | 6-198 |
| | Standard | 4 ns | N/A | 7 ns | 195 mW | 54S158 | J,W | 74S158 | N | 3-43 | 6-79 |
| | Standard | N/A | 5 ns | 8 ns | 250 mW | 54S157 | J,W | 74S157 | N | 3-43 | 6-79 |
| | TRI-STATE | 12 ns | N/A | 12 ns | 35 mW | 54LS258B | J,W | 74LS258B | N | 3-58 | 6-198 |
| | TRI-STATE | N/A | 12 ns | 12 ns | 50 mW | 54LS257B | J,W | 74LS257B | N | 3-57 | 6-198 |
| | Standard | 7 ns | N/A | 12 ns | 24 mW | 54LS158 | J,W | 74LS158 | N | 3-43 | 6-79 |
| | Standard | N/A | 9 ns | 14 ns | 49 mW | 54LS157 | J,W | 74LS157 | N | 3-43 | 6-79 |
| | Standard | N/A | 9 ns | 14 ns | 150 mW | 54157 | J,W | 74157 | N | 3-43 | 6-79 |
| | Standard | N/A | 40 ns | 60 ns | 15 mW | 54L157A | J,W | 74L157A | N | 3-43 | 6-79 |
| | Standard | N/A | 9 ns | 14 ns | 150 mW | 9322 | J,W | 8322 | N | 7-167 | 7-168 |
| | Standard | N/A | 40 ns | 60 ns | 15 mW | 71L22 | J,W | 81L22 | N | 7-23 | 7-24 |
| | TRI-STATE | N/A | 9.5 ns | N/A | 200 mW | 7123 | J,W | 8123 | N | 7-23 | 7-24 |
| | TRI-STATE | N/A | 40 ns | N/A | 20 mW | 71L23 | J,W | 81L23 | N | 7-23 | 7-24 |
| Quad 2-Line to 1-Line With Storage | Standard | N/A | 20 ns from clock | N/A | 65 mW | 54LS298 | J,W | 74LS298 | N | 3-61 | 6-212 |
| Dual 4-Line to 1-Line | TRI-STATE | N/A | 6 ns | 12 ns | 275 mW | 54S253 | J,W | 74S253 | N | 3-57 | 6-195 |
| | TRI-STATE | N/A | 15 ns | 25 ns | 38 mW | 54LS253 | J,W | 74LS253 | N | 3-57 | 6-195 |
| | Standard | N/A | 6 ns | 9.5 ns | 225 mW | 54S153 | J,W | 74S153 | N | 3-41 | 6-69 |
| | Standard | N/A | 10.5 ns | 20 ns | 170 mW | 54153 | J,W | 74153 | N | 3-41 | 6-69 |
| | Standard | N/A | 14 ns | 22 ns | 31 mW | 54LS153 | J,W | 74LS153 | N | 3-41 | 6-69 |
| | Standard | 12 ns | 20 ns | 20 ns | 135 mW | 9309 | J,W | 8309 | N | 7-150 | 7-151 |
| | TRI-STATE | N/A | 13.5 ns | 20 ns | 170 mW | 7214 | J,W | 8214 | N | 7-37 | 7-38 |
| | Standard | 15 ns | N/A | 18 ns | 31 mW | 54LS352 | J,W | 74LS352 | N | 3-62 | 6-221 |
| | TRI-STATE | 15 ns | N/A | 15 ns | 38 mW | 54LS353 | J,W | 74LS353 | N | 3-62 | 6-223 |
| 8-Line to 1-Line | TRI-STATE | 4.5 ns | 8 ns | 14 ns | 275 mW | 54S251 | J,W | 74S251 | N | 3-57 | 6-191 |
| | TRI-STATE | 11 ns | 18 ns | 17 ns | 155 mW | 54251 | J,W | 74251 | N | 3-57 | 6-191 |
| | TRI-STATE | 17 ns | 21 ns | 21 ns | 35 mW | 54LS251 | J,W | 74LS251 | N | 3-57 | 6-191 |
| | Standard | 4.5 ns | 8 ns | 9 ns | 225 mW | 54S151 | J,W | 74S151 | N | 3-41 | 6-65 |
| | Standard | 8 ns | 16 ns | 22 ns | 145 mW | 54151A | J,W | 74151A | N | 3-41 | 6-65 |
| | Standard | 11 ns | 18 ns | 27 ns | 30 mW | 54LS151 | J,W | 74LS151 | N | 3-41 | 6-65 |
| | Standard | 9 ns | 16 ns | 17 ns | 135 mW | 9312 | J,W | 8312 | N | 7-150 | 7-151 |
| | Standard | 11 ns | 18 ns | 17 ns | 155 mW | 7121 | J,W | 8121 | N | 7-20 | 7-21 |
| 16-Line to 1-Line | Standard | 11 ns | N/A | 18 ns | 200 mW | 54150 | J,W | 74150 | N | 3-40 | 6-65 |
| | TRI-STATE | 11 ns | N/A | 21 ns | 225 mW | 7219 | J,W | 8219 | N | 7-37 | 7-38 |

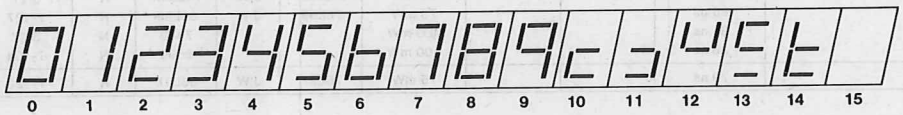
## Decoders/Demultiplexers

| Description | Type of Output | Typ. Select Time | Typ. Enable Time | Typ. Total Power Disipation | Device Type and Package: Mil. | | Device Type and Package: Coml. | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|---|
| Dual 2-Line to 4-Line | Totem-Pole | 7.5 ns | 6 ns | 300 mW | 54S139 | J,W | 74S139 | N | 3-38 | 6-55 |
| | Totem-Pole | 18 ns | 15 ns | 30 mW | 54LS155 | J,W | 74LS155 | N | 3-42 | 6-76 |
| | Totem-Pole | 21 ns | 16 ns | 250 mW | 54155 | J,W | 74155 | N | 3-42 | 6-76 |
| | Totem-Pole | 22 ns | 19 ns | 34 mW | 54LS139 | J,W | 74LS139 | N | 3-38 | 6-55 |
| | Open-Collector | 23 ns | 18 ns | 250 mW | 54156 | J,W | 74156 | N | 3-42 | 6-76 |
| | Open-Collector | 33 ns | 26 ns | 31 mW | 54LS156 | J,W | 74LS156 | N | 3-42 | 6-76 |
| 3-Line to 8-Line | Totem-Pole | 8 ns | 7 ns | 225 mW | 54S138 | J,W | 74S138 | N | 3-38 | 6-55 |
| | Totem-Pole | 22 ns | 21 ns | 31 mW | 54LS138 | J,W | 74LS138 | N | 3-38 | 6-55 |
| | Totem-Pole | 25 ns | N/A | 140 mW | 7223 | J,W | 8223 | N | 7-44 | 7-45 |
| 4-Line to 10-Line, BCD to Decimal | Totem-Pole | 17 ns | N/A | 35 mW | 54LS42 | J,W | 74LS42 | N | 3-12 | 6-8 |
| | Totem-Pole | 17 ns | N/A | 140 mW | 5442 | J,W | 7442 | N | 3-12 | 6-8 |
| | Totem-Pole | 20 ns | N/A | 125 mW | 9301 | J,W | 8301 | N | 7-148 | 7-149 |
| | Totem-Pole | 67 ns | N/A | 15 mW | 54L42A | J,W | 74L42A | N | 3-12 | 6-8 |
| 4-Line to 16-Line | Totem-Pole | 19.5 ns | 17.5 ns | 170 mW | 54154 | J,W | 74154 | N | 3-42 | 6-72 |
| | Totem-Pole | 19.5 ns | 17.5 ns | 170 mW | 9311 | J,W | 8311 | N | 7-161 | 7-162 |
| | Totem-Pole | 23 ns | 19 ns | 45 mW | 54LS154 | J,W | 74LS154 | N | 3-42 | 6-72 |
| | Totem-Pole | 55 ns | 45 ns | 24 mW | 54L154A | J,W | 74L154A | N | 3-42 | 6-72 |
| 1 of 10 Decoder | Totem-Pole | 19.5 ns | N/A | 125 mW | 9301 | J,W | 8301 | N | 7-148 | 7-149 |

## Display Decoders/Drivers

| Description | Output Sink Current | Off-State Output Voltage | Typ. Total Power Dissipation | Blanking | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Mil. | | Coml. | | | |
| BDC to 7-Segment Decoders/Drivers | 40 mA | 30 V | 320 mW | Ripple | 5446A | J,W | 7446A | N | 3-13 | 6-13 |
| | 40 mA | 15 V | 320 mW | Ripple | 5447A | J,W | 7447A | N | 3-13 | 6-13 |
| | 24 mA | 15 V | 35 mW | Ripple | | | 74LS47 | N | 3-13 | 6-13 |
| | 12 mA | 15 V | 35 mW | Ripple | 54LS47 | J,W | | | 3-13 | 6-13 |
| | 6.4 mA | 5.5 V | 265 mW | Ripple | 5448 | J,W | 7448 | N | 3-13 | 6-13 |
| | 8 mA | 5.5 V | 40 mW | Direct | | | 74LS49 | N | 3-14 | 6-13 |
| | 6 mA | 5.5 V | 125 mW | Ripple | | | 74LS48 | N | 3-13 | 6-13 |
| | 4 mA | 5.5 V | 40 mW | Direct | 54LS49 | J,W | | N | 3-14 | 6-13 |
| | 2 mA | 5.5 V | 125 mW | Ripple | 54LS48 | J,W | | | 3-13 | 6-13 |
| | 24 mA | 5.5 V | 35 mW | Ripple | | | 74LS247 | N | 3-56 | 6-188 |
| | 12 mA | 5.5 V | 35 mW | Ripple | 54LS247 | J,W | | | 3-56 | 6-188 |
| | 8 mA | 5.5 V | 40 mW | Direct | | | 74LS249 | N | 3-56 | 6-188 |
| | 6 mA | 5.5 V | 125 mW | Ripple | | | 74LS248 | N | 3-56 | 6-188 |
| | 4 mA | 5.5 V | 40 mW | Direct | 54LS249 | J,W | | | 3-56 | 6-188 |
| | 2 mA | 5.5 V | 125 mW | Ripple | 54LS248 | J,W | | | 3-56 | 6-188 |
| BCD to Decimal Decoders/Drivers | 80 mA | 30 V | 215 mW | Invalid Codes | 5445 | J,W | 7445 | N | 3-13 | 6-11 |
| | 80 mA | 15 V | 215 mW | Invalid Codes | 54145 | J,W | 74145 | N | 3-39 | 6-11 |
| | 7 mA | 60 V | 80 mW | Invalid Codes | 54141 | J,W | 74141 | N | 3-39 | 6-5 |
| | 16 mA | 5.5 V | 140 mW | Invalid Codes | 5442 | J,W | 7442 | N | 3-12 | 6-8 |
| 7-Segment to BCD Decoders/Drivers | 3.6 mA | 2.4 V | 75 mW | Direct | 76L25 | J,W | 86L25 | N | 7-111 | 7-112 |
| Nixie Driver | 7 mA | 70 V | 105 mW | None | 5441A | J,W | 7441A | N | 3-12 | 6-5 |

## Resultant Displays Using 46A, 47A, 48, LS47, LS48, LS49




## Latches

| Description | No. of Bits | Clear | Outputs | Typ. Delay Time | Typ. Total Power Dissipation | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Mil. | | Coml. | | | |
| Addressable Latches | 8 | Low | Q | 21 ns | 280 mW | 9334 | J,W | 8334 | N | 7-170 | 7-171 |
| | 8 | Low | Q | 21 ns | 150 mW | 54259 | J,W | 74259 | N | 3-58 | 6-202 |
| | 8 | Low | Q | 17 ns | 110 mW | 54LS259 | J,W | 74LS259 | N | 3-58 | 6-202 |
| DG (Clocked) Latches | 4 | None | Q, $\overline{Q}$ | 11 ns | 32mW | 54LS75 | J,W | 74LS75 | N | 3-23 | 6-19 |
| | 4 | None | Q | 10 ns | 35 mW | 54LS77 | J,W | 74LS77 | N | 3-24 | 6-19 |
| | 4 | None | Q, $\overline{Q}$ | 15 ns | 160 mW | 5475 | J,W | 7475 | N | 3-23 | 6-19 |
| | 4 | None | Q, $\overline{Q}$ | 52 ns | 17.5 mW | 54L75A | J,W | 74L75A | N | 3-23 | 6-19 |
| $\overline{S}$-$\overline{R}$ Latches | 4 | None | Q | 12 ns | 19 mW | 54LS279 | J,W | 74LS279 | N | 3-59 | 5-63 |
| | 4 | None | Q | 19 ns | 180 mW | 7544 | J,W | 8544 | N | 7-59 | 7-60 |
| TRI-STATE® Counters/Latches | 4 | High | Q | 28 ns | 330 mW | 7552 | J,W | 8552 | N | 7-71 | 7-72 |
| | 4 | High | Q | 95 ns | 38 mW | 75L52 | J,W | 85L52 | N | 7-71 | 7-72 |
| | 4 | High | Q | 28 ns | 330 mW | 7554 | J,W | 8554 | N | 7-71 | 7-72 |
| | 4 | High | Q | 95 ns | 38 mW | 75L54 | J,W | 85L54 | N | 7-71 | 7-72 |
| | 8 | High | Q | 21 ns | 330 mW | 7553 | J,W | 8553 | N | 7-79 | 7-80 |
| TRI-STATE OCTAL | 8 | None | Q | 12 ns | 525 mW | 54S373 | J,W | 74S373 | N | 3-64 | 6-227 |
| | 8 | None | Q | 17 ns | 120 mW | 54LS373 | J,W | 74LS373 | N | 3-64 | 6-227 |

## Multipliers

| Description | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|
| | Mil. | | Coml. | | | |
| 4-Bit by 4-Bit Parallel Binary Multipliers | 7875A | J,W | 8875A | N | 7-133 | 7-134 |
| | 7875B | J,W | 8875B | N | 7-133 | 7-134 |

## Parity Generators/Checkers

| Description | Typ Delay Time | Typ. Total Power Dissipation | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|
| | | | Mil. | | Coml. | | | |
| 8-Bit Odd/Even Parity Generators/Checkers | 35 ns | 170 mW | 54180 | J,W | 74180 | N | 3-48 | 6-133 |
| 9-Bit Odd/Even Parity Generators/Checkers | 13 ns<br>34 ns | 335 mW<br>130 mW | 54S280<br>7220 | J,W<br>J,W | 74S280<br>8220 | N<br>N | 3-59<br>7-41 | 6-205<br>7-42 |

## Priority Encoders

| Description | Typ. Propagation Delay Time | Typ.Total Power Dissipation | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|
| | | | Mil. | | Coml. | | | |
| Cascadable Octal Priority Encoders | 12 ns<br>12 ns | 190 mW<br>190 mW | 54148<br>9318 | J,W<br>J,W | 74148<br>8318 | N<br>N | 3-40<br>7-164 | 6-59<br>7-165 |
| Full BCD Priority Encoders | 10 ns | 225 mW | 54147 | J,W | 74147 | N | 3-140 | 6-59 |

## Register Files

| Description | Typ. Address Time | Typ. Read Enable Time | Data Input Rate | Typ. Total Power Dissipation | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Mil. | | Coml. | | | |
| 4 Words of 4-Bits | 27 ns<br>30 ns | 15 ns<br>15 ns | 20 MHz<br>20 MHz | 125 mW<br>635 mW | 54LS170 | J,W | 74LS170<br>74170 | N<br>N | 3-46<br>3-46 | 6-114<br>6-114 |
| 4 Words of 4-Bits (TRI-STATE® Outputs) | 24 ns<br>24 ns | 19 ns<br>19 ns | 20 MHz<br>30 MHz | 135 mW<br>400 mW | 54LS670<br>7542 | J,W<br>J,W | 74LS670<br>8542 | N<br>N | 3-66<br>7-56 | 6-241<br>7-57 |
| 64-Bit RAM | 110 ns<br>80 ns<br>35 ns<br>28 ns | | | 75 mW<br>75 mW<br>400 mW<br>400 mW | 54L89A<br>76L99 | J,W<br>J,W | 74L89A<br>86L99<br>7489<br>8599 | N<br>N<br>N<br>N | 3-27<br>7-127<br>3-27<br>7-104 | 6-34<br>7-128<br>6-34<br>7-105 |
| 1024-Bit ROM | 70 ns | | | 75 mW | 76L97 | J,W | 86L97 | N | 7-123 | 7-124 |

## Registers, Other

| Description | Freq. | Async. Clear | Typ. Total Power Dissipation | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Mil. | | Coml. | | | |
| Quad Bus Buffer Registers | 30 MHz<br>25 MHz<br>25 MHz<br>6 MHz | High<br>High<br>High<br>High | 85 mW<br>250 mW<br>250 mW<br>28 mW | 54LS173<br>54173<br>7551<br>75L51 | J,W<br>J,W<br>J,W<br>J,W | 74LS173<br>74173<br>8551<br>85L51 | N<br>N<br>N<br>N | 3-46<br>3-46<br>7-67<br>7-67 | 6-120<br>6-120<br>7-69<br>7-69 |
| Quad D-Type Registers | 75 MHz<br>30 MHz<br>25 MHz | Low<br>Low<br>Low | 300 mW<br>55 mW<br>150 mW | 54S175<br>54LS175<br>54175 | J,W<br>J,W<br>J,W | 74S175<br>74LS175<br>74175 | N<br>N<br>N | 3-47<br>3-47<br>3-47 | 6-123<br>6-123<br>6-123 |
| Quad Multiplexers With Storage | 25 MHz<br>6 MHz | None<br>None | 65 mW<br>30 mW | 54LS298<br>54L98 | J,W<br>J,W | 74LS298<br>74L98 | N<br>N | 3-61<br>3-68 | 6-212<br>6-52 |
| Hex D-Type Registers | 75 MHz<br>30 MHz<br>25 MHz | Low<br>Low<br>Low | 450 mW<br>80 mW<br>225 mW | 54S174<br>54LS174<br>54174 | J,W<br>J,W<br>J,W | 74S174<br>74LS174<br>74174 | N<br>N<br>N | 3-47<br>3-47<br>3-47 | 6-123<br>6-123<br>6-123 |
| 8-Bit Universal Shift/Storage Registers | 15 MHz<br>50 MHz | None<br>Low | 400 mW<br>700 mW | 7546<br>54S299 | J,W<br>J,W | 8546<br>74S299 | N<br>N | 7-61<br>3-61 | 7-62<br>6-217 |
| Octal D-Type Registers | 35 MHz<br>75 MHz | None<br>None | 135 mW<br>450 mW | 54LS374<br>54S374 | J,W<br>J,W | 74LS374<br>74S374 | N<br>N | 3-64<br>3-64 | 6-227<br>6-227 |
| 8-Bit Dual Rank S/R | 25 MHz<br>25 MHz | None<br>None | 305 mW<br>305 mW | 54LS962<br>54LS952 | J,W<br>J,W | 74LS962<br>74LS952 | N<br>N | 3-68<br>3-68 | 6-244<br>6-244 |
| Successive Approximation Registers | 15 MHz<br>15 MHz<br>15 MHz | None<br>None<br>None | 325 mW<br>300 mW<br>450 mW | 2502<br>2503<br>2504 | J,W<br>J,W<br>J,W | 2502C<br>2503C<br>2504C | N<br>N<br>N | 7-3<br>7-3<br>7-3 | 7-7<br>7-7<br>7-7 |

## Registers, Shift

| Description | No. of Bits | Shift Freq. | Serial Data Input | Async. Clear | Modes | | | | Typ. Total Power Dissipation | Device Type and Package | | | | Connection Diagram Page No. | Electrical Tables Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | S-R* | S-L* | Load | Hold | | Mil. | | Coml. | | | |
| Parallel-In, Parallel-Out (Bidirectional) | 8 | 25 MHz | D | Low | X | X | X | X | 360 mW | 54198 | J,W | 74198 | N | 3-53 | 6-179 |
| | 4 | 70 MHz | D | Low | X | X | X | X | 450 mW | 54S194 | J,W | 74S194 | N | 3-51 | 6-170 |
| | 4 | 25 MHz | D | Low | X | X | X | X | 75 mW | 54LS194A | J,W | 74LS194A | N | 3-51 | 6-170 |
| | 4 | 25 MHz | D | Low | X | X | X | X | 195 mW | 54194 | J,W | 74194 | N | 3-51 | 6-170 |
| Parallel-In, Parallel-Out | 8 | 25 MHz | J-$\overline{K}$ | Low | X | | X | X | 360 mW | 54199 | J,W | 74199 | N | 3-53 | 6-179 |
| | 5 | 10 MHz | D | Low | X | | X | | 240 mW | 5496 | J,W | 7496 | N | 3-30 | 6-48 |
| | 5 | 10 MHz | J-$\overline{K}$ | Low | X | | X | | 375 mW | 54S195 | J,W | 74S195 | N | 3-52 | 6-175 |
| | 4 | 30 MHz | J-$\overline{K}$ | Low | X | | X | | 195 mW | 54195 | J,W | 74195 | N | 3-52 | 6-175 |
| | 4 | 30 MHz | J-$\overline{K}$ | Low | X | | X | | 300 mW | 9300 | J,W | 8300 | N | 7-145 | 7-146 |
| | 4 | 30 MHz | J-$\overline{K}$ | Low | X | | X | | 70 mW | 54LS195A | J,W | 74LS195A | N | 3-52 | 6-175 |
| | 4 | 25 MHz | D | None | X | | X | | 195 mW | 5495 | J,W | 7495 | N | 3-30 | 6-45 |
| | 4 | 6 MHz | D | None | X | | X | | 24 mW | 54L95 | J,W | 74L95 | N | 3-30 | 6-45 |
| Serial-In, Parallel-Out | 8 | 25 MHz | Gated D | Low | X | | | | 80 mW | 54LS164 | J,W | 74LS164 | N | 3-44 | 6-96 |
| | 8 | 25 MHz | Gated D | Low | X | | | | 175 mW | 54164 | J,W | 74164 | N | 3-44 | 6-96 |
| | 8 | 25 MHz | Gated D | Low | X | | | | 175 mW | 7570 | J,W | 8570 | N | 7-96 | 7-97 |
| | 8 | 6 MHz | Gated D | Low | X | | | | 30 mW | 54L164A | J,W | 74L164A | N | 3-44 | 6-96 |
| | 8 | 6 MHz | Gated D | Low | X | | | | 30 mW | 76L70 | J,W | 86L70 | N | 7-96 | 7-97 |
| Parallel-In, Serial Out | 8 | 25 MHz | D | None | X | | X | X | 200 mW | 54165 | J,W | 74165 | N | 3-44 | 6-99 |
| | 8 | 25 MHz | D | None | X | | X | X | 125 mW | 54LS165 | J,W | 74LS165 | N | 3-44 | 6-99 |
| | 8 | 25 MHz | D | Low | X | | X | X | 110 mW | 54LS166 | J,W | 74LS166 | N | 3-45 | 6-103 |
| | 8 | 20 MHz | D | Low | X | | X | X | 360 mW | 54166 | J,W | 74166 | N | 3-45 | 6-103 |
| | 8 | 14 MHz | D | None | X | | X | X | 200 mW | 7590 | J,W | 8590 | N | 7-99 | 7-101 |
| | 8 | 6 MHz | D | None | X | | X | X | 30 mW | 54L165A | J,W | 74L165A | N | 3-44 | 6-99 |
| | 8 | 6 MHz | D | None | X | | X | X | 30 mW | 76L90 | J,W | 86L90 | N | 7-99 | 7-99 |
| Serial-Out | 8 | 4 MHz | Gated D | None | X | | | | 17.5 mW | 54L91 | J,W | 74L91 | N | 3-28 | 6-43 |

*S-R ≡ shift right, S-L ≡ shift left.

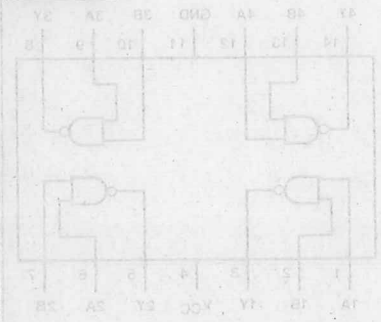
Registers Shift

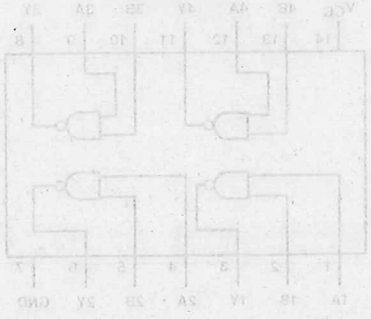
| Description | No. of Bits | Shift Freq. | Shift Data Input | Async. Clear | Modes S-R* | S-L* | Load | Hold | Typ. Total Power Dissipation | Device Type and Package MIL | Comm'l | Connection Diagram Page No. | Electrical Values Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parallel-In, | 8 | 25 MHz | D | Low | X | X | X | | 260 mW | 54/74S | 74S | 3-52 | 6-173 |
| Parallel-Out | 4 | 70 MHz | D | Low | X | X | X | | 400 mW | 54/74H | H | 3-51 | 6-170 |
| (Bidirectional) | 4 | 25 MHz | D | Low | X | X | X | | 75 mW | 74LS194A | LS | 3-51 | 6-170 |
| | 4 | 25 MHz | D | Low | X | X | X | | 195 mW | 54/74H | H | 3-51 | 6-170 |
| Parallel-In, | 8 | 25 MHz | J-K | Low | X | | X | X | 360 mW | 54/74S | S | 3-52 | 6-173 |
| Parallel-Out | 8 | 10 MHz | D | Low | X | | X | | 240 mW | 74C | H | 3-50 | 6-168 |
| | 5 | 10 MHz | J-K | Low | X | | X | | 315 mW | 54/74S | S | 3-52 | 6-173 |
| | 4 | 30 MHz | J-K | Low | X | | X | | 180 mW | 74S | H | 3-52 | 6-173 |
| | 4 | 20 MHz | J-K | Low | X | | X | | 200 mW | 54/74 | H | 3-49 | 6-165 |
| | 4 | 30 MHz | J-K | Low | X | | X | | 70 mW | 74LS | H | 3-51 | 6-170 |
| | 4 | 25 MHz | D | Low | X | | X | | 225 mW | 74 | H | 3-49 | 6-165 |
| | 4 | 5 MHz | D | Low | X | | X | | 25 mW | 74C | H | 3-50 | 6-168 |
| Serial-In, | 8 | 25 MHz | Gated D | Low | X | | | | 90 mW | 74LS | H | 3-54 | 6-182 |
| Parallel-Out | 8 | 25 MHz | Gated D | Low | X | | | | 225 mW | 74 | H | 3-54 | 6-182 |
| | 8 | 25 MHz | Gated D | Low | X | | | | 225 mW | 74S | H | 3-54 | 6-182 |
| | 8 | 5 MHz | Gated D | Low | X | | | | 30 mW | 74C | H | 3-54 | 6-182 |
| Parallel-In, | 8 | 25 MHz | D | None | X | | X | X | 300 mW | 74S | H | 3-54 | 6-182 |
| Serial Out | 8 | 25 MHz | D | None | X | | X | X | 225 mW | 74LS | H | 3-54 | 6-182 |
| | 8 | 25 MHz | D | Low | X | | X | X | 110 mW | 74LS | H | 3-53 | 6-179 |
| | 8 | 20 MHz | D | Low | X | | X | X | 280 mW | 74 | H | 3-48 | 6-163 |
| | 8 | 14 MHz | D | None | X | | X | X | 220 mW | 4035 | H | 3-55 | 7-101 |
| | 8 | 8 MHz | D | None | X | | X | X | 30 mW | 74L | H | 3-54 | 6-182 |
| Serial-Out | 8 | 5 MHz | D | None | X | | X | X | 30 mW | 74L | H | 3-54 | 6-182 |

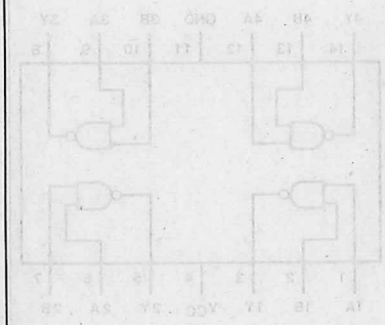
*S-R = shift right, S-L = shift left.

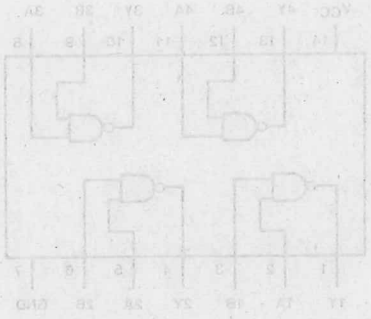
# Section 3
# Connection Diagrams

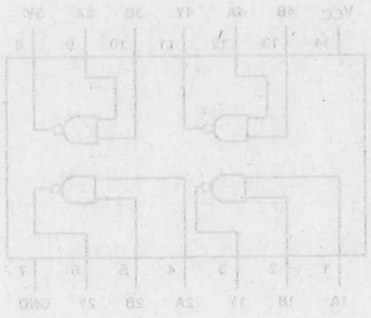
3







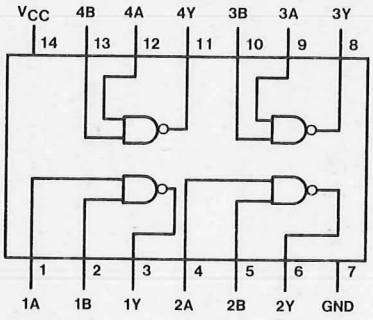




3

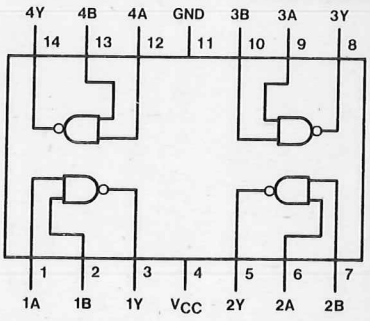
## 00 Quad 2-Input NAND Gates

$Y = \overline{AB}$




5400 (J)
54H00 (J)
54L00 (J,W)
54LS00 (J,W)
54S00 (J,W)

7400 (N)
74H00 (N)
74L00 (N)
74LS00 (N)
74S00 (N)

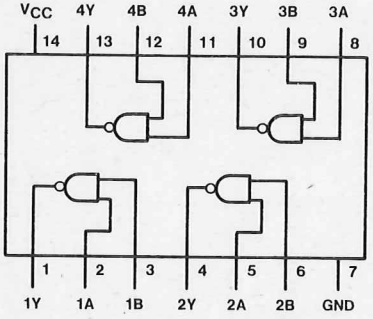



5400 (W)
54L00 (W)

See page 5-4

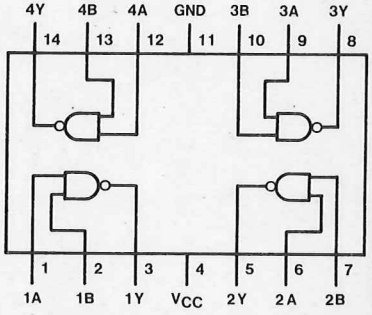
## 01 Quad 2-Input NAND Gates with Open-Collector Outputs

$Y = \overline{AB}$

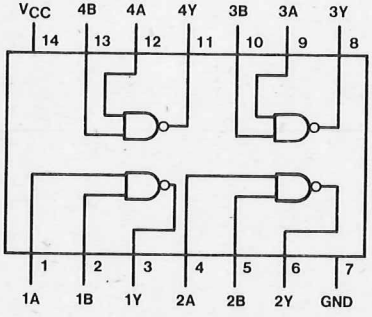



5401 (J)
54LS01 (J,W)

7401 (N)
74LS01 (N)




5401 (W)
54L01 (W)

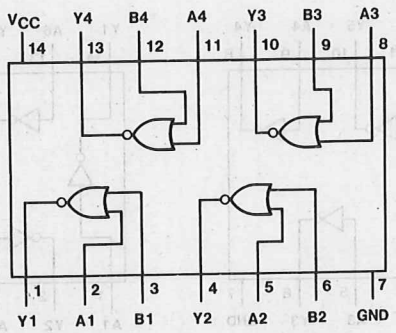


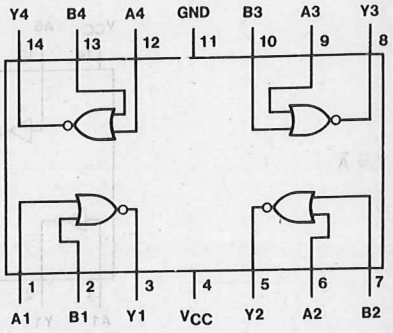

54H01 (J); 74H01 (N)

See page 5-6

## 02 Quad 2-Input NOR Gates

$Y = \overline{A + B}$




5402 (J)
54L02 (J)
54LS02 (J,W)
54S02 (J,W)

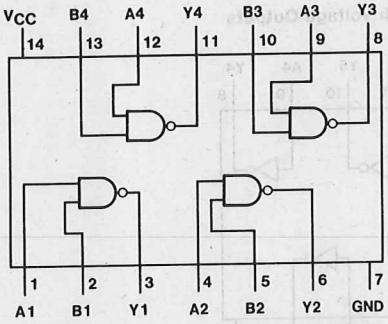
7402 (N)
74L02 (N)
74LS02 (N)
74S02 (N)

5402 (W)
54L02 (W)

See page 5-8

## 03 Quad 2-Input NAND Gates with Open-Collector Outputs

$Y = \overline{AB}$



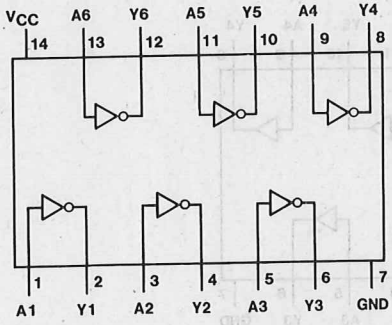

5403 (J)
54L03 (J)
54LS03 (J,W)
54S03 (J,W)

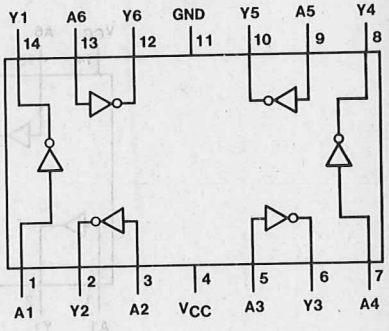
7403 (N)
74L03 (N)
74LS03 (N)
74S03 (N)

See page 5-6

## 04 Hex Inverters

$Y = \overline{A}$




5404 (J)
54H04 (J)
54L04 (J)
54LS04 (J,W)
54S04 (J,W)

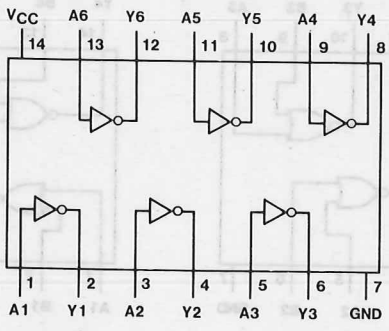
7404 (N)
74H04 (N)
74L04 (N)
74LS04 (N)
74S04 (N)

5404 (W)
54L04 (W)

See page 5-4

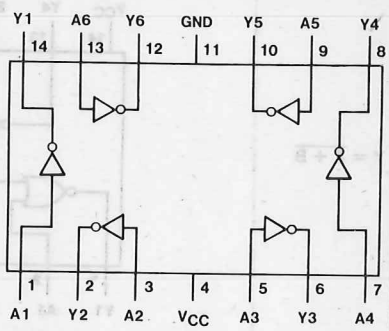
## 05 Hex Inverters with Open-Collector Outputs

$Y = \overline{A}$




5405 (J)
54L05 (J)
54LS05 (J,W)
54S05 (J,W)

7405 (N)
74L05 (N)
74LS05 (N)
74S05 (N)

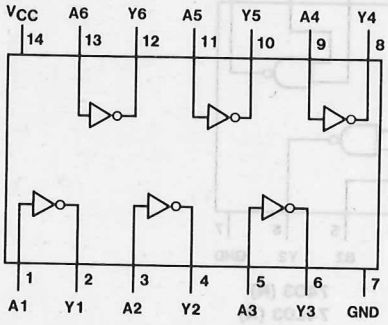



5405 (W)
54L05 (W)

See page 5-6

## 06 Hex Inverter Buffers with Open-Collector High Voltage Outputs

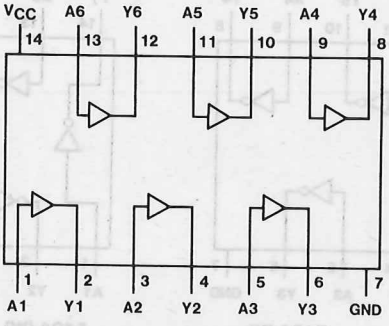
$Y = \overline{A}$




5406 (J,W); 7406 (N)

See page 5-10

## 07 Hex Buffers with Open-Collector High Voltage Outputs

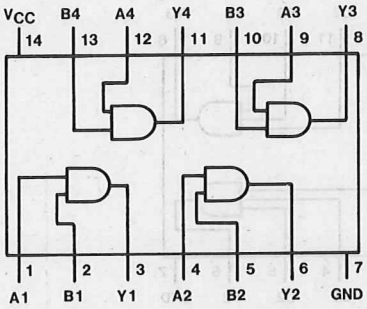



5407 (J,W); 7407 (N)

See page 5-10

## 08 Quad 2-Input AND Gates

$Y = AB$



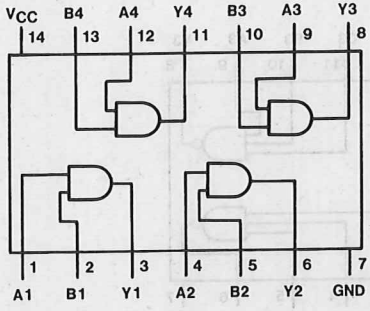

5408 (J,W)
54H08 (J)
54L08 (J,W)
54LS08 (J,W)
54S08 (J,W)

7408 (N)
74H08 (N)
74L08 (N)
74LS08 (N)
74S08 (N)

See page 5-12

## 09 Quad 2-Input AND Gates with Open-Collector Outputs

$Y = AB$



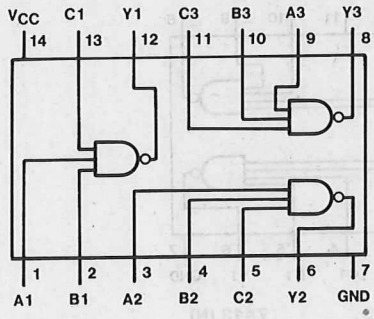

5409 (J,W)
54L09 (J,W)
54LS09 (J,W)
54S09 (J,W)

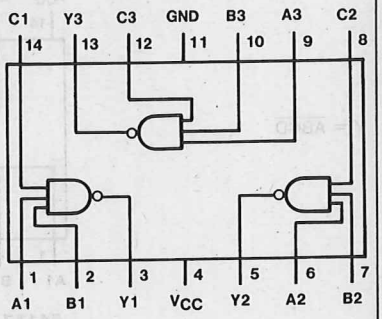
7409 (N)
74L09 (N)
74LS09 (N)
74S09 (N)

See page 5-14

## 10 Triple 3-Input NAND Gates

$Y = \overline{ABC}$




5410 (J)
54H10 (J)
54L10 (J)
54LS10 (J,W)
54S10 (J,W)

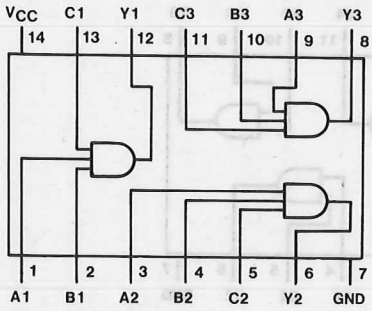
7410 (N)
74H10 (N)
74L10 (N)
74LS10 (N)
74S10 (N)

5410 (W)
54L10 (W)

See page 5-4

## 11 Triple 3-Input AND Gates

$Y = ABC$



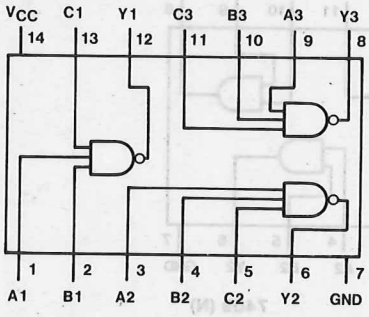

**5411 (J)**
**54H11 (J)**
**54L11 (J)**
**54LS11 (J,W)**
**54S11 (J,W)**

**7411 (N)**
**74H11 (N)**
**74L11 (N)**
**74LS11 (N)**
**74S11 (N)**

See page 5-12

## 12 Triple 3-Input NAND Gates with Open-Collector Outputs

$Y = \overline{ABC}$

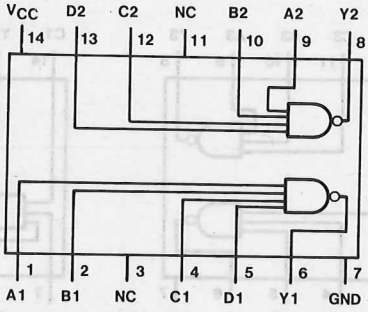



**54LS12 (J,W); 74LS12 (N)**

See page 5-6

## 13 Dual 4-Input NAND Schmitt Triggers

$Y = \overline{ABCD}$



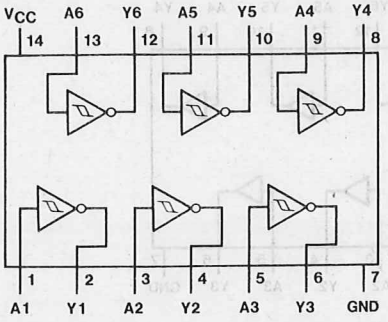

**5413 (J,W)**
**54LS13 (J,W)**

**7413 (N)**
**74LS13 (N)**

See page 5-16

## 14 Hex Schmitt Triggers

$Y = \overline{A}$

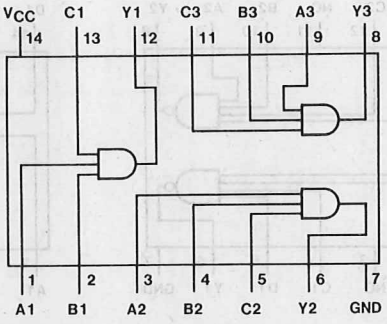



**5414 (J,W)** **7414 (N)**
**54LS14 (J,W)** **74LS14 (N)**

See page 5-16

## 15 Triple 3-Input AND Gates with Open-Collector Outputs

$Y = ABC$

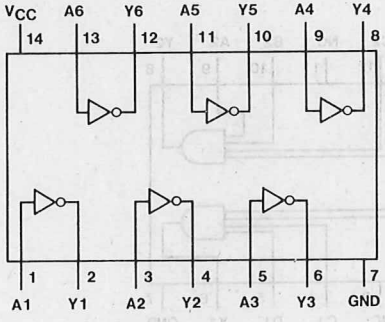



**54LS15 (J,W)** **74LS15 (N)**
**54S15 (J,W)** **74S15 (N)**

See page 5-14

## 16 Hex Inverter Buffers with Open-Collector High-Voltage Outputs

$Y = \overline{A}$

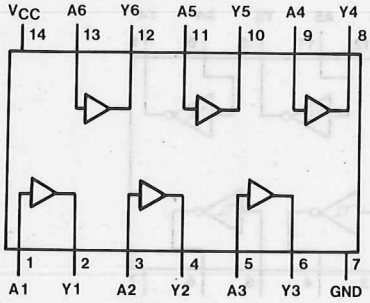



**5416 (J,W); 7416 (N)**

See page 5-10

## 17 Hex Buffers with Open-Collector High-Voltage Outputs

$Y = A$

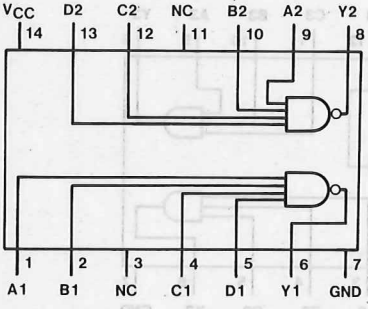


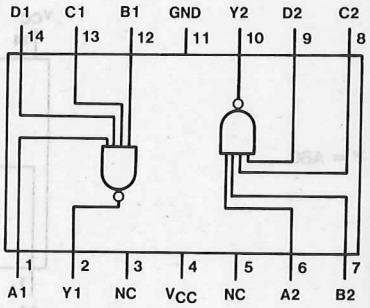

**5417 (J,W); 7417 (N)**

See page 5-10

## 20 Dual 4-Input NAND Gates

$Y = \overline{ABCD}$




**5420 (J)**
**54H20 (J)**
**54L20 (J)**
**54LS20 (J,W)**
**54S20 (J,W)**

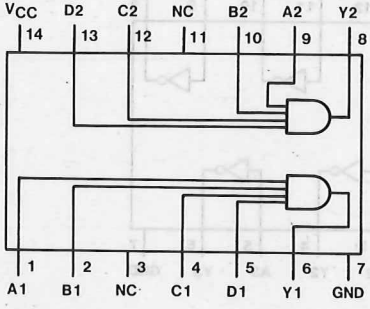
**7420 (N)**
**74H20 (N)**
**74L20 (N)**
**74LS20 (N)**
**74S20 (N)**

**5420 (W)**
**54L20 (W)**

See page 5-4

## 21 Dual 4-Input AND Gates

$Y = ABCD$



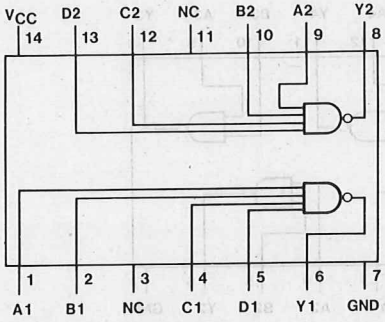

**54H21 (J)**
**54LS21 (J,W)**

**74H21 (N)**
**74LS21 (N)**

See page 5-12

## 22 Dual 4-Input NAND Gates with Open Collector Outputs

$Y = \overline{ABCD}$

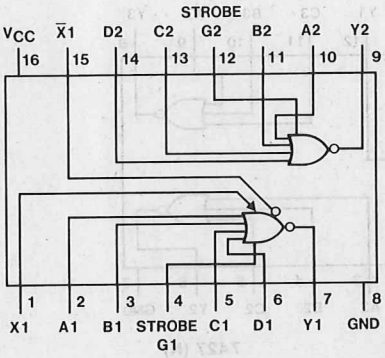



**54LS22 (J,W)** **74LS22 (N)**
**54S22 (J,W)** **74S22 (N)**

See page 5-6

## 23 Expandable Dual 4-Input NOR Gates with Strobe

$Y1 = \overline{G1\ (A1+B1+C1+D1)+X}$
$Y2 = \overline{G2\ (A2+B2+C2+D2)}$
X = output of 5460/7460

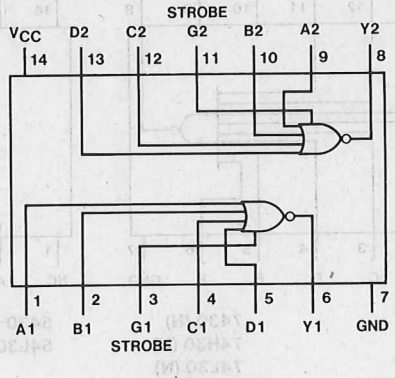



**5423 (J,W); 7423 (N)**

See page 5-18

## 25 Dual 4-Input NOR Gates with Strobe

$Y = \overline{G(A+B+C+D)}$

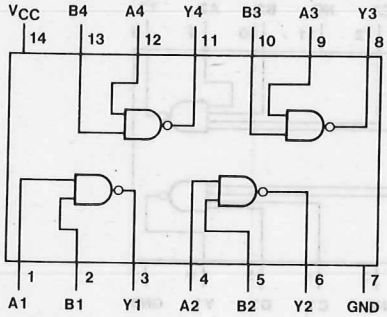



**5425 (J,W); 7425 (N)**

See page 5-8

## 26 Quad 2-Input High-Voltage NAND Gates

$Y = \overline{AB}$



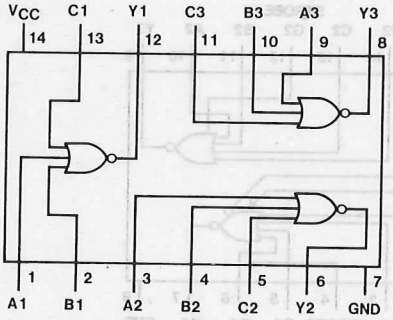

**5426 (J)**
**54L26 (J)**
**54LS26 (J,W)**

**7426 (N)**
**74L26 (N)**
**74LS26 (N)**

See page 5-10

## 27 Triple 3-Input NOR Gates

$Y = \overline{A+B+C}$



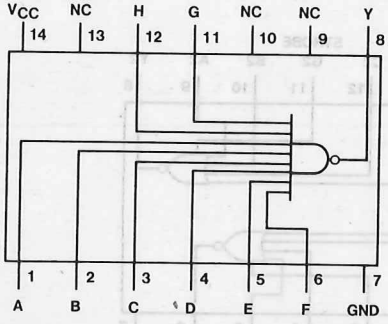

**5427 (J,W)**
**54LS27 (J,W)**

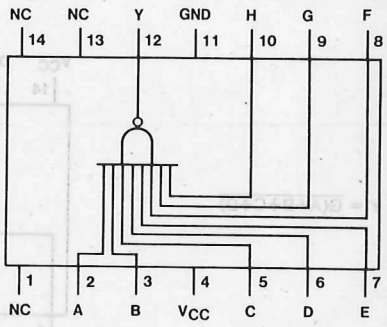
**7427 (N)**
**74LS27 (N)**

See page 5-8

## 30 8-Input NAND Gates

$Y = \overline{ABCDEFGH}$




**5430 (J)**
**54H30 (J)**
**54L30 (J)**
**54LS30 (J,W)**
**54S30 (J,W)**

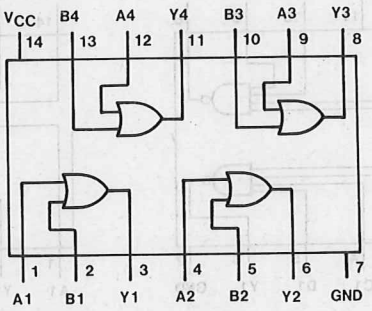
**7430 (N)**
**74H30 (N)**
**74L30 (N)**
**74LS30 (N)**
**74S30 (N)**

**5430 (W)**
**54L30 (W)**

See page 5-4

## 32 Quad 2-Input OR Gates

$Y = A + B$



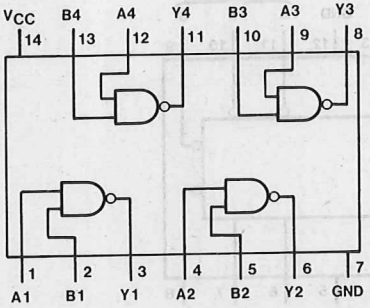

**5432 (J,W)**
**54L32 (J,W)**
**54LS32 (J,W)**
**54S32 (J,W)**

**7432 (N)**
**74L32 (N)**
**74LS32 (N)**
**74S32 (N)**

See page 5-20

## 37 Quad 2-Input NAND Buffers

$Y = \overline{AB}$



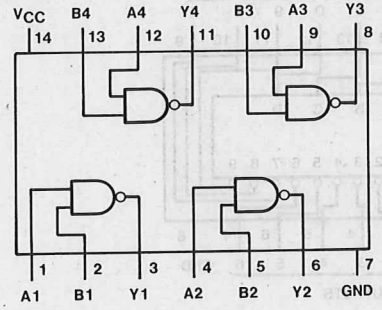

**5437 (J,W)**
**54LS37 (J,W)**

**7437 (N)**
**74LS37 (N)**

See page 5-22

## 38 Quad 2-Input NAND Buffers with Open-Collector Outputs

$Y = \overline{AB}$



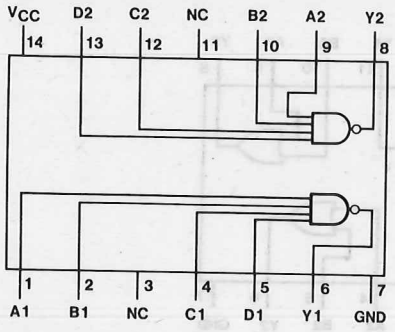

**5438 (J,W)**
**54LS38 (J,W)**

**7438 (N)**
**74LS38 (N)**

See page 5-10

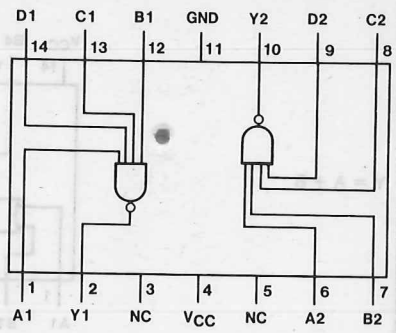
## 40 Dual 4-Input NAND Buffers

$Y = \overline{ABCD}$




5440 (J)
54H40 (J)
54LS40 (J,W)
54S40 (J,W)

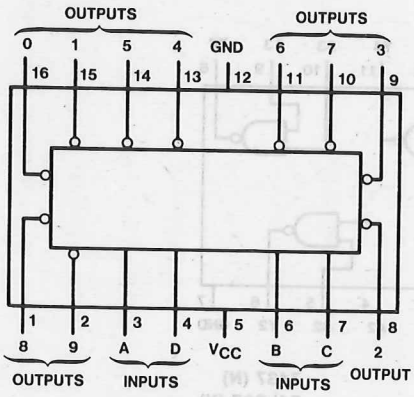
7440 (N)
74H40 (N)
74LS40 (N)
74S40 (N)




5440 (W)

See page 5-22

## 41 Nixie Driver

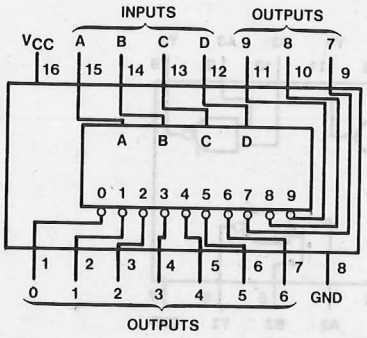



5441A (J,W); 7441A (N)

See page 6-4

### 4 Line-to-10-Line Decoder

## 42 BCD-to-Decimal



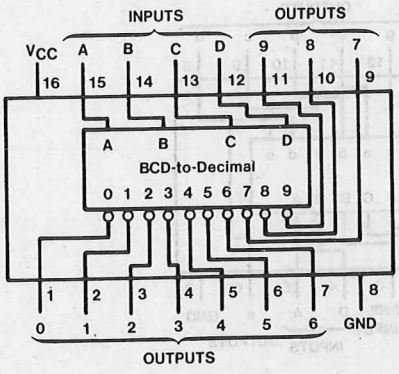

5442A (J,W)
54L42A (J,W)
54LS42 (J,W)

7442A (N)
74L42A (N)
74LS42 (N)

See page 6-7

## BCD-to-Decimal Decoder/Driver

**45** Lamp, Relay, or MOS Driver
80-mA Current Sink
Outputs Off for Invalid Codes



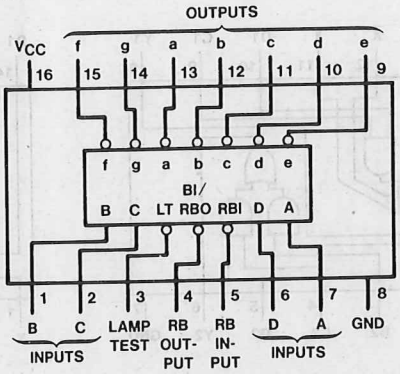

5445 (J,W); 7445 (N)

See page 6-10

## BCD-to-Seven-Segment Decoders/Drivers

**46** Active-Low, Open-Collector, 30-V Outputs

**47** Active-Low, Open-Collector, 15-V Outputs



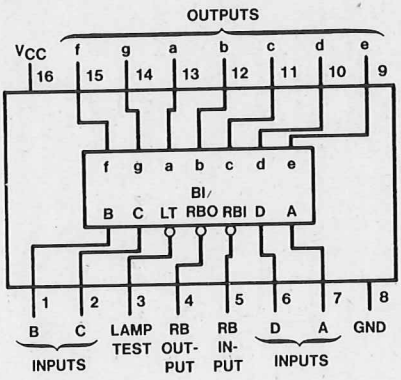

5446A (J,W)
5447 (J,W)
54LS47 (J,W)

7446A (N)
7447A (N)
74LS47 (N)

See page 6-12

## BCD-to-Seven-Segment Decoders/Drivers

**48** Internal Pull-Up Outputs



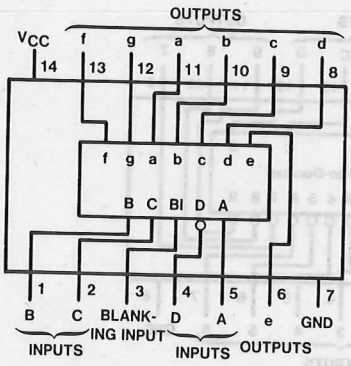

5448 (J,W)
54LS48 (J,W)

7448 (N)
74LS48 (N)

See page 6-12

BCD-to-Seven-Segment Decoders/Drivers

## 49 Open-Collector Outputs



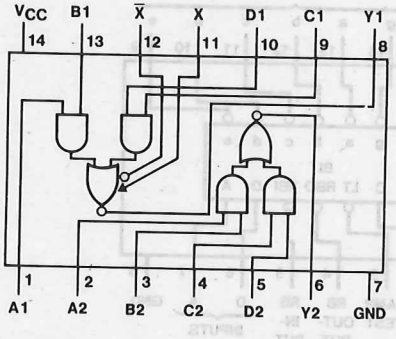

See page 6-12

54LS49 (J,W); 74LS49 (N)

## 50 Dual 2-Wide, 2-Input, AND-OR-INVERT Gates

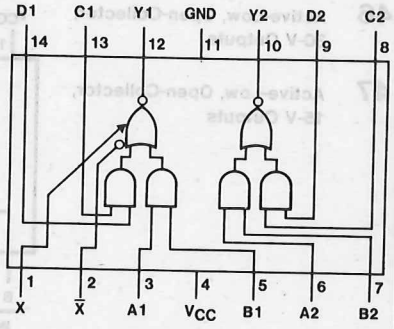
$Y = \overline{AB+CD+X}$

50: X = output of 5460/7460




5450 (J)
54H50 (J)

7450 (N)
74H50 (N)

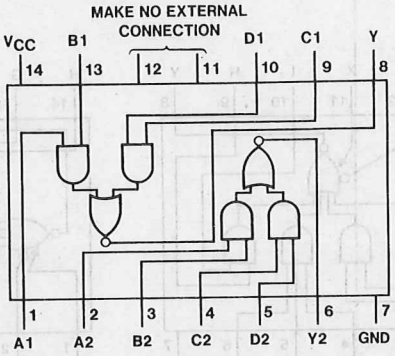



5450 (W)

See page 5-18

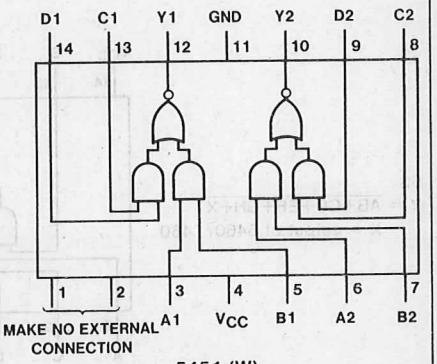
## 51 Dual 2-Wide, 2-Input AND-OR-INVERT Gates

51, S51
$Y = \overline{AB+CD}$



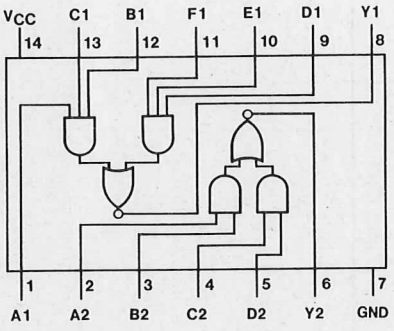

5451 (J)
54S51 (J,W)

7451 (N)
74S51 (N)



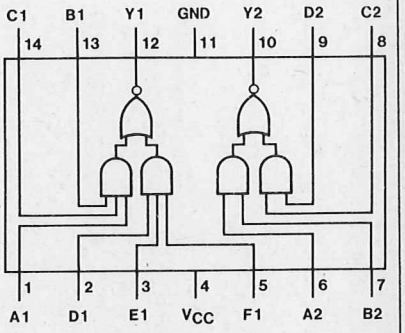

5451 (W)

L51, LS51
$Y1 = \overline{(A1xB1xC1) + (D1xE1xF1)}$
$Y2 = \overline{(A2xB2) + (C2xD2)}$




54L51 (J)
54LS51 (J,W)

74L51 (N)
74LS51 (N)




54L51 (W)

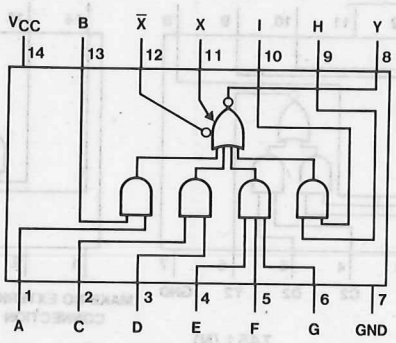
See page 5-24

## 53 Expandable 4-Wide AND-OR-INVERT Gates

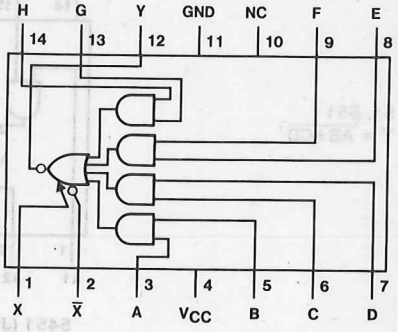
53

$Y = \overline{AB+CD+EF+GH+X}$

X = output of 5460/7460




5453 (J); 7453 (N)

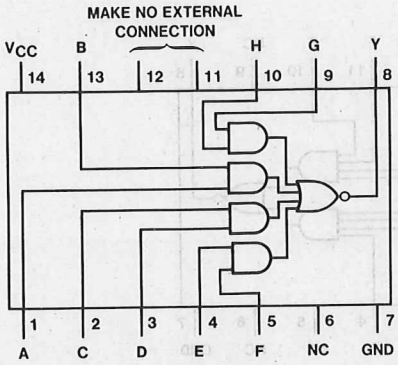



5453 (W)

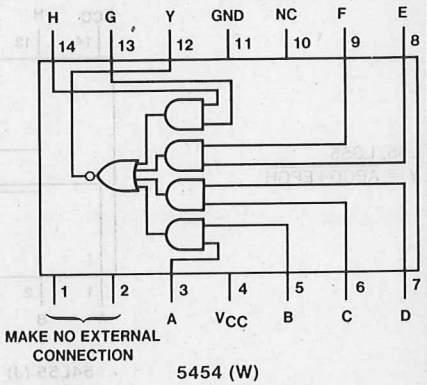
See page 5-18

## 54 4-Wide AND-OR-INVERT Gates

54
$Y = \overline{AB+CD+EF+GH}$

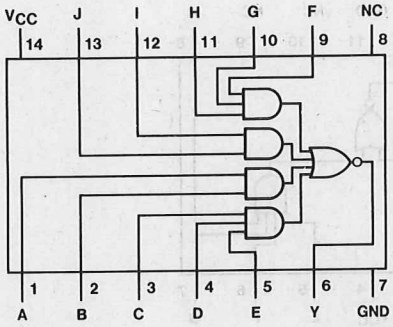



5454 (J); 7454 (N)




5454 (W)

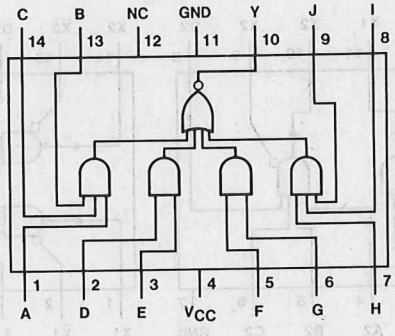
L54, LS54
$Y = \overline{AB+CDE+FGH+IJ}$




54L54 (J)
54LS54 (J,W)

74L54 (N)
74LS54 (N)

L54
$Y = \overline{ABC+DE+FG+HIJ}$

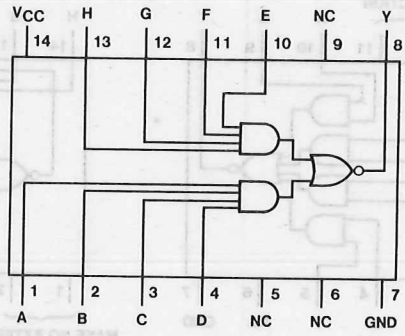



54L54 (W)

See page 5-24

## 55 2-Wide, 4-Input AND-OR-INVERT Gates

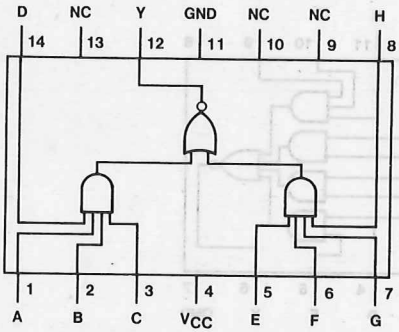
L55, LS55
$Y = \overline{ABCD+EFGH}$




54L55 (J)
54LS55 (J,W)

74L55 (N)
74LS55 (N)

L55
$Y = \overline{ABCD+EFGH}$

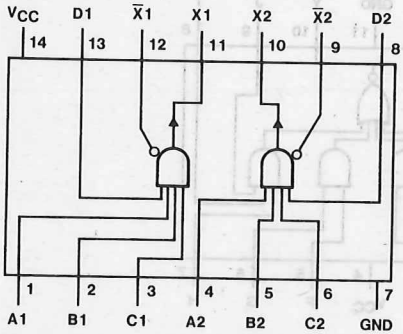



54L55 (W)

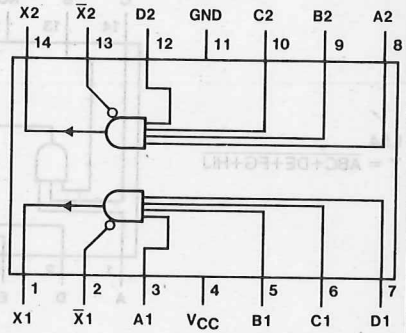
See page 5-24

## 60 Dual 4-Input Expanders

X = ABCD when connected to X and $\overline{X}$ inputs of 5423/7423, 5450/7450 or 5453/7453




5460 (J); 7460 (N)

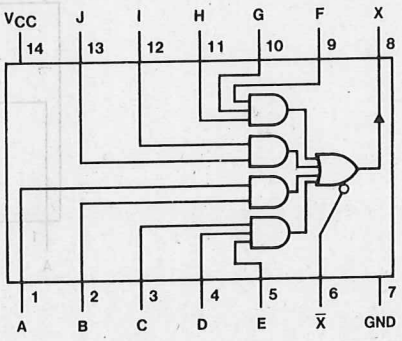



5460 (W)

See page 5-26

## 62 4-Wide AND-OR Expander

$X = AB+CDE+FGH+IJ$ when connected to X and $\overline{X}$ inputs of 54H50/74H50

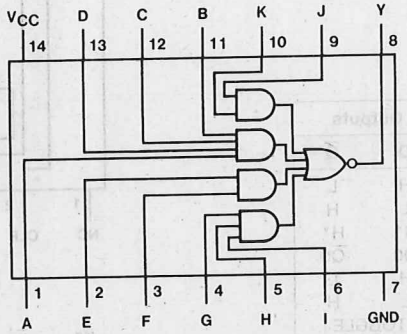



54H62 (J); 74H62 (N)

See page 5-27

## 64 4-Wide AND-OR-INVERT Gates

$Y = \overline{ABCD+EF+GHI+JK}$

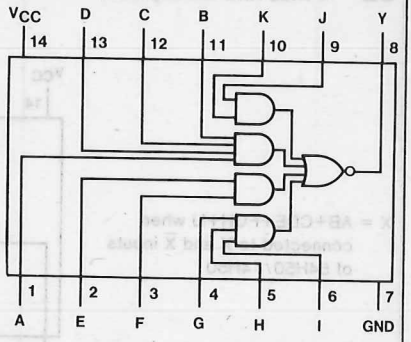



54S64 (J,W); 74S64 (N)

See page 5-24

## 65 4-Wide AND-OR-INVERT Gates with Open-Collector Outputs

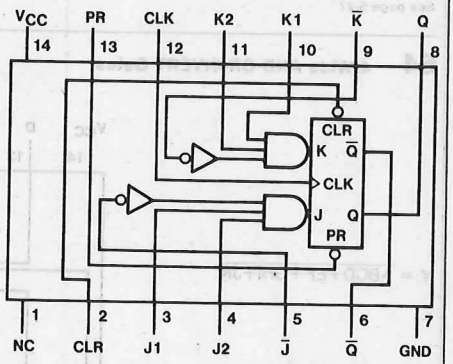
$Y = \overline{ABCD+EF+GHI+JK}$



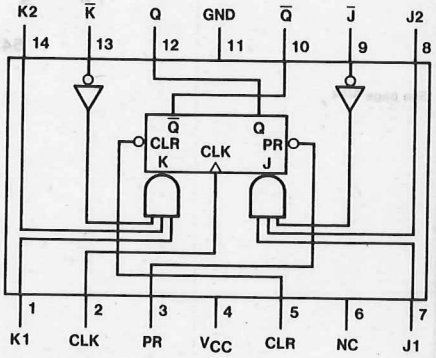

54S65 (J,W); 74S65 (N)

See page 5-28

## 70 AND-Gated J-K Positive-Edge-Triggered Flip-Flops with Preset and Clear




5470 (J); 7470 (N)




5470 (W)

### Truth Table

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| PR | CLR | CLK | J | K | Q | $\overline{Q}$ |
| L | H | L | X | X | H | L |
| H | L | L | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | ↑ | L | L | Q0 | $\overline{Q}$0 |
| H | H | ↑ | H | L | H | L |
| H | H | ↑ | L | H | L | H |
| H | H | ↑ | H | H | TOGGLE | |
| H | H | L | X | X | Q0 | $\overline{Q}$0 |

$J = J1 \cdot J2 \cdot \overline{J}$
$K = K1 \cdot K2 \cdot \overline{K}$

If inputs J and $\overline{K}$ are not used, they must be grounded.

Preset or Clear Function can occur only when clock input is low.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level

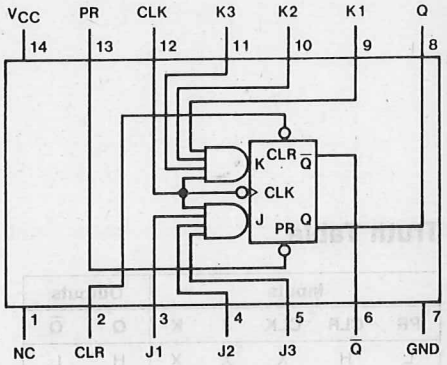
See page 5-29

## 71 AND-OR-Gated J-K Master-Slave Flip-Flops with Preset

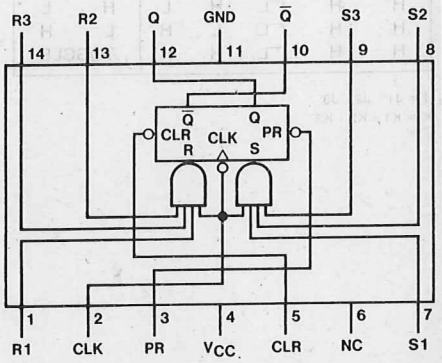
### Truth Table

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| PR | CLR | CLK | S | R | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | ⎍ | L | L | Q0 | $\overline{Q}$0 |
| H | H | ⎍ | H | L | H | L |
| H | H | ⎍ | L | H | L | H |
| H | H | ⎍ | H | H | INDETER-MINATE | |

R = R1 · R2 · R3
S = S1 · S2 · S3




54L71 (J); 74L71 (N)




54L71 (W)

See page 5-31

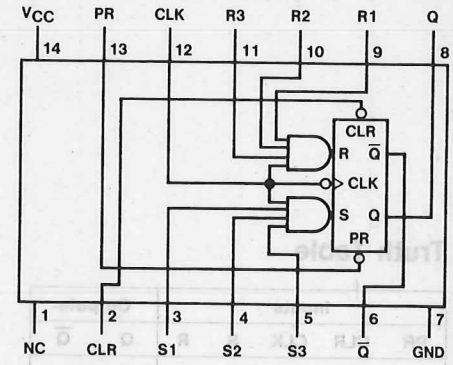
⎍⎍= high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

## 72 AND-Gated J-K Master-Slave Flip-Flops with Preset and Clear

### Truth Table

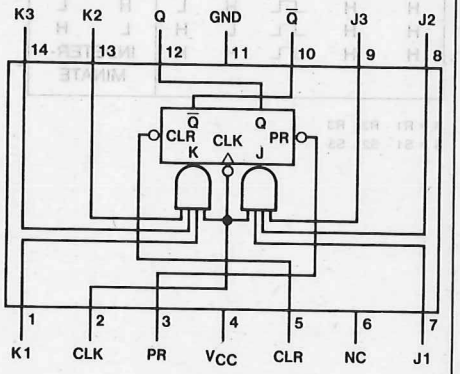
| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| PR | CLR | CLK | J | K | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | ⎍ | L | L | Q0 | $\overline{Q}$0 |
| H | H | ⎍ | H | L | H | L |
| H | H | ⎍ | L | H | L | H |
| H | H | ⎍ | H | H | TOGGLE | |

J = J1 · J2 · J3
K = K1 · K2 · K3




5472 (J)
54L72 (J)

7472 (N)
74L72 (N)




5472 (W); 54L72 (W)

See page 5-29 (72), 5-31 (L72)

## 73 Dual J-K Flip-Flops with Clear

### Truth Table

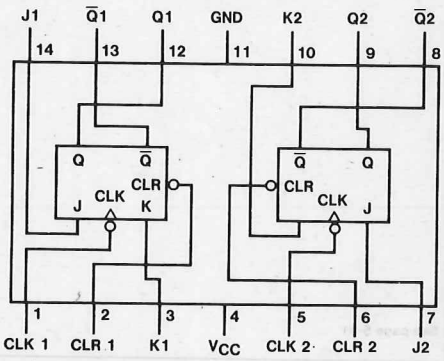
73, L73

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| CLR | CLK | J | K | Q | $\overline{Q}$ |
| L | X | X | X | L | H |
| H | ⎍ | L | L | Q0 | $\overline{Q}$0 |
| H | ⎍ | H | L | H | L |
| H | ⎍ | L | H | L | H |
| H | ⎍ | H | H | TOGGLE | |

### Truth Table

LS73A

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| CLR | CLK | J | K | Q | $\overline{Q}$ |
| L | X | X | X | L | H |
| H | ↓ | L | L | Q0 | $\overline{Q}$0 |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | TOGGLE | |
| H | H | X | X | Q0 | $\overline{Q}$0 |



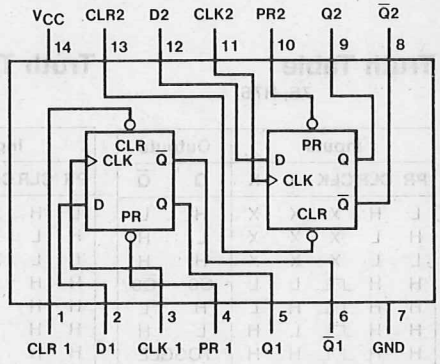

5473 (J,W)
54L73 (J,W)
54LS73 (J,W)

7473 (N)
74L73 (N)
74LS73 (N)

See page 5-29 (73), 5-31 (L73), 5-33 (LS73)

**Notes:** ⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to ouput on the falling edge of the pulse.
Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

## 74 Dual D Positive-Edge-Triggered Flip-Flops with Preset and Clear



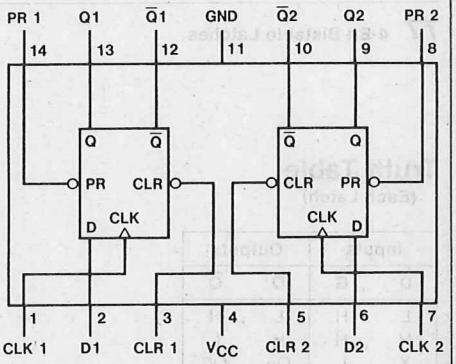

5474 (J)
54H74 (J)
54L74 (J)
54LS74A (J,W)
54S74 (J,W)

7474 (N)
74H74 (N)
74L74 (N)
74LS74A (N)
74S74 (N)

### Truth Table

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| PR | CLR | CLK | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H* | H* |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | Q0 | $\overline{Q}$0 |

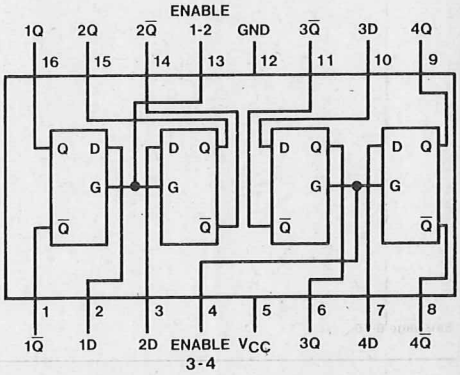
**Notes:** Q0 = the level of Q before the indicated input conditions were established.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.




5474 (W); 54L74 (W)

See page 5-29 (74), 5-38 (H74), 5-31 (L74), 5-33 (LS74A), 5-35 (S74)

## 75 4-Bit Bistable Latches




5475 (J,W)
54L75A (J,W)
54LS75 (J,W)

7475 (N)
74L75A (N)
74LS75 (N)

### Truth Table
(Each Latch)

| Inputs | | Outputs | |
|---|---|---|---|
| D | G | Q | $\overline{Q}$ |
| L | H | L | H |
| H | H | H | L |
| X | L | $Q_0$ | $\overline{Q}_0$ |

H = high level, L = low level, X = irrelevant
$Q_0$ = the level of Q before the high-to-low transition of G

See page 6-18

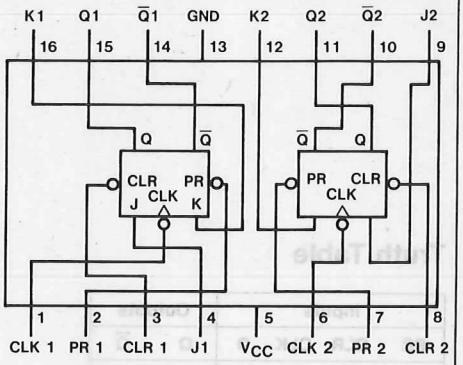
## 76 Dual J-K Flip-Flops with Preset and Clear

### Truth Table
76, H76

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| PR | CLR | CLK | J | K | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | ⎍ | L | L | Q0 | $\overline{Q}$0 |
| H | H | ⎍ | H | L | H | L |
| H | H | ⎍ | L | H | L | H |
| H | H | ⎍ | H | H | TOGGLE | |

### Truth Table
LS76

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| PR | CLR | CLK | J | K | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | ↓ | L | L | Q0 | $\overline{Q}$0 |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | TOGGLE | |
| H | H | H | X | X | Q0 | $\overline{Q}$0 |




5476 (J,W)
54LS76A (J,W)

7476 (N)
74LS76A (N)

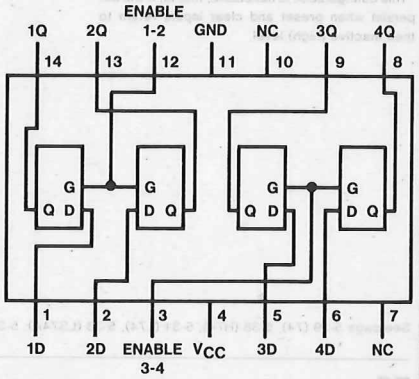
See page 5-29 (76), 5-33 (LS76A)

## 77 4-Bit Bistable Latches

### Truth Table
(Each Latch)

| Inputs | | Outputs | |
|---|---|---|---|
| D | G | Q | $\overline{Q}$ |
| L | H | L | H |
| H | H | H | L |
| X | L | $Q_0$ | $\overline{Q}$0 |

H = high level, L = low level, X = irrelevant
$Q_0$ = the level of Q before the high-to-low transistion of G




54LS77 (W); 74LS77 (W)

See page 6-18

Notes: ⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

## 78 Dual J-K Flip-Flops with Preset, Common Clear, and Common Clock

### Truth Table

L78

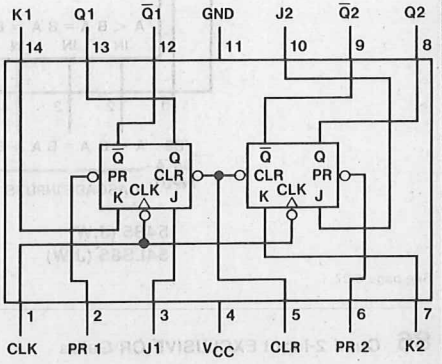
| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| PR | CLR | CLK | J | K | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | ⊓ | L | L | Q0 | $\overline{Q}$0 |
| H | H | ⊓ | H | L | H | L |
| H | H | ⊓ | L | H | L | H |
| H | H | ⊓ | H | H | TOGGLE | |

### Truth Table

LS78

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| PR | CLR | CLK | J | K | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | ↓ | L | L | Q0 | $\overline{Q}$0 |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | TOGGLE | |
| H | H | H | X | X | Q0 | $\overline{Q}$0 |

See page 5-31 (L78), 5-33 (LS78A)

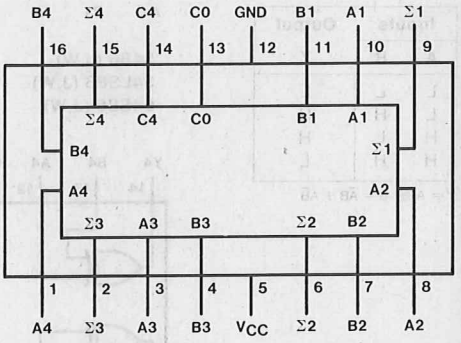



54L78 (J,W)
54LS78A (J,W)

74L78 (N)
74LS78A (N)

3

## 83 4-Bit Binary Full Adders With Fast Carry



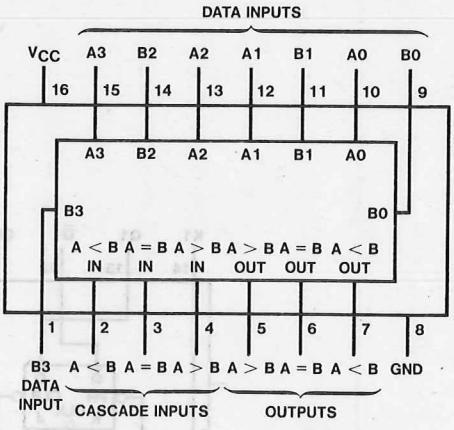

5483 (J,W)
54LS83A (J,W)

7483 (N)
74LS83A (N)

See page 6-21

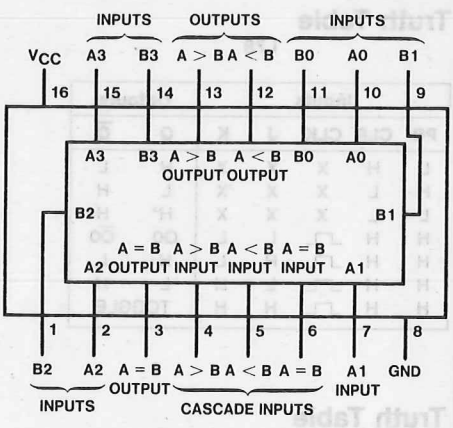
**Notes:** ⊓ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

## 85 4-Bit Magnitude Comparators




5485 (J,W)
54LS85 (J,W)

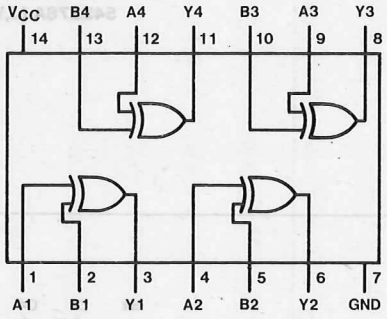
7485 (N)
74LS85 (N)




54L85 (J,W); 74L85 (N)

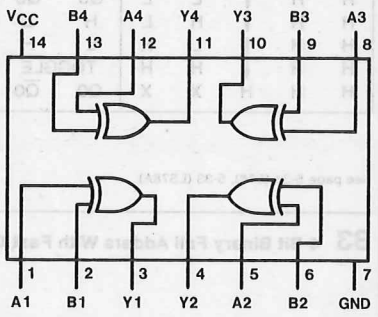
See page 6-27

## 86 Quad 2-Input EXCLUSIVE-OR Gates




5486 (J,W)
54LS86 (J,W)
54S86 (J,W)

7486 (N)
74LS86 (N)
74S86 (N)

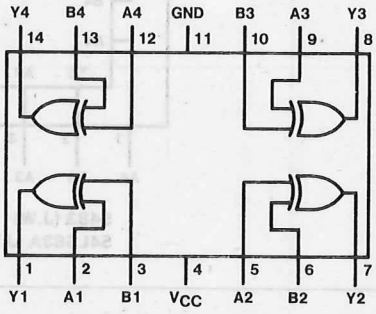



54L86 (J); 74L86 (N)

### Truth Table
(86,L86, LS86, S86)

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

$Y = A \oplus B = \overline{A}B + A\overline{B}$

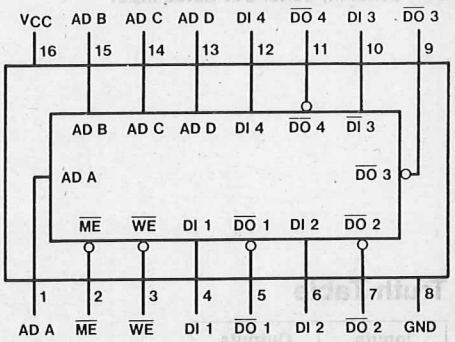



54L86 (W)

See page 5-40

## 64-Bit Read/Write Memories

### 89 16 4-Bit Words




5489B (J) 7489B (N)
54L89A (J) 74L89A (N)

See page 6-33

## Decade Counters

### 90 Divide-By-Two and Divide-By-Five

'90A, 'L90, 'LS90
BCD Count Sequence
(See Note A)

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

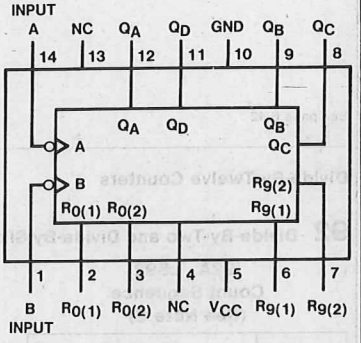
'90A, 'L90, 'LS90
Bi-Quinary (5-2)
(See Note B)

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_A$ | $Q_D$ | $Q_C$ | $Q_B$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

**Note A:** Output $Q_A$ is connected to input B for BCD count.
**Note B:** Output $Q_D$ is connected to input A for bi-quinary count.

'90A, 'L90, 'LS90
Reset/Count Function Table

| Reset Inputs | | | | Output | | | |
|---|---|---|---|---|---|---|---|
| $R_{O(1)}$ | $R_{O(2)}$ | $R_{9(1)}$ | $R_{9(2)}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | X | L | L | L | L |
| H | H | X | L | L | L | L | L |
| X | X | H | H | H | L | L | H |
| X | L | X | L | COUNT | | | |
| L | X | L | X | COUNT | | | |
| L | X | X | L | COUNT | | | |
| X | L | L | X | COUNT | | | |




5490A (J,W) 7490A (N)
54L90 (J,W) 74L90 (N)
54LS90 (J,W) 74LS90 (N)

NC—No internal connection (54LS90/74LS90)
NC—make no external connection (5490A/7490A) (54L90/74L90)

See page 6-36

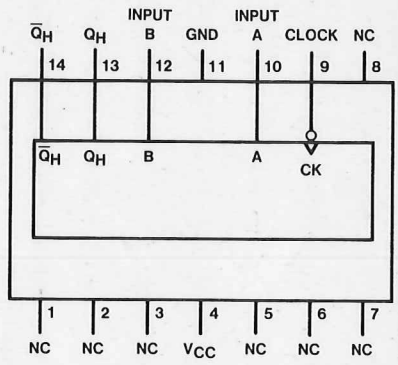
**8-Bit Shift Registers**

## 91 Serial-In, Serial-Out Gated Input

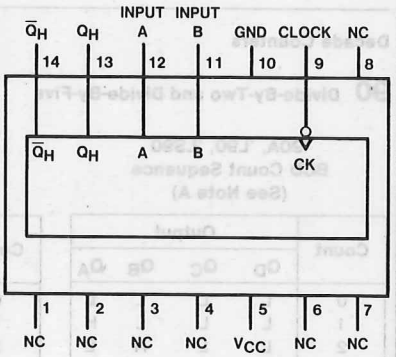
### Truth Table

| Inputs AT $t_n$ | | Outputs AT $t_{n+8}$ | |
|---|---|---|---|
| A | B | $Q_H$ | $\overline{Q}_H$ |
| H | H | H | L |
| L | X | L | H |
| X | L | L | H |

H = high, L = low
X = irrelevant
$t_n$ = Reference bit time, clock low
$t_{+8}$ = Bit time after 8 low-to-high clock transitions




54L91 (W)




54L91 (J); 74L91 (N)

NC—make no external connection

See page 6-42

**Divide-By-Twelve Counters**

## 92 Divide-By-Two and Divide-By-Six

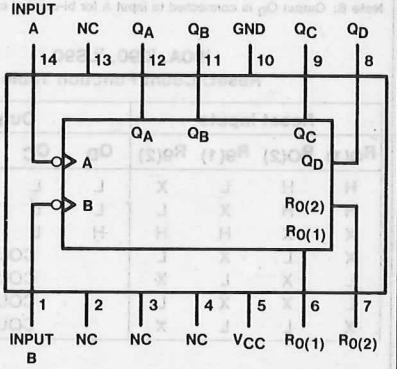
'92A, 'LS92
Count Sequence
(See Note C)

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | H | L | L | L |
| 7 | H | L | L | H |
| 8 | H | L | H | L |
| 9 | H | L | H | H |
| 10 | H | H | L | L |
| 11 | H | H | L | H |

C. Output $Q_A$ is connected to input B.

'92A, 'LS92,
Reset/Count Function Table

| Reset Inputs | | Output | | | |
|---|---|---|---|---|---|
| $R_{O(1)}$ | $R_{O(2)}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | L | L | L |
| L | X | COUNT | | | |
| X | L | COUNT | | | |




5492A (J,W) 7492A (N)
54LS92 (J,W) 74LS92 (N)

NC—No internal connection (54LS92/74LS92)
NC—Make no external connection (5492A/7492A)

See page 6-36

4-Bit Binary Counters

## 93 Divide-By-Two and Divide-By-Eight

'93A, 'L93, 'LS93
Count Sequence
(See Note C)

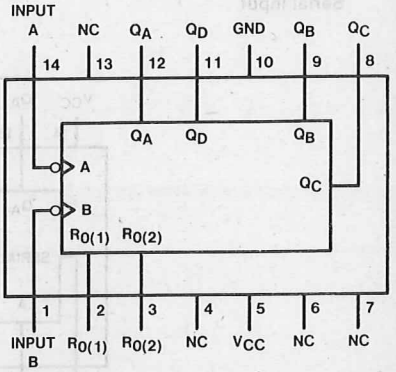
| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

'93A, 'L93, 'LS93
Reset/Count Function Table

| Reset Inputs | | Output | | | |
|---|---|---|---|---|---|
| $R_{O(1)}$ | $R_{O(2)}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | L | L | L |
| L | X | COUNT | | | |
| X | L | COUNT | | | |

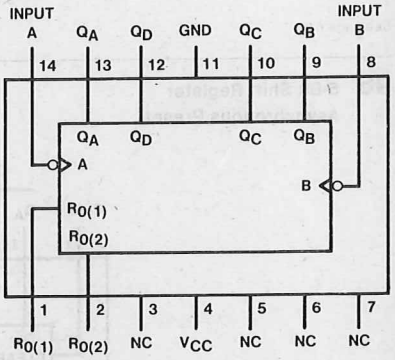
C. Output $Q_A$ is connected to input B.

See page 6-36




5493A (J,W)
54LS93 (J,W)

7493A (N)
74LS93 (N)



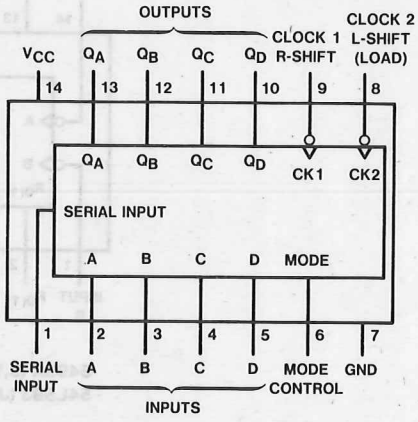

54L93 (J,W); 74L93 (N)

NC—No internal connection (54LS93/74LS93)
NC—Make no external connection (5493A/7493A)
(54L93/74L93)

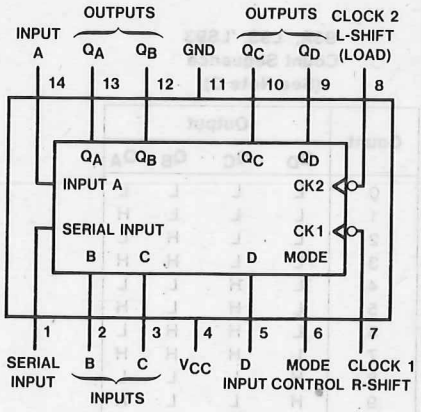
3

4-Bit Shift Registers

## 95 Parallel In/Parallel Out Shift Right, Shift Left Serial Input



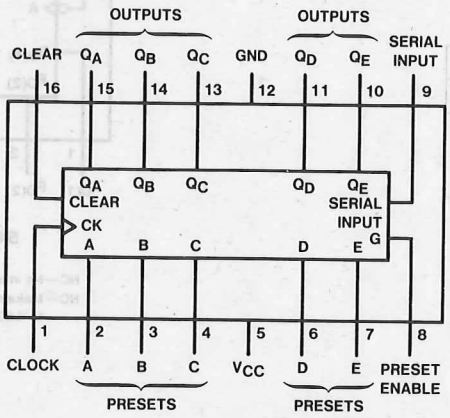

5495 (J,W); 7495 (N)




54L95 (J,W); 74L95 (N)

See page 6-44

## 96 5-Bit Shift Register Asynchronous Preset

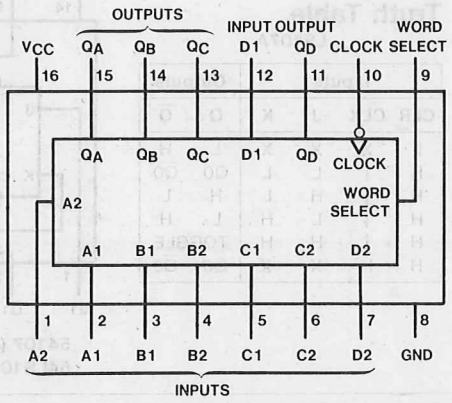



5496 (J,W); 7496 (N)

See page 6-47

4-Bit Data Selector/Storage Registers

## 98 Selects 1 of 2 4-Bit Words Parallel In/Out



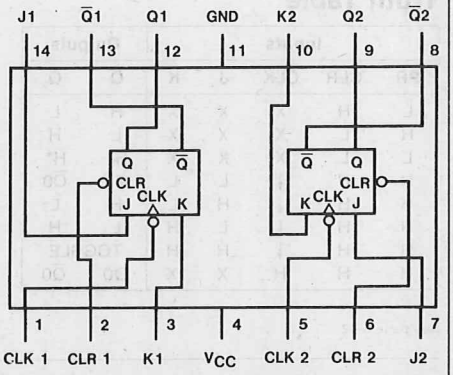

54L98 (J); 74L98 (N)

See page 6-51

## 103 Dual J-K Negative-Edge-Triggered Flip-Flops with Clear

### Truth Table

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| CLR | CLK | J | K | Q | $\overline{Q}$ |
| L | X | X | X | L | H |
| H | ↓ | L | L | Q0 | $\overline{Q}$0 |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | TOGGLE | |
| H | H | X | X | Q0 | $\overline{Q}$0 |



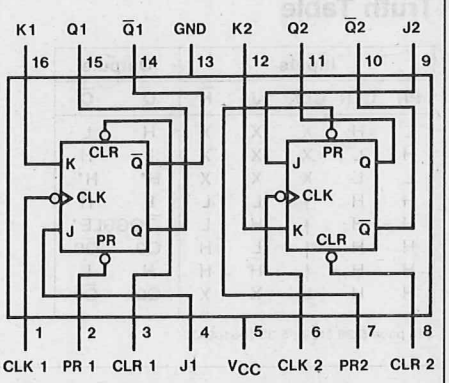

54H103 (J); 74H103 (N)

See page 5-42

## 106 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear

### Truth Table

| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| PR | CLR | CLK | J | K | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | ↓ | L | L | Q0 | $\overline{Q}$0 |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | TOGGLE | |
| H | H | H | X | X | Q0 | $\overline{Q}$0 |




54H106 (J); 74H106 (N)

See page 5-42

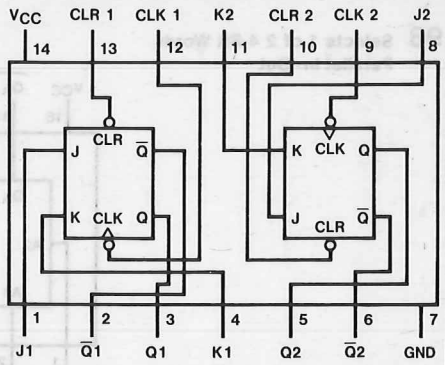
## 107 Dual J-K Master-Slave Flip-Flops with Clear

### Truth Table
107

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| CLR | CLK | J | K | Q | $\overline{Q}$ |
| L | X | X | X | L | H |
| H | ⎍ | L | L | Q0 | $\overline{Q0}$ |
| H | ⎍ | H | L | H | L |
| H | ⎍ | L | H | L | H |
| H | ⎍ | H | H | TOGGLE | |

### Truth Table
LS107A

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| CLR | CLK | J | K | Q | $\overline{Q}$ |
| L | X | X | X | L | H |
| H | ↓ | L | L | Q0 | $\overline{Q0}$ |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | TOGGLE | |
| H | H | X | X | Q0 | $\overline{Q0}$ |




54107 (J)
54LS107A (J,W)

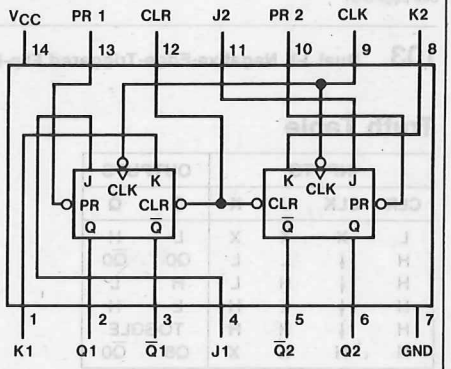
74107 (N)
74LS107A (N)

See page 5-29 (107), 5-33 (LS107A)

## 108 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset, Common Clear, and Common Clock

### Truth Table

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| PR | CLR | CLK | J | K | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | ↓ | L | L | Q0 | $\overline{Q0}$ |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | TOGGLE | |
| H | H | H | X | X | Q0 | $\overline{Q0}$ |



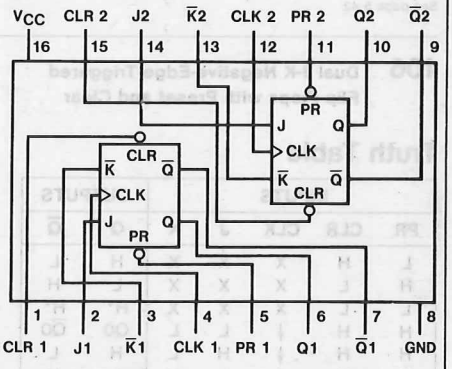

54H108 (J); 74H108 (N)

See page 5-42

## 109 Dual J-$\overline{K}$ Positive-Edge-Triggered Flip-Flops with Preset and Clear

### Truth Table

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| PR | CLR | CLK | J | $\overline{K}$ | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | ↑ | L | L | L | H |
| H | H | ↑ | H | L | TOGGLE | |
| H | H | ↑ | L | H | Q0 | $\overline{Q0}$ |
| H | H | ↑ | H | H | H | L |
| H | H | L | X | X | Q0 | $\overline{Q0}$ |




54109 (J,W)
54LS109 (J,W)

74109 (N)
74LS109 (N)

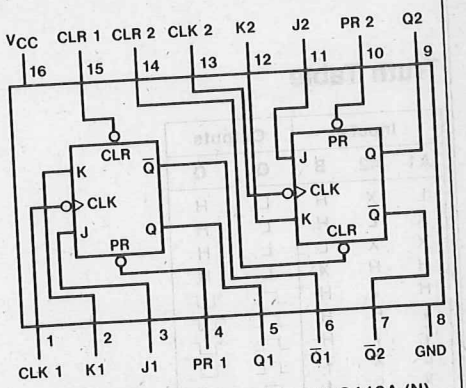
See page 5-29 (109), 5-33 (LS109A)

**Notes:** ⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

## 112 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear

### Truth Table

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| PR | CLR | CLK | J | K | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | ↓ | L | L | Q0 | $\overline{Q}$0 |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | TOGGLE | |
| H | H | H | X | X | Q0 | $\overline{Q}$0 |




54LS112A (J,W)
54S112 (J,W)

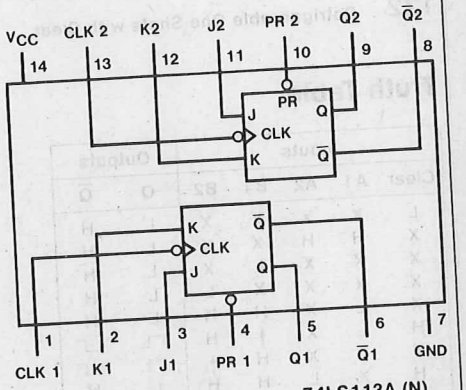
74LS112A (N)
74S112 (N)

See page 5-33 (LS112A), 5-35 (S112)

## 113 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset

### Truth Table

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| PR | CLK | J | K | Q | $\overline{Q}$ |
| L | X | X | X | H | L |
| H | ↓ | L | L | Q0 | $\overline{Q}$0 |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | TOGGLE | |
| H | H | X | X | Q0 | $\overline{Q}$0 |




54LS113A (J,W)
54S113 (J,W)

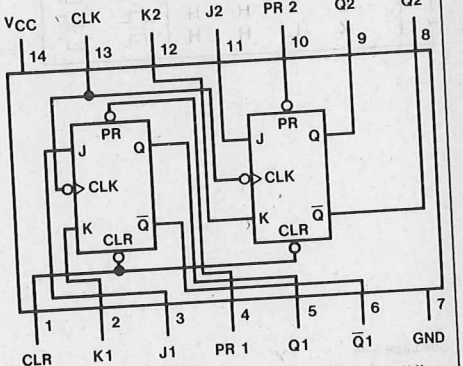
74LS113A (N)
74S113 (N)

See page 5-33 (LS113A), 5-35 (S113)

## 114 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset, Common Clear, and Common Clock

### Truth Table

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| PR | CLR | CLK | J | K | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | ↓ | L | L | Q0 | $\overline{Q}$0 |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | TOGGLE | |
| H | H | H | X | X | Q0 | $\overline{Q}$0 |




54LS114A (J,W)
54S114 (J,W)

74LS114A (N)
74S114 (N)

See page 5-33 (LS114A), 5-35 (S114)

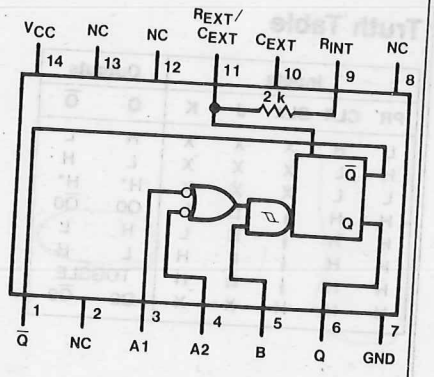
**Notes:** Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

## 121 One Shots

### Truth Table

| Inputs | | | Outputs | |
|---|---|---|---|---|
| A1 | A2 | B | Q | $\overline{Q}$ |
| L | X | H | L | H |
| X | L | H | L | H |
| X | X | L | L | H |
| H | H | X | L | H |
| H | ↓ | H | ⊓ | ⊔ |
| ↓ | H | H | ⊓ | ⊔ |
| ↓ | ↓ | H | ⊓ | ⊔ |
| L | X | ↑ | ⊓ | ⊔ |
| X | L | ↑ | ⊓ | ⊔ |

See page 5-44



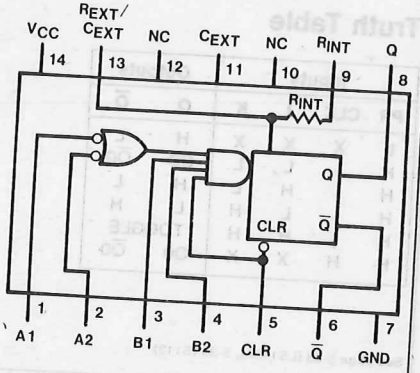

54121 (J,W); 74121 (N)

## 122 Retriggerable One Shots with Clear

### Truth Table

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| Clear | A1 | A2 | B1 | B2 | Q | $\overline{Q}$ |
| L | X | X | X | X | L | H |
| X | H | H | X | X | L | H |
| X | X | X | L | X | L | H |
| X | X | X | X | L | L | H |
| X | L | X | H | H | L | H |
| H | L | X | ↑ | H | ⊓ | ⊔ |
| H | L | X | H | ↑ | ⊓ | ⊔ |
| H | X | L | H | H | L | H |
| H | X | L | ↑ | H | ⊓ | ⊔ |
| H | H | ↓ | H | H | ⊓ | ⊔ |
| H | ↓ | ↓ | H | H | ⊓ | ⊔ |
| H | ↓ | H | H | H | ⊓ | ⊔ |
| ↑ | L | X | H | H | ⊓ | ⊔ |
| ↑ | X | L | H | H | ⊓ | ⊔ |

See page 5-46



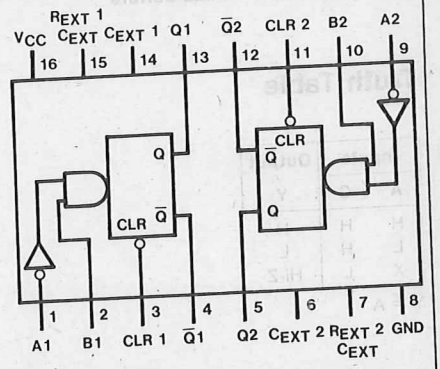

54LS122 (J,W); 74LS122 (N)

**Notes:** ⊓⊔ = one high-level pulse, ⊔⊓ = one low-level pulse.
To use the internal timing resistor of 54121/74121, connect $R_{INT}$ to $V_{CC}$.
An external timing capacitor may be connected between $C_{EXT}$ and $R_{EXT}/C_{EXT}$ (positive).
For accurate repeatable pulse widths, connect an external resistor between $R_{EXT}/C_{EXT}$ and $V_{CC}$ with $R_{INT}$ open-circuited.
To obtain variable pulse widths, connect external variable resistance between $R_{INT}$ or $R_{EXT}/C_{EXT}$ and $V_{CC}$.

## 123 Dual Retriggerable One Shots with Clear

### Truth Table
123, L123A

| Inputs | | | Outputs | |
|---|---|---|---|---|
| A | B | CLR | Q | $\overline{Q}$ |
| H | X | H | L | H |
| X | L | H | L | H |
| L | ↑ | H | ⎍ | ⎌ |
| ↓ | H | H | ⎍ | ⎌ |
| X | X | L | L | H |

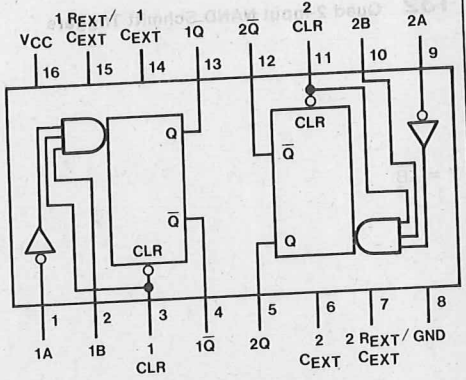



54123 (J,W)
54L123A (J,W)

74123 (N)
74L123A (N)

### Truth Table
LS123

| Inputs | | | Outputs | |
|---|---|---|---|---|
| Clear | A | B | Q | $\overline{Q}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | ⎍ | ⎌ |
| H | ↓ | H | ⎍ | ⎌ |
| ↑ | L | H | ⎍ | ⎌ |




54LS123 (J,W); 74LS123 (N)

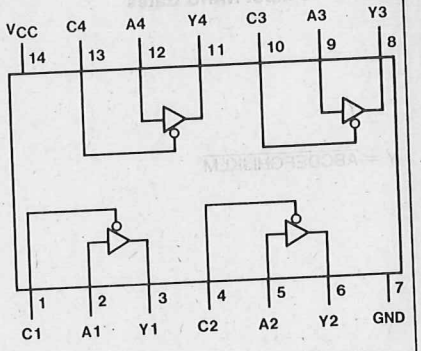
See page 5-46

## 125 TRI-STATE® Quad Buffers

### Truth Table

| Inputs | | Output |
|---|---|---|
| A | C | Y |
| H | L | H |
| L | L | L |
| X | H | Hi-Z |

Y = A




54125 (J,W)
54LS125A (J,W)

74125 (N)
74LS125A (N)

See page 5-48

**Notes:** ⎍ = one high-level pulse, ⎌ = one low-level pulse.
An external timing capacitor may be connected between $C_{EXT}$ and $R_{EXT}/C_{EXT}$ (positive).
For accurate repeatable pulse widths, connect an external resistor between $R_{EXT}/C_{EXT}$ and $V_{CC}$.
To obtain variable pulse widths, connect external variable resistance between $R_{EXT}/C_{EXT}$ and $V_{CC}$.

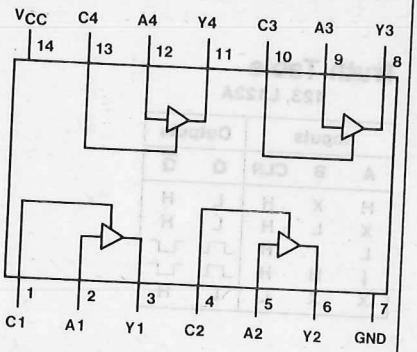
## 126 TRI-STATE® Quad Buffers

### Truth Table

| Inputs | | Output |
|---|---|---|
| A | C | Y |
| H | H | H |
| L | H | L |
| X | L | Hi-Z |

$Y = A$

See page 5-48



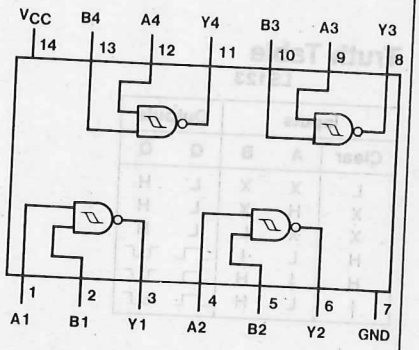

54126 (J,W)
54LS126A (J,W)

74126 (N)
74LS126A (N)

## 132 Quad 2-Input NAND Schmitt Triggers

$Y = \overline{AB}$

See page 5-16

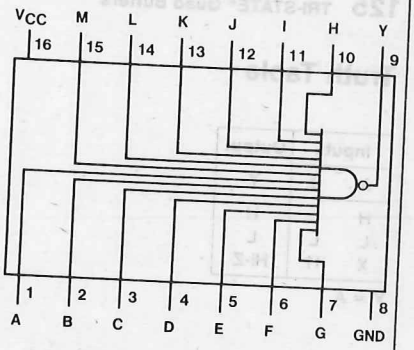



54132 (J,W)
54LS132 (J,W)

74132 (N)
74LS132 (N)

## 133 13-Input NAND Gates

$Y = \overline{ABCDEFGHIJKLM}$



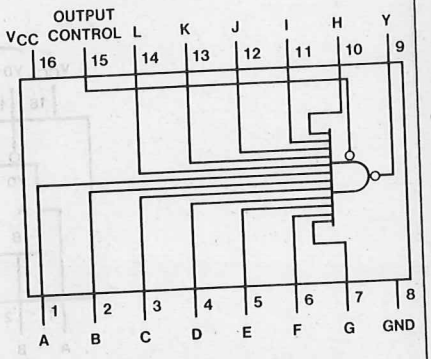

54S133 (J,W); 74S133 (N)

See page 5-4

## 134 TRI-STATE® 12-Input NAND Gates

$Y = \overline{ABCDEFGHIJKL}$

Output is off (disabled) when output control is high.




54S134 (J,W); 74S134 (N)

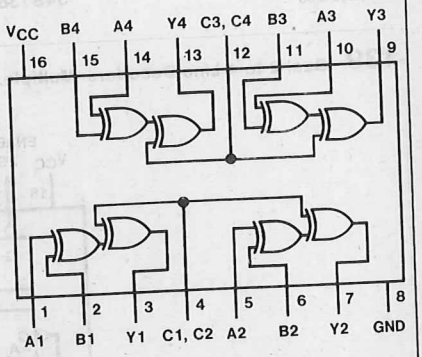
See page 5-48

## 135 Quad EXCLUSIVE-OR/NOR Gates

### Truth Table

| Inputs | | | Output |
|---|---|---|---|
| A | B | C | Y |
| L | L | L | L |
| L | H | L | H |
| H | L | L | H |
| H | H | L | L |
| L | L | H | H |
| L | H | H | L |
| H | L | H | L |
| H | H | H | H |

$Y = (A \oplus B) \oplus C =$
$A\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}\overline{B}C + ABC$




54S135 (J,W); 74S135 (N)

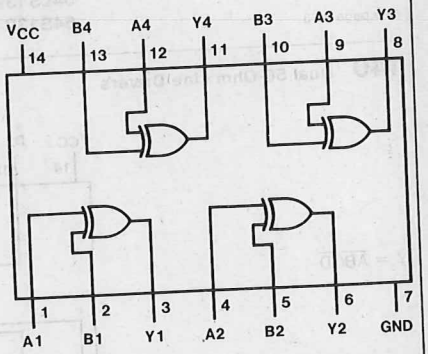
See page 5-50

## 136 Quad EXCLUSIVE-OR Gates with Open-Collector Outputs

### Truth Table

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

$Y = A \oplus B = \overline{A}B + A\overline{B}$

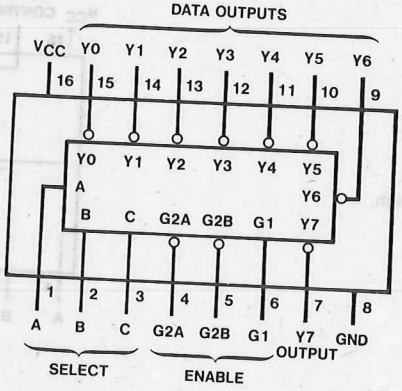



54LS136 (J,W)
54S136 (J,W)

74LS136 (N)
74S136 (N)

See page 5-52

## 138 3-to-8 Line Decoders/Multiplexers

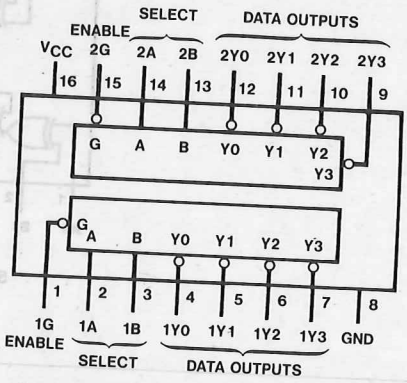



**54LS138 (J,W)**
**54S138 (J,W)**

**74LS138 (N)**
**74S138 (N)**

See page 6-53

## 139 Dual 2-to-4 Line Decoders/Multiplexers



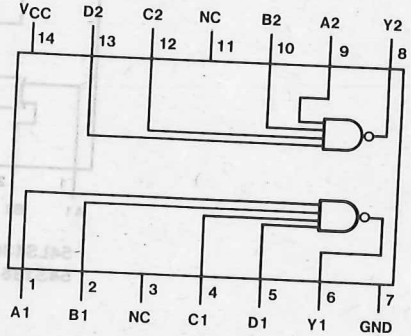

**54LS139 (J,W)**
**54S139 (J,W)**

**74LS139 (N)**
**74S139 (N)**

See page 6-53

## 140 Dual 50-Ohm Line Drivers

$Y = \overline{ABCD}$

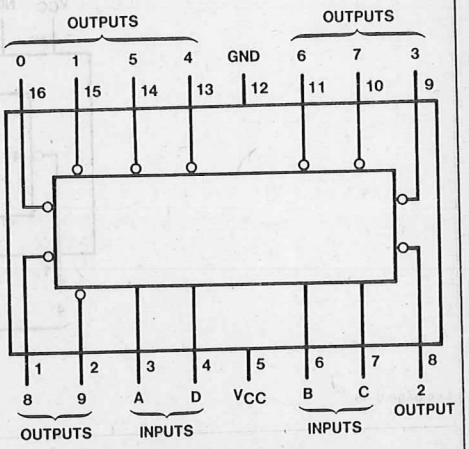



**54S140 (J,W); 74S140 (N)**

See page 5-22

## 141 NIXIE® Driver

| Input | | | | Output |
|---|---|---|---|---|
| D | C | B | A | ON* |
| L | L | L | L | 0 |
| L | L | L | H | 1 |
| L | L | H | L | 2 |
| L | L | H | H | 3 |
| L | H | L | L | 4 |
| L | H | L | H | 5 |
| L | H | H | L | 6 |
| L | H | H | H | 7 |
| H | L | L | L | 8 |
| H | L | L | H | 9 |
| (Over Range) | | | | |
| H | L | H | L | None |
| H | L | H | H | None |
| H | H | L | L | None |
| H | H | L | H | None |
| H | H | H | L | None |
| H | H | H | H | None |



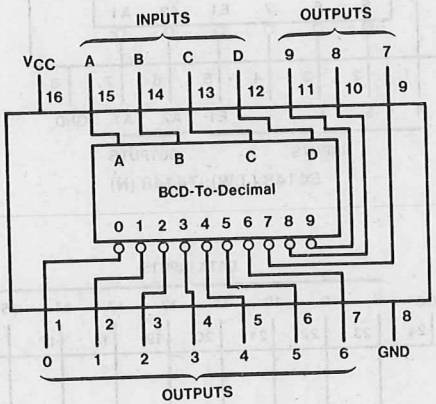

54141 (J,W); 74141 (N)

See page 6-4

3

### BCD-To-Decimal Decoders/Drivers For Lamps, Relays, MOS

## 145 BCD-to decimal

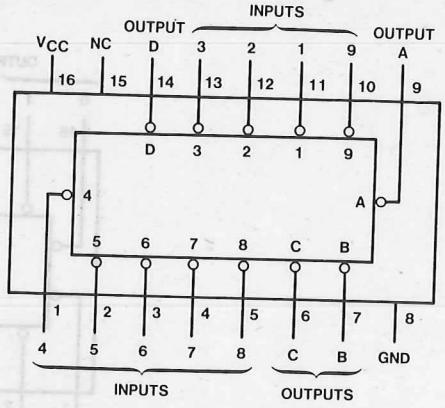



54145 (J,W); 74145 (N)

See page 6-10

## 10-Line Decimal to 4-Line BCD Priority Encoders

### 147



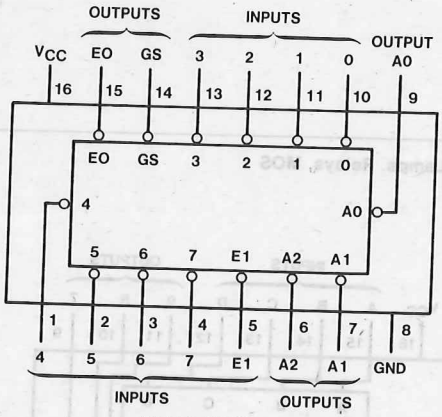

54147 (J,W); 74147 (N)

NC—No internal connection

See page 6-58

## 8-Line-To-3-Line Octal Priority Encoders

### 148

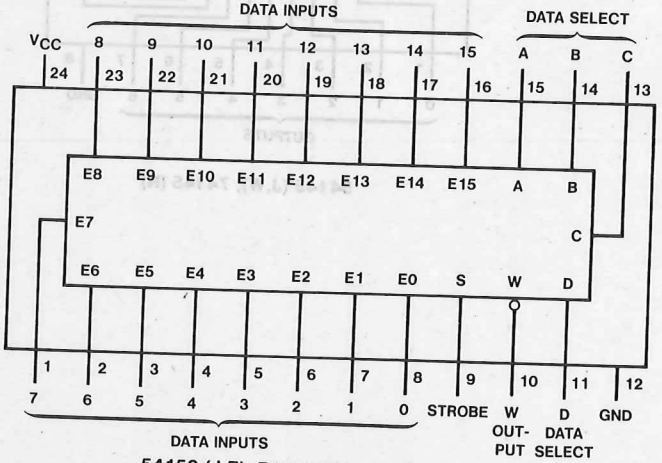



54148 (J,W); 74148 (N)

See page 6-58

## 1-Of-16-Data Selectors/Multiplexers

### 150

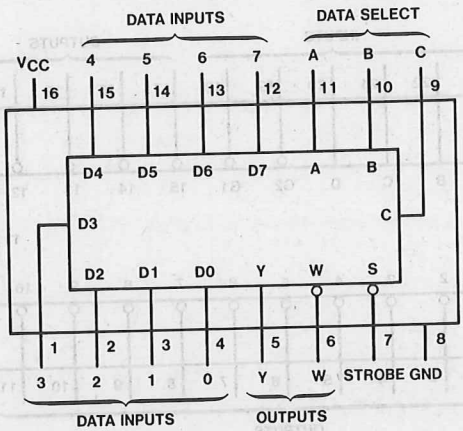



54150 (J,F); 74150 (N)

See page 6-62

**1-Of-8 Data Selectors/Multiplexers**

## 151



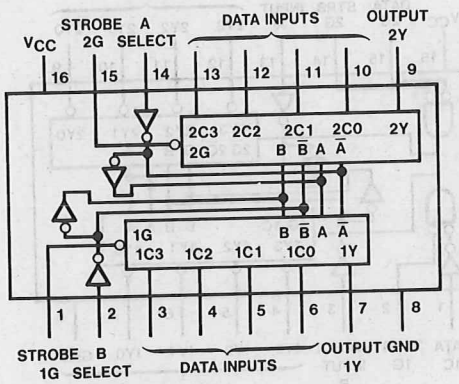

**54151A (J,W)**
**54LS151 (J,W)**
**54S151 (J,W)**

**74151A (N)**
**74LS151 (N)**
**74S151 (N)**

See page 6-62

**Dual 4-Line To 1-Line Data Selectors/Multiplexers**

## 153



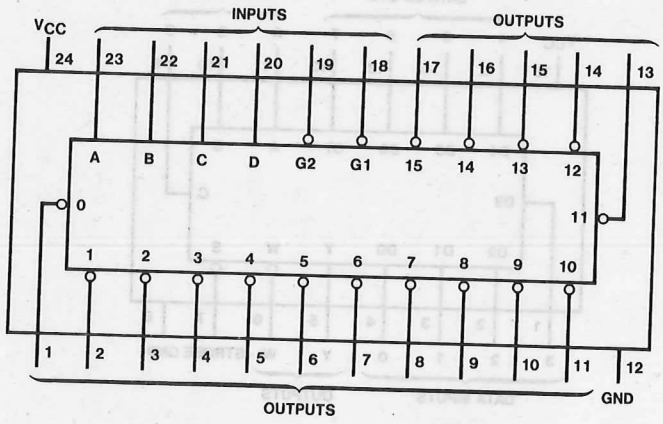

**54153 (J,W)**
**54LS153 (J,W)**
**54S153 (J,W)**

**74153 (N)**
**74LS153 (N)**
**74S153 (N)**

See page 6-68

4-Line to 16-Line Decoders/Demultiplexers

## 154




54154 (J,F)
54L154A (J,F)
54LS154 (J,W)

74154 (N)
74L154A (N)
74LS154 (N)

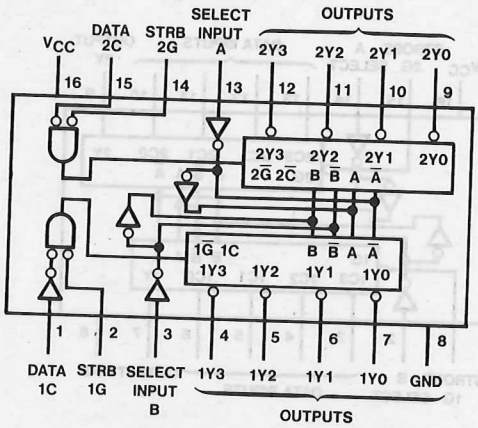
See page 6-71

Decoders/Demultiplexers

Dual 2- to 4-line decoder
Dual 1- to 4-line demultiplexer
3- to 8-line decoder
1- to 8-line demultiplexer

**155** Totem-pole outputs

**156** Open-collector outputs




54155 (J,W)
54LS155 (J,W)
54156 (J,W)
54LS156 (J,W)

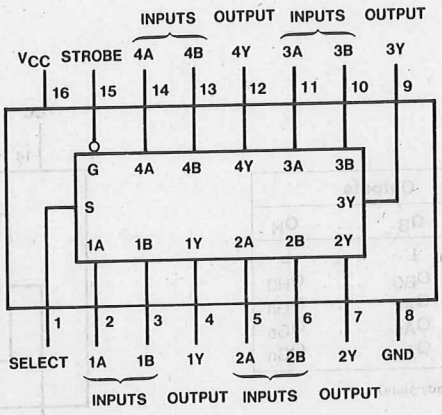
74155 (N)
74LS155 (N)
74156 (N)
74LS156 (N)

See page 6-75

## Quad 2- To 1-Line Data Selectors/Multiplexers

**157** Noninverted data outputs

**158** Inverted data outputs




54157 (J,W)
54L157A (J,W)
54LS157 (J,W)
54S157 (J,W)
54LS158 (J,W)
54S158 (J,W)

74157 (N)
74L157A (N)
74LS157 (N)
74S157 (N)
74LS158 (N)
74S158 (N)

See page 6-78

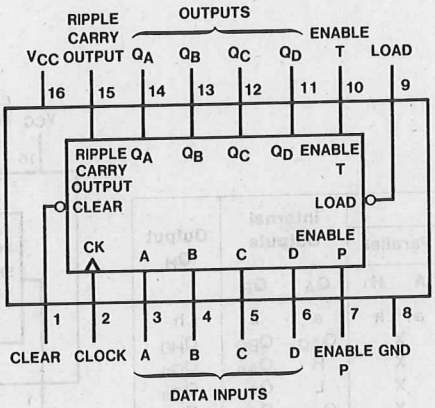
## Synchronous 4-Bit Counters

**160** Decade, direct clear

**161** Binary, direct clear

**162** Decade, synchronous clear

**163** Binary, synchronous clear




54160A (J,W)
54LS160A (J,W)
54S160 (J,W)
54161A (J,W)
54LS161A (J,W)
54S161 (J,W)
54162A (J,W)
54LS162A (J,W)
54S162 (J,W)
54163A (J,W)
54LS163A (J,W)
54S163 (J,W)

74160A (N)
74LS160A (N)
74S160 (N)
74161A (N)
74LS161A (N)
74S161 (N)
74162A (N)
74LS162A (N)
74S162 (N)
74163A (N)
74LS163A (N)
74S163 (N)

See page 6-82

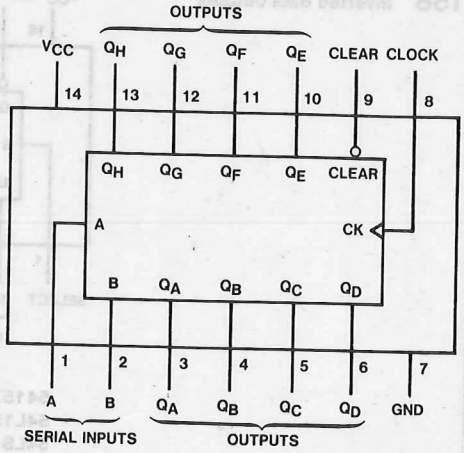
**8-Bit Parallel Output Serial Shift Registers**

## 164 Asynchronous clear

### Truth Table

| Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| Clear | Clock | A | B | $Q_A$ | $Q_B$ | ... | $Q_H$ |
| L | X | X | X | L | L | ... | L |
| H | L | X | X | $Q_{A0}$ | $Q_{B0}$ | ... | $Q_{H0}$ |
| H | ↑ | H | H | H | $Q_{An}$ | ... | $Q_{Gn}$ |
| H | ↑ | L | X | L | $Q_{An}$ | ... | $Q_{Gn}$ |
| H | ↑ | X | L | L | $Q_{An}$ | ... | $Q_{Gn}$ |

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
$Q_{A0}$, $Q_{B0}$, $Q_{H0}$ = the level of $Q_A$, $Q_B$, or $Q_H$, respectively, before the indicated steady-state input conditions were established.
$Q_{An}$, $Q_{Gn}$ = the level of $Q_A$ or $Q_G$ before the most-recent ↑ transition of the clock; indicates a one-bit shift.




54164 (J,W)
54L164A (J,W)
54LS164 (J,W)

74164 (N)
74L164A (N)
74LS164 (N)

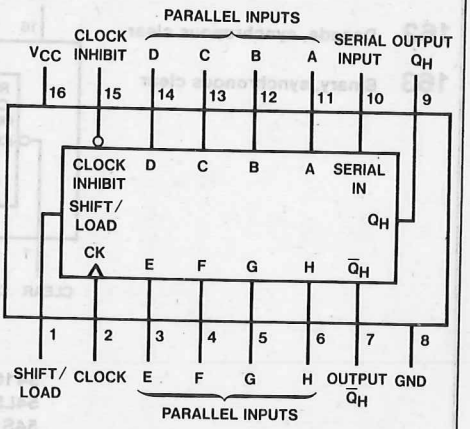
See page 6-95

**Parallel-Load 8-Bit Shift Registers With Complementary Outputs**

## 165

### Truth Table

| Inputs | | | | | Internal Outputs | | Output $Q_H$ |
|---|---|---|---|---|---|---|---|
| Shift/ Load | Clock Inhibit | Clock | Serial | Parallel A...H | $Q_A$ | $Q_B$ | |
| L | X | X | X | a...h | a | b | h |
| H | L | L | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |
| H | L | ↑ | H | X | H | $Q_{An}$ | $Q_{Gn}$ |
| H | L | ↑ | L | X | L | $Q_{An}$ | $Q_{Gn}$ |
| H | H | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |



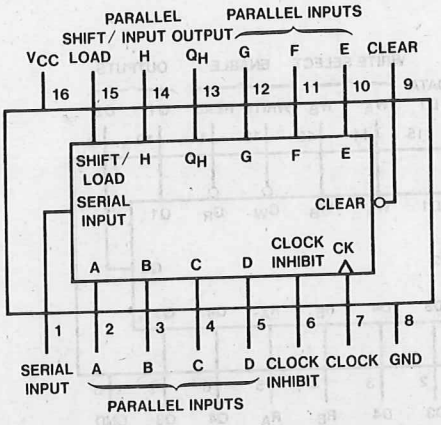

54165 (J,W)
54L165A (J,W)
54LS165 (J,W)

74165 (N)
74L165A (N)
74LS165 (N)

See page 6-98

8-Bit Shift Registers

## 166 Parallel/serial input Serial output




54166 (J)
54LS166 (J,W)

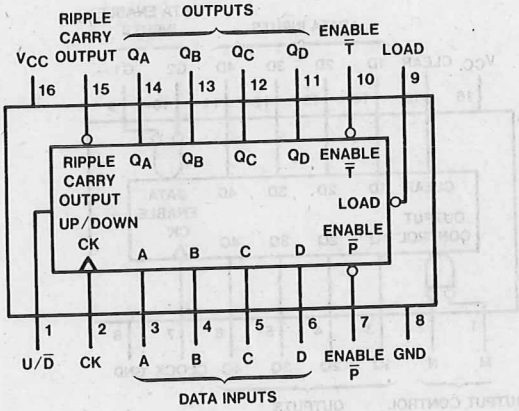
74166 (N)
74LS166 (N)

See page 6-102

4-Bit Up/Down Synchronous Counters

## 168 Decade

## 169 Binary




54LS168A (J,W)
54LS169A (J,W)

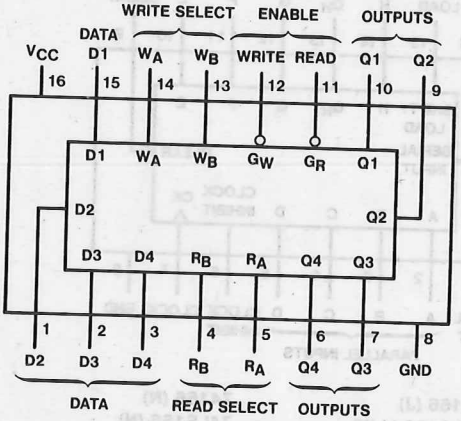
74LS168A (N)
74LS169A (N)

See page 6-106

## 4-By-4 Register Files

### 170

Separate read/write addressing
Simultaneous read and write
Open-collector outputs
Expandable to 1024 words




54LS170 (J,W)

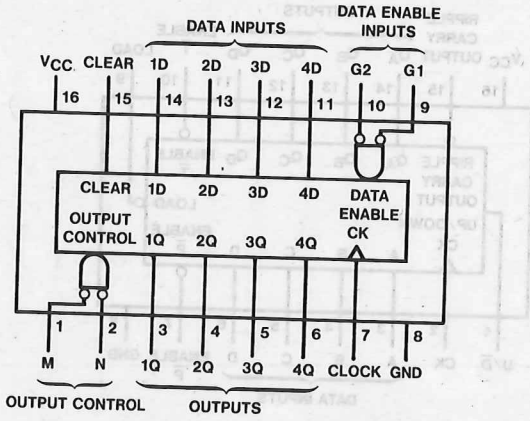
74170 (N)
74LS170 (N)

See page 6-113

## 4-Bit D-Type Registers

### 173

TRI-STATE® outputs




54173 (J,W)
54LS173 (J,W)

74173 (N)
74LS173 (N)

See page 6-118

Hex D-Type Flip-Flops

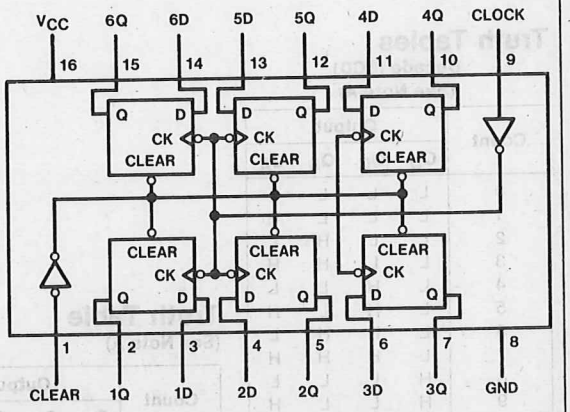
## 174 Single rail outputs
## Common direct clear

### Truth Table
(Each Flip-Flop)

| Inputs | | | Outputs |
|---|---|---|---|
| Clear | Clock | D | Q |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | L | X | $Q_0$ |

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
$Q_0$ = the level of Q before the indicated steady-state input conditions were established.

See page 6-122




54174 (J,W)
54LS174 (J,W)
54S174 (J,W)

74174 (N)
74LS174 (N)
74S174 (N)

Quad D-Type Flip-Flops

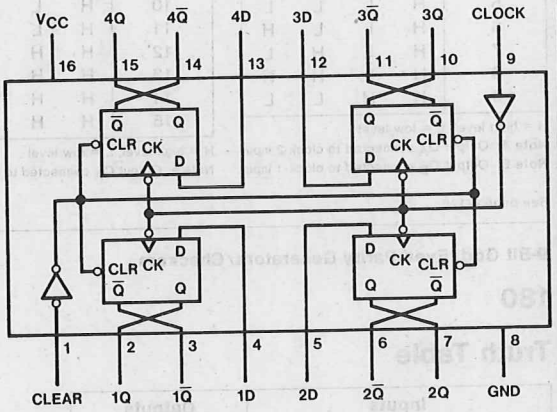
## 175 Complementary outputs
## Common direct clear

### Truth Table
(Each Flip-Flop)

| Inputs | | | Outputs | |
|---|---|---|---|---|
| Clear | Clock | D | Q | $\overline{Q}$ |
| L | X | X | L | H |
| H | ↑ | H | H | L |
| H | ↑ | L | L | H |
| H | L | X | $Q_0$ | $\overline{Q}_0$ |

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
$Q_0$ = the level of Q before the indicated steady-state input conditions were established.

See page 6-122




54175 (J,W)
54LS175 (J,W)
54S175 (J,W)

74175 (N)
74LS175 (N)
74S175 (N)

3

Presettable Counters/Latches

## 176 Decade (Bi-quinary)

## 177 Binary

## Truth Tables

Decade (BCD)
(See Note A)

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

Bi-Quinary (5-2)
(See Note B)

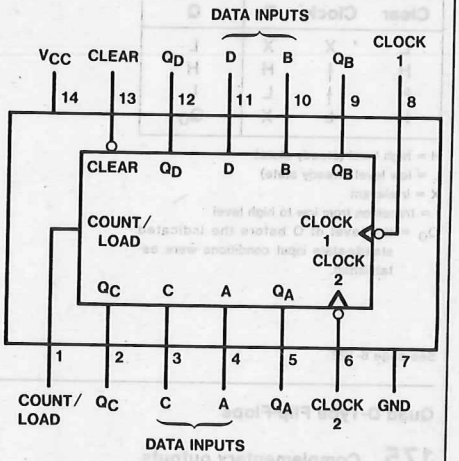
| Count | Output | | | |
|---|---|---|---|---|
| | $Q_A$ | $Q_D$ | $Q_C$ | $Q_B$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

H = high level, L = low level
Note A: Output $Q_A$ connected to clock-2 input.
Note B: Output $Q_D$ connected to clock-1 input.

## Truth Table
(See Note A)

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

H = high level, L = low level
Note A: Output $Q_A$ connected to clock-2 input.




54176 (J)
54177 (J)

74176 (N)
74176 (N)

See page 6-126

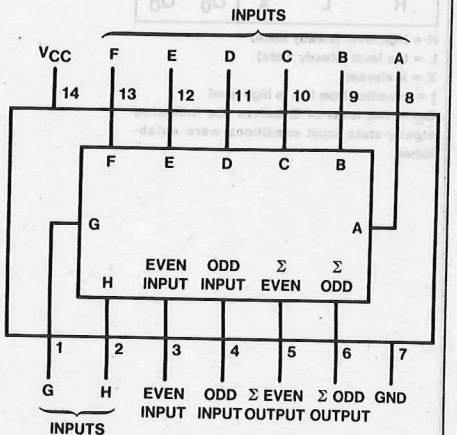
9-Bit Odd/Even Parity Generators/Checkers

## 180

## Truth Table

| Inputs | | | Outputs | |
|---|---|---|---|---|
| Σ of H's at A thru H | Even | Odd | Σ Even | Σ Odd |
| Even | H | L | H | L |
| Odd | H | L | L | H |
| Even | L | H | L | H |
| Odd | L | H | H | L |
| X | H | H | L | L |
| X | L | L | H | H |

H = high level, L = low level, X = irrelevant

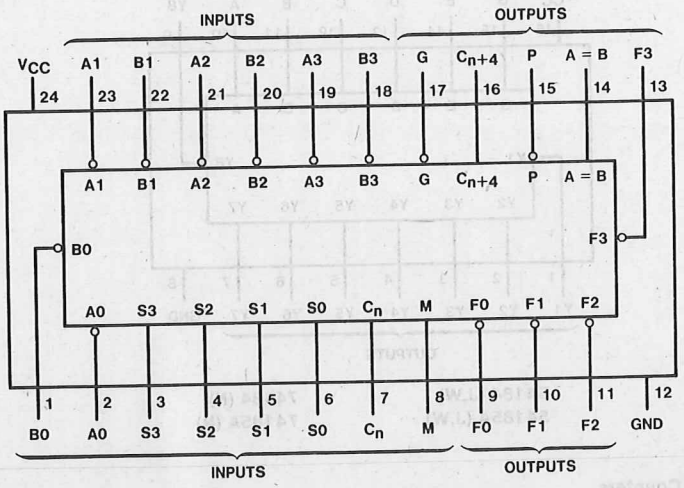



54180 (J,W); 74180 (N)

See page 6-132

## Arithmetic Logic Units/Function Generators

### 181 16 Arithmetic operations 16 Logic functions




54181 (J)
54S181 (J)

74181 (N)
74S181 (N)

See page 6-135

## Look-Ahead Carry Generators

### 182

## Truth Table

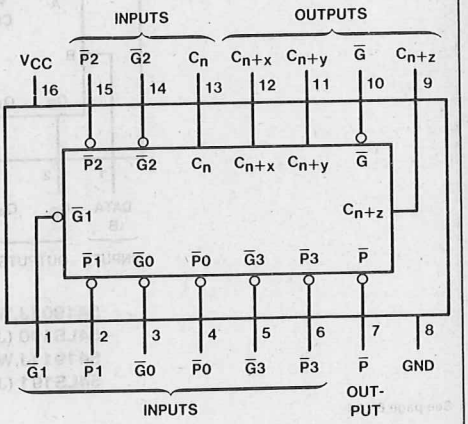
For $\overline{G}$ Output

| Inputs | | | | | | | Output |
|---|---|---|---|---|---|---|---|
| $\overline{G}3$ | $\overline{G}2$ | $\overline{G}1$ | $\overline{G}0$ | $\overline{P}3$ | $\overline{P}2$ | $\overline{P}1$ | $\overline{G}$ |
| L | X | X | X | X | X | X | L |
| X | L | X | X | L | X | X | L |
| X | X | L | X | L | L | X | L |
| X | X | X | L | L | L | L | L |
| All other combinations | | | | | | | H |

H = high level, L = low level, X = irrelevant
Any inputs not shown in a given table are irrelevant with respect to that output.

For $\overline{P}$ Output

| Inputs | | | | Output |
|---|---|---|---|---|
| $\overline{P}3$ | $\overline{P}2$ | $\overline{P}1$ | $\overline{P}0$ | $\overline{P}$ |
| L | L | L | L | L |
| All other combinations | | | | H |




54S182 (J,W); 74S182 (N)

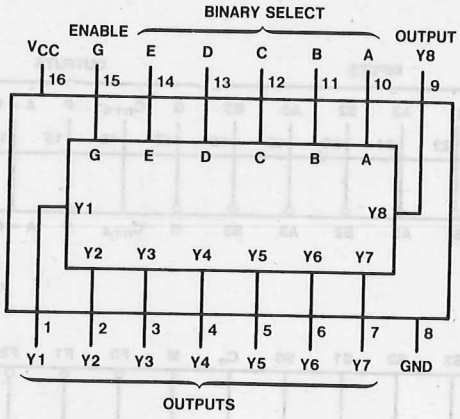
See page 6-144

## Code Converters

### Cascadeable to N-Bits

**184** BCD-to-Binary

**185** Binary-to-BCD




54184 (J,W)
54185A (J,W)

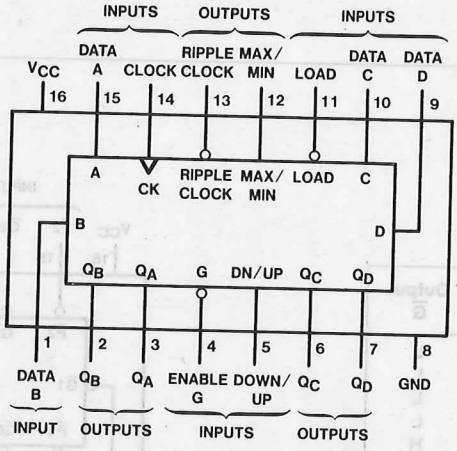
74184 (N)
74185A (N)

See page 6-148

## Synchronous Up/Down Counters

**190** BCD

**191** Binary




54190 (J,W)
54LS190 (J,W)
54191 (J,W)
54LS191 (J,W)

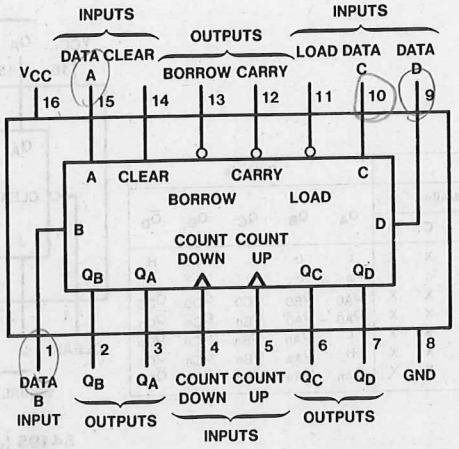
74190 (N)
74LS190 (N)
74191 (N)
74LS191 (N)

See page 6-154

## Synchronous Up/Down Dual Clock Counters

## 192 BCD with clear

## 193 Binary with clear




**54192 (J,W)**
**54L192 (J,W)**
**54LS192 (J,W)**
**54193 (J,W)**
**54L193 (J,W)**
**54LS193 (J,W)**

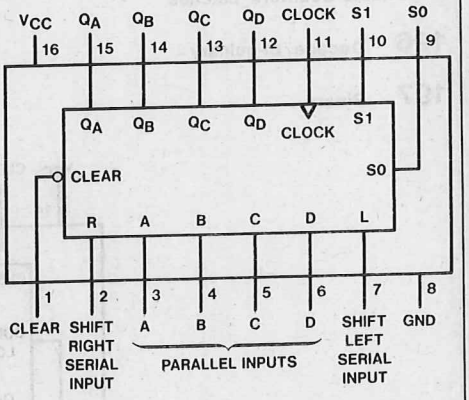
**74192 (N)**
**74L192 (N)**
**74LS192 (N)**
**74193 (N)**
**74L193 (N)**
**74LS193 (N)**

See page 6-161

3

## 4-Bit Bidirectional Universal Shift Registers

## 194




### Truth Table

| Inputs | | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clear | Mode | | Clock | Serial | | Parallel | | | | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| | S1 | S2 | | Left | Right | A | B | C | D | | | | |
| L | X | X | X | X | X | X | X | X | X | L | L | L | L |
| H | X | X | L | X | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| H | H | H | ↑ | X | X | a | b | c | d | a | b | c | d |
| H | L | H | ↑ | X | H | X | X | X | X | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| H | L | H | ↑ | X | L | X | X | X | X | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| H | H | L | ↑ | H | X | X | X | X | X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | H |
| H | H | L | ↑ | L | X | X | X | X | X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | L |
| H | L | L | X | X | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
$Q_{A0}$, $Q_{B0}$, $Q_{C0}$, $Q_{D0}$, = the level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the indicated steady-state input conditions were established.
$Q_{An}$, $Q_{Bn}$, $Q_{Cn}$, $Q_{Dn}$ = the level of $Q_A$, $Q_B$, $Q_C$, respectively, before the most-recent ↑ transition of the clock.

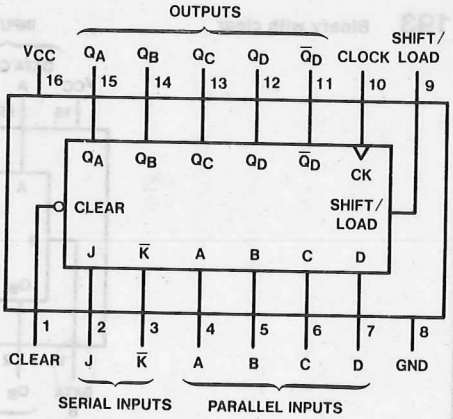
**54194 (J,W)**
**54LS194A (J,W)**
**54S194 (J,W)**

**74194 (N)**
**74LS194A (N)**
**74S194 (N)**

See page 6-169

**4-Bit Parallel-Access Shift Registers**

## 195




### Truth Table

| Inputs | | | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clear | Shift/ Load | Clock | Serial | | Parallel | | | | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $\overline{Q}_D$ |
| | | | J | $\overline{K}$ | A | B | C | D | | | | | |
| L | X | X | X | X | X | X | X | X | L | L | L | L | H |
| H | L | ↑ | X | X | a | b | c | d | a | b | c | d | $\overline{d}$ |
| H | H | L | X | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $\overline{Q}_{D0}$ |
| H | H | ↑ | L | H | X | X | X | X | $Q_{A0}$ | $Q_{A0}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |
| H | H | ↑ | L | L | X | X | X | X | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |
| H | H | ↑ | H | H | X | X | X | X | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |
| H | H | ↑ | H | L | X | X | X | X | $\overline{Q}_{An}$ | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
$Q_{A0}$, $Q_{B0}$, $Q_{C0}$, $Q_{D0}$, = the level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the indicated steady-state input conditions were established.
$Q_{An}$, $Q_{Bn}$, $Q_{Cn}$ = the level of $Q_A$, $Q_B$, $Q_C$, respectively, before the most-recent transition of the clock.

See page 6-174

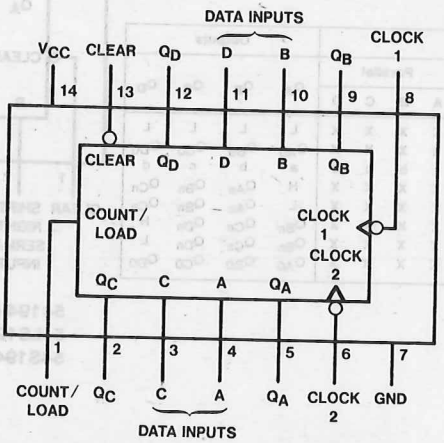
**54195 (J,W)**
**54LS195A (J,W)**
**54S195 (J,W)**

**74195 (N)**
**74LS195A (N)**
**74S195 (N)**

**Presettable Counters/Latches**

## 196 Decade/Bi-quinary

## 197 Binary



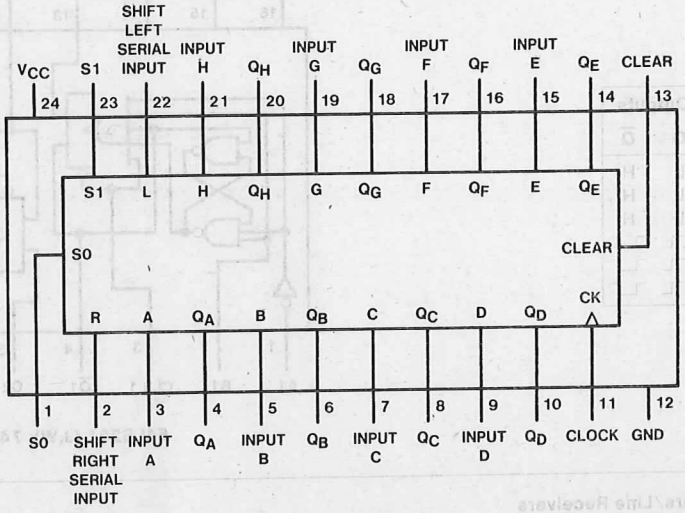

**54196 (J,N)**
**54LS196 (J,W)**
**54S196 (J,W)**
**54197 (J)**
**54LS197 (J,W)**
**54S197 (J,W)**

**74196 (N)**
**74LS196 (N)**
**74S196 (N)**
**74197 (N)**
**74LS197 (N)**
**74S197 (N)**

See page 6-126

8-Bit Bidirectional Universal Shift Registers

## 198

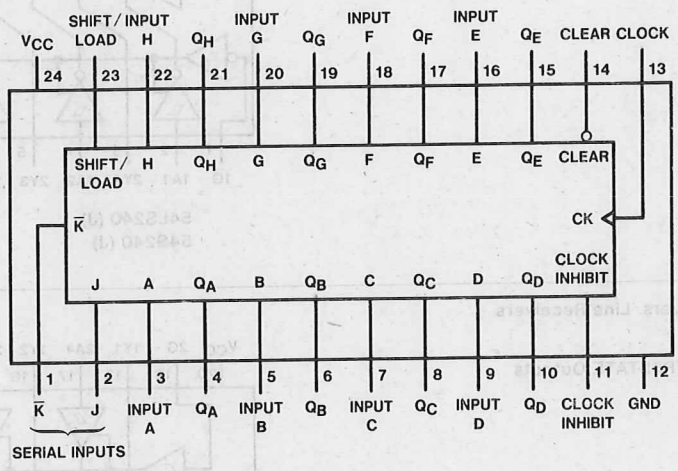



54198 (J); 74198 (N)

See page 6-178

8-Bit Bidirectional Universal Shift Registers

## 199 J-$\overline{K}$ serial inputs



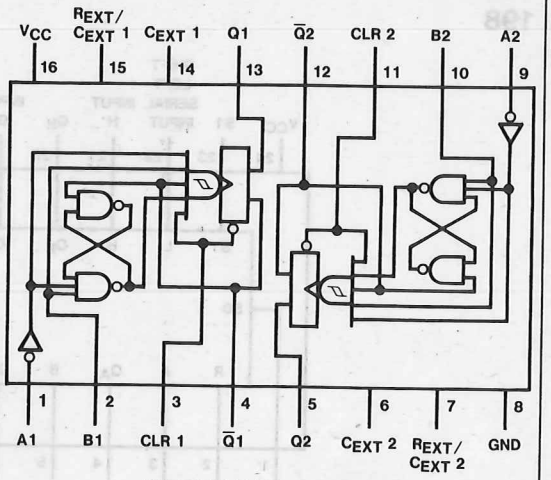

54199 (J); 74199 (N)

See page 6-178

## 221 Dual One Shots with Schmitt-Trigger Inputs

### Truth Table

| Inputs | | | Outputs | |
|---|---|---|---|---|
| Clear | A | B | Q | $\overline{Q}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | ⎍ | ⎍ |
| H | ↓ | H | ⎍ | ⎍ |
| ↑ | L | H | ⎍ | ⎍ |

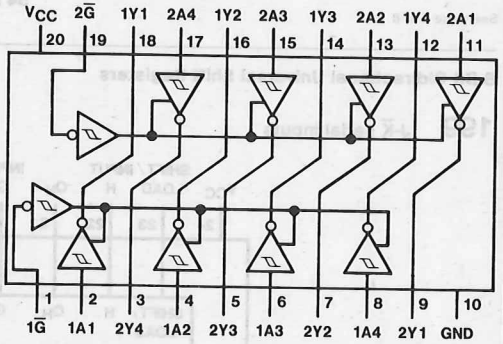



54LS221 (J,W); 74LS221 (N)

See page 5-44

Octal Buffers/Line Drivers/Line Receivers

## 240 Inverted TRI-STATE® Outputs



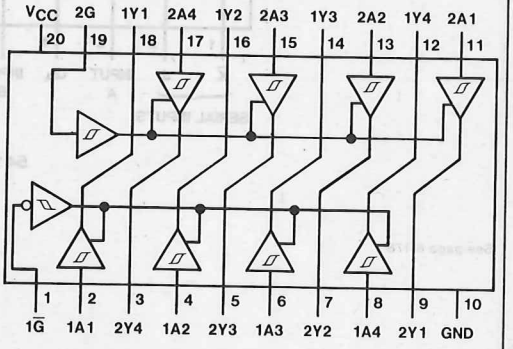

54LS240 (J)
54S240 (J)

74LS240 (N)
74S240 (N)

See page 5-53

Octal Buffers/Line Drivers/Line Receivers

## 241 Noninverted TRI-STATE Outputs



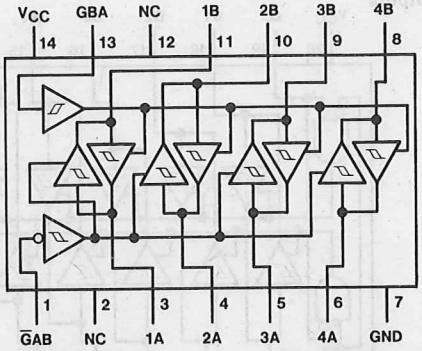

54LS241 (J)
54S241 (J)

74LS241 (N)
74S241 (N)

See page 5-53

**Quadruple BUS Transceivers**

## 242 Inverted TRI-STATE® Outputs



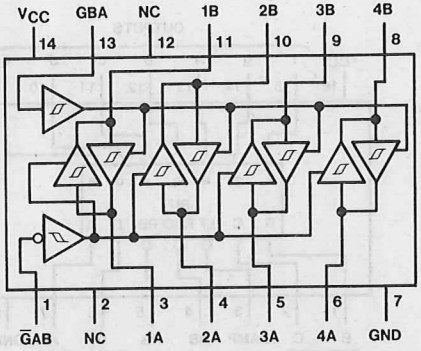

**54LS242 (J)** **74LS242 (N)**
**54S242 (J)** **74S242 (N)**

NC—No internal connection

See page 5-57

**Quadruple Bus Transceivers**

## 243 Noninverted TRI-STATE Outputs



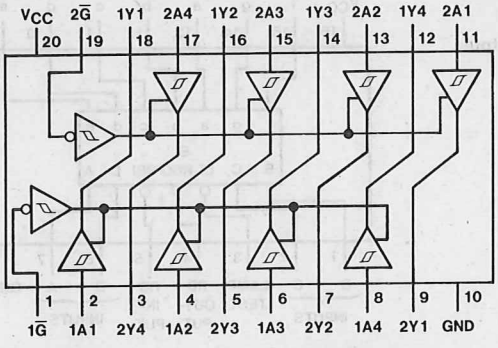

**54LS243 (J)** **74LS243 (N)**
**54S243 (J)** **74S243 (N)**

NC—No internal connection

See page 5-57

**Octal Buffers/Line Drivers/Line Receivers**

## 244 Noninverted TRI-STATE Outputs

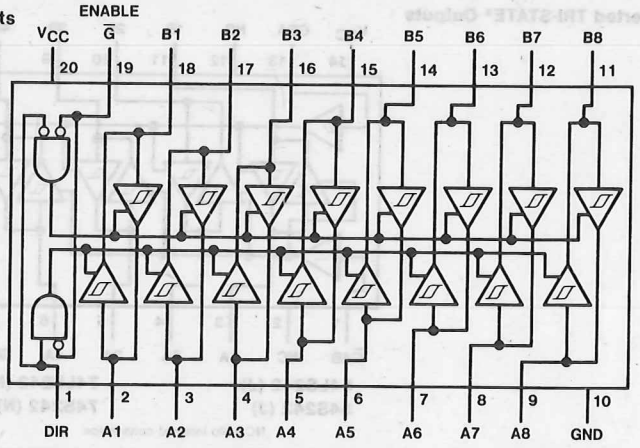



**54LS244 (J)** **74LS244 (N)**
**54S244 (J)** **74S244 (N)**

See page 5-53

## Octal Bus Tranceivers

### 245 Noninverted TRI-STATE® Outputs

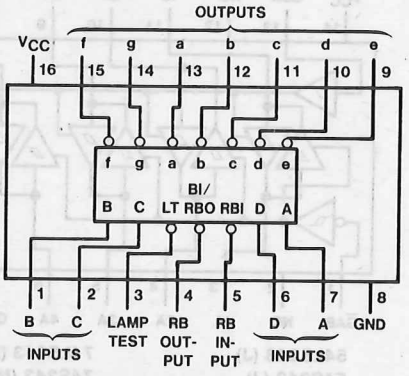



See page 5-60

54LS245 (J); 74LS245 (N)

## BCD-to-Seven-Segment Decoders/Drivers

### 247 Active-Low, Open-Collector, 15-V Outputs



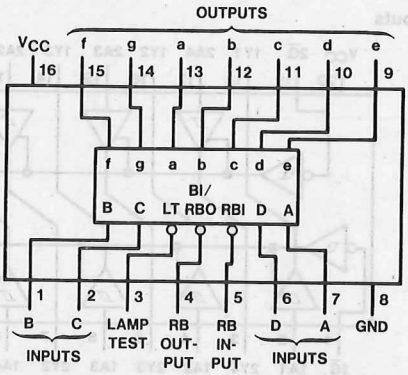

See page 6-184

54LS247 (J,W); 74LS247 (N)

## BCD-to-Seven-Segment Decoders/Drivers

### 248 Internal Pull-Up Outputs

### 249 Open-Collector Outputs




See page 6-184

54LS248 (J,W) 74LS248 (N)
54LS249 (J,W) 74LS249 (N)

Data Selectors/Multiplexers

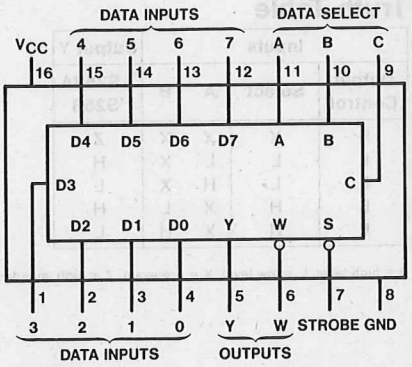
## 251 True and Inverted TRI-STATE® Outputs

### Truth Table

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| Select | | | Strobe | | |
| C | B | A | S | Y | W |
| X | X | X | H | Z | Z |
| L | L | L | L | D0 | $\overline{D0}$ |
| L | L | H | L | D1 | $\overline{D1}$ |
| L | H | L | L | D2 | $\overline{D2}$ |
| L | H | H | L | D3 | $\overline{D3}$ |
| H | L | L | L | D4 | $\overline{D4}$ |
| H | L | H | L | D5 | $\overline{D5}$ |
| H | H | L | L | D6 | $\overline{D6}$ |
| H | H | H | L | D7 | $\overline{D7}$ |

H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off)
D0, D1...D7 = the level of the respective D input

See page 6-190




54251 (J,W) 74251 (N)
54LS251 (J,W) 74LS251 (N)
54S251 (J,W) 74S251 (N)

Dual Data Selectors/Multiplexers

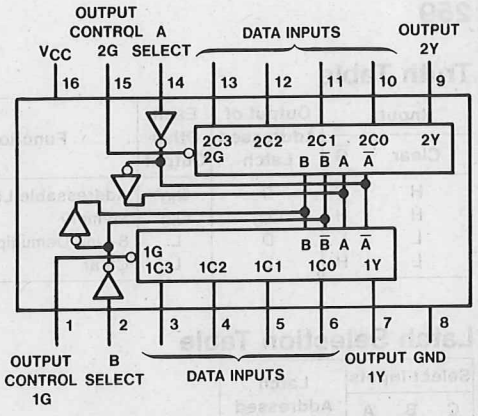
## 253 TRI-STATE Outputs

### Truth Table

| Select Inputs | | Data Inputs | | | | Output Control | Output |
|---|---|---|---|---|---|---|---|
| B | A | C0 | C1 | C2 | C3 | G | Y |
| X | X | X | X | X | X | H | Z |
| L | L | L | X | X | X | L | L |
| L | L | H | X | X | X | L | H |
| L | H | X | L | X | X | L | L |
| L | H | X | H | X | X | L | H |
| H | L | X | X | L | X | L | L |
| H | L | X | X | H | X | L | H |
| H | H | X | X | X | L | L | L |
| H | H | X | X | X | H | L | H |

Address inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

See page 6-194




54LS253 (J,W) 74LS253 (N)
54S253 (J,W) 74S253 (N)

Quad Data Selectors/Multiplexers

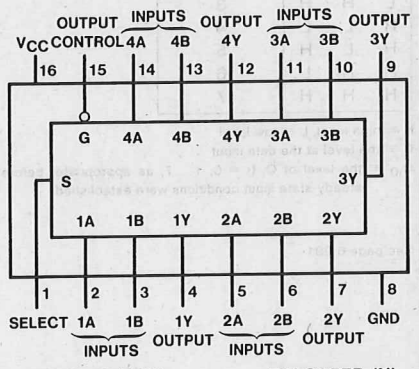
## 257 Noninverted TRI-STATE Outputs

### Truth Table

| Inputs | | | | Output Y |
|---|---|---|---|---|
| Output Control | Select | A | B | 'LS257A 'S257 |
| H | X | X | X | Z |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |

H = high level, L = low level, X = irrelevant, Z = high impedance, (off)

See page 6-197




54LS257B (J,W) 74LS257B (N)
54S257 (J,W) 74S257 (N)

Quad Data Selectors/Multiplexers

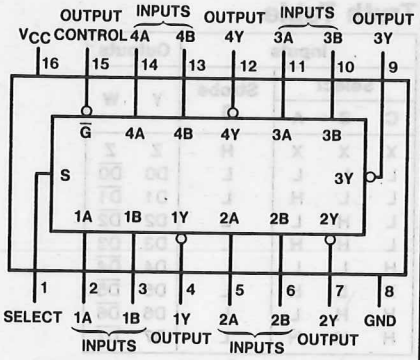
## 258 Inverted TRI-STATE® Outputs

### Truth Table

| Inputs | | | | Output Y |
|---|---|---|---|---|
| Output Control | Select | A | B | 'LS258A 'S258 |
| H | X | X | X | Z |
| L | L | L | X | H |
| L | L | H | X | L |
| L | H | X | L | H |
| L | H | X | H | L |

H = high level, L = low level, X = irrelevant, Z = high impedance, (off)

See page 6-197




54LS258B (J,W) 74LS258B (N)
54S258 (J,W) 74S258 (N)

Eight-Bit Addressable Latches

## 259

### Truth Table

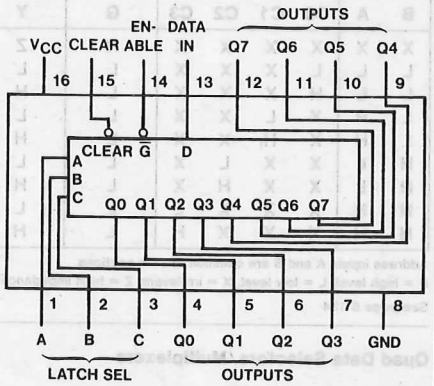
| Inputs | | Output of Addressed Latch | Each Other Output | Function |
|---|---|---|---|---|
| Clear | $\overline{G}$ | | | |
| H | L | D | $Q_{i0}$ | Addressable Latch |
| H | H | $Q_{i0}$ | $Q_{i0}$ | Memory |
| L | L | D | L | 8-Line Demultiplexer |
| L | H | L | L | Clear |

### Latch Selection Table

| Select Inputs | | | Latch Addressed |
|---|---|---|---|
| C | B | A | |
| L | L | L | 0 |
| L | L | H | 1 |
| L | H | L | 2 |
| L | H | H | 3 |
| H | L | L | 4 |
| H | L | H | 5 |
| H | H | L | 6 |
| H | H | H | 7 |

H = high level, L = low level
D = the level at the data input
$Q_{i0}$ = the level of $Q_i$ (i = 0, 1...7, as appropriate) before the indicated steady-state input conditions were established.

See page 6-201



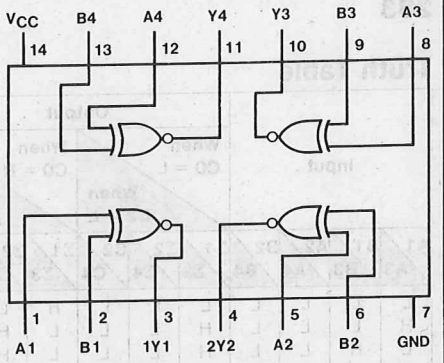

54LS259 (J,W) 74LS259 (N)
54259 (J,W) 74259 (N)

## 266 Quad EXCLUSIVE-NOR Gates with Open-Collector Outputs

### Truth Table

| Inputs A | Inputs B | Output Y |
|---|---|---|
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | H |

$Y = A \overline{\oplus} B = AB + \overline{A}\overline{B}$




54LS266 (J,W); 74LS266 (N)

See page 5-52

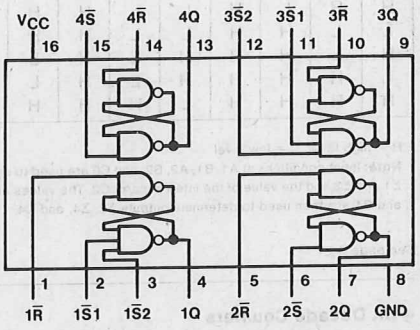
## Quad $\overline{S}$-$\overline{R}$ Latches

## 279

### Truth Table

| Inputs $\overline{S}$† | Inputs $\overline{R}$ | Output Q |
|---|---|---|
| H | H | $Q_0$ |
| L | H | H |
| H | L | L |
| L | L | H* |

H = high level
L = low level
$Q_0$ = the level of Q before the indicated input conditions were established.
*This output level is pseudo stable; that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level.
†For latches with double $\overline{S}$ inputs:
H = both $\overline{S}$ inputs high
L = one or both $\overline{S}$ inputs low




54LS279 (J,W); 74LS279 (N)

See page 5-63

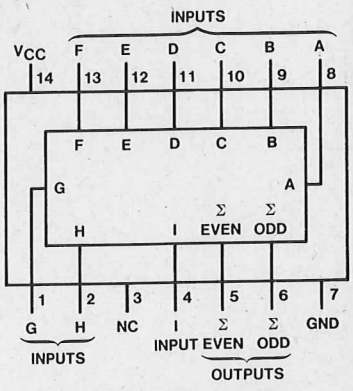
## 9-Bit Odd/Even Parity Generators/Checkers

## 280 N-Bit Cascadeable

### Truth Table

| Number of Inputs A Thru I That Are High | Outputs Σ Even | Outputs Σ Odd |
|---|---|---|
| 0, 2, 4, 6, 8 | H | L |
| 1, 3, 5, 7, 9 | L | H |

H = high level, L = low level




54S280 (J,W); 74S280 (N)

See page 6-204

**4-Bit Binary Full Adders**

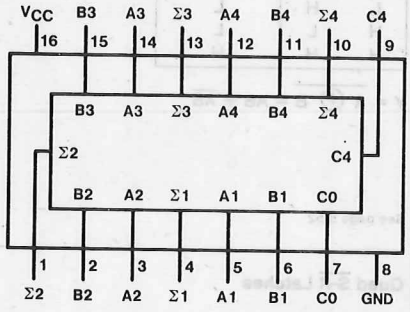
## 283

### Truth Table

| Input | | | | Output | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | When C0 = L | | | When C0 = H | | |
| | | | | When C2 = L | | | When C2 = H | | |
| A1 / A3 | B1 / B3 | A2 / A4 | B2 / B4 | Σ1 / Σ3 | Σ2 / Σ4 | C2 / C4 | Σ1 / Σ3 | Σ2 / Σ4 | C2 / C4 |
| L | L | L | L | L | L | L | H | L | L |
| H | L | L | L | H | L | L | L | H | L |
| L | H | L | L | H | L | L | L | H | L |
| H | H | L | L | L | H | L | H | H | L |
| L | L | H | L | L | H | L | H | H | L |
| H | L | H | L | H | H | L | L | L | H |
| L | H | H | L | H | H | L | L | L | H |
| H | H | H | L | L | L | H | H | L | H |
| L | L | L | H | L | H | L | H | H | L |
| H | L | L | H | H | H | L | L | L | H |
| L | H | L | H | H | H | L | L | L | H |
| H | H | L | H | L | L | H | H | L | H |
| L | L | H | H | L | L | H | H | L | H |
| H | L | H | H | H | L | H | L | H | H |
| L | H | H | H | H | L | H | L | H | H |
| H | H | H | H | L | H | H | H | H | H |

H = high level, L = low level

**Note:** Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.



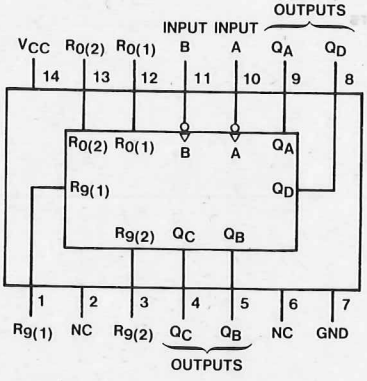

**54LS283 (J,W)**
**54S283 (J,W)**

**74LS283 (N)**
**74S283 (N)**

See page 6-21

**4-Bit Decade Counters**

## 290 Divide-by-Two and Divide-by-5



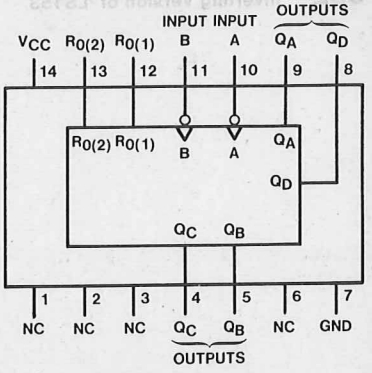

**54LS290 (J,W); 74LS290 (N)**

NC—no internal connection

See page 6-207

4-Bit Binary Counters

## 293 Divide-by-Two and Divide-by-Eight




54LS293 (J,W); 74LS293 (N)

NC—no internal connection

See page 6-207

Quad 2-Input Multiplexers With Storage

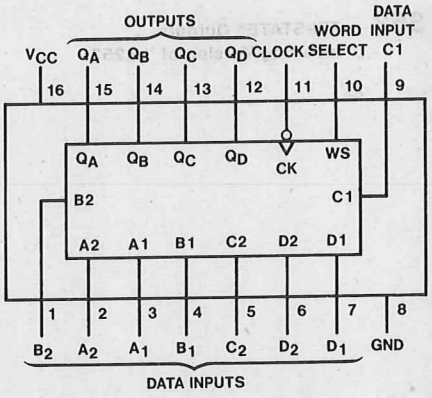
## 298

## Truth Table

| Inputs | | Outputs | | | |
|---|---|---|---|---|---|
| Word Select | Clock | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| L | ↓ | a1 | b1 | c1 | d1 |
| H | ↓ | a2 | b2 | c2 | d2 |
| X | H | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
a1, a2, etc. = the level of steady-state input at A1, A2, etc.
$Q_{A0}$, $Q_{B0}$, etc. = the level of $Q_A$, $Q_B$, etc. entered on the most-recent ↓ transition of the clock input.

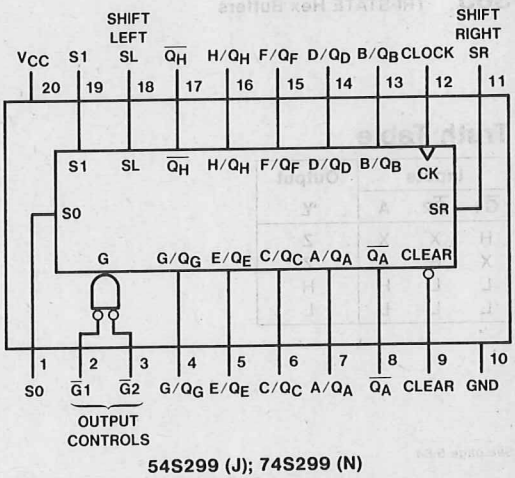
See page 6-211




54LS298 (J,W); 74LS298 (N)

8-Bit Bidirectional Universal Shift/Storage Registers

## 299 TRI-STATE® Outputs

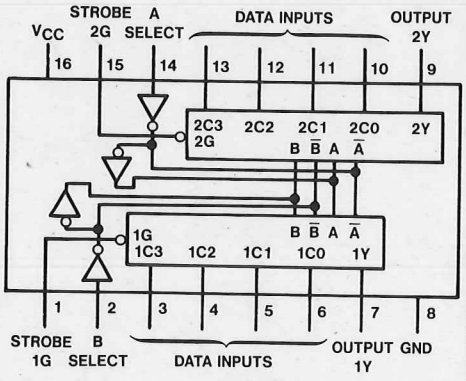



54S299 (J); 74S299 (N)

See page 6-214

**Dual 4-Line-to-1-Line Data Selectors/Multiplexers**

## 352 Inverting Version of 'LS153

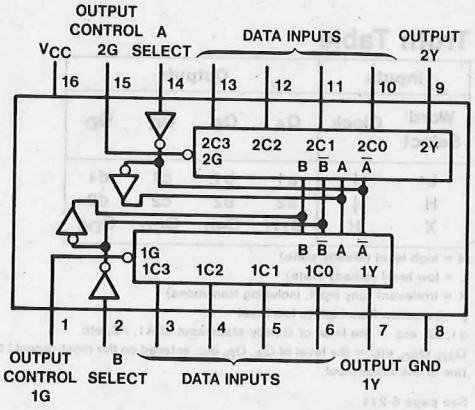



54LS352 (J,W); 74LS352 (N)

See page 6-220

**Dual 4-Line-to-1-Line Data Selectors/Multiplexers**

## 353 TRI-STATE® Outputs Inverting Version of 'LS253



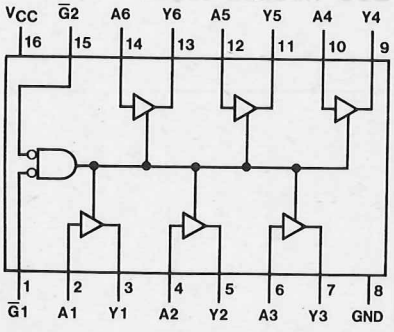

54LS353 (J,W); 74LS353 (N)

See page 6-222

## 365 TRI-STATE Hex Buffers

### Truth Table

| Inputs | | | Output |
|---|---|---|---|
| $\overline{G}1$ | $\overline{G}2$ | A | Y |
| H | X | X | Z |
| X | H | X | Z |
| L | L | H | H |
| L | L | L | L |




54365 (J,W)
54LS365A (J,W)

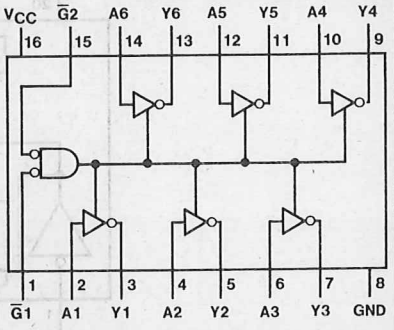
74365 (N)
74LS365A (N)

See page 5-64

## 366 TRI-STATE® Hex Inverting Buffers

### Truth Table

| Inputs | | | Output |
|---|---|---|---|
| $\overline{G}1$ | $\overline{G}2$ | A | Y |
| H | X | X | Z |
| X | H | X | Z |
| L | L | H | L |
| L | L | L | H |



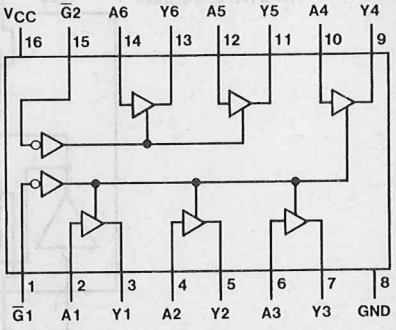

54366 (J,W) 74366 (N)
54LS366A (J,W) 74LS366A (N)

See page 5-64

## 367 TRI-STATE Hex Buffers

### Truth Table

| Inputs | | Output |
|---|---|---|
| $\overline{G}$ | A | Y |
| H | X | Z |
| L | H | H |
| L | L | L |



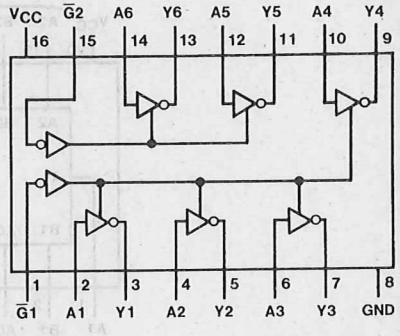

54367 (J,W) 74367 (N)
54LS367A (J,W) 74LS367A (N)

See page 5-64

## 368 TRI-STATE Hex Inverting Buffers

### Truth Table

| Inputs | | Output |
|---|---|---|
| $\overline{G}$ | A | Y |
| H | X | Z |
| L | H | L |
| L | L | H |

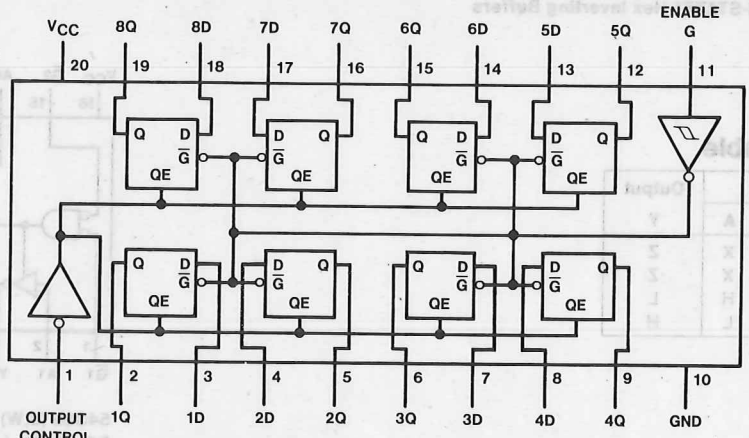



54368 (J,W) 74368 (N)
54LS368A (J,W) 74LS368A (N)

See page 5-64

## Octal D-Type Latches

### 373 TRI-STATE® Outputs



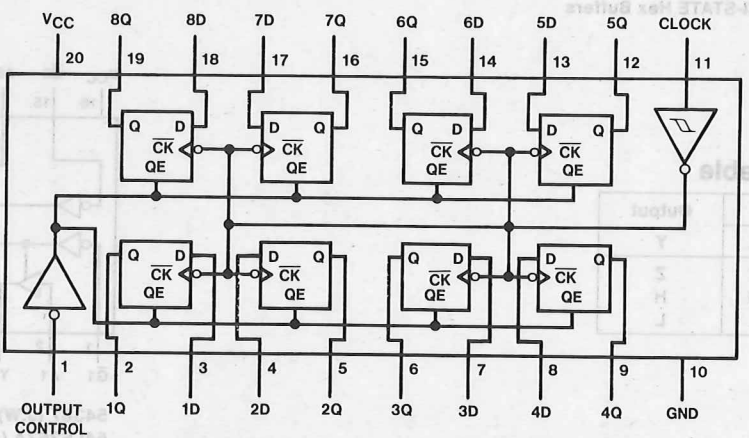

54LS373 (J)
54S373 (J)

74LS373 (N)
74S373 (N)

See page 6-225

## Octal D-Type Flip-Flops

### 374 TRI-STATE Outputs



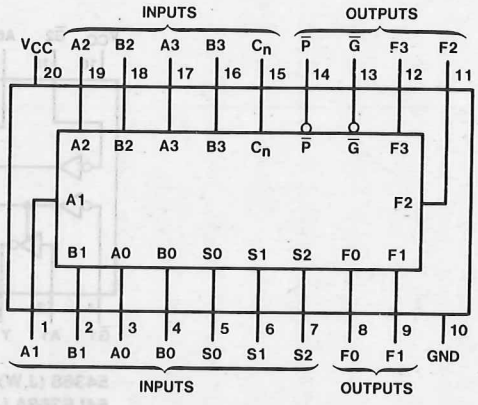

54LS374 (J)
54S374 (J)

74LS374 (N)
74S374 (N)

See page 6-225

## Arithmetic Logic Units/Function Generators

### 381

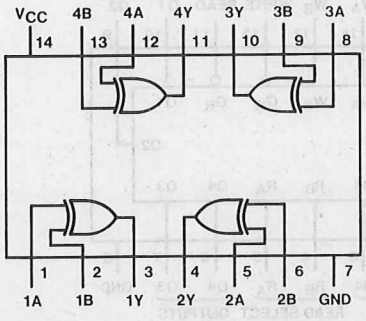



54S381 (J); 74S381 (N)

See page 6-230

**Quad 2-Input Exclusive-OR Gates**

## 386




**Positive Logic:**

$Y = A \oplus B = \overline{A}B + A\overline{B}$

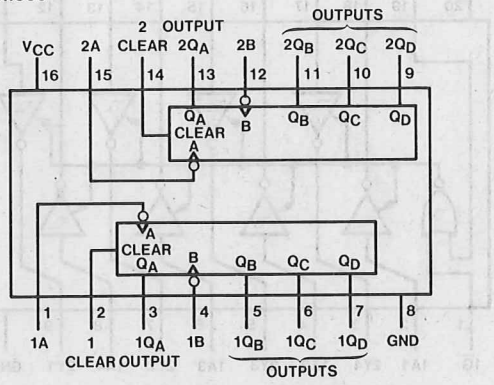
**54LS386 (J,W); 74LS386 (N)**

See page 5-40

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**Dual Decade Counters**

## 390 Bi-Quinary or BCD Sequences



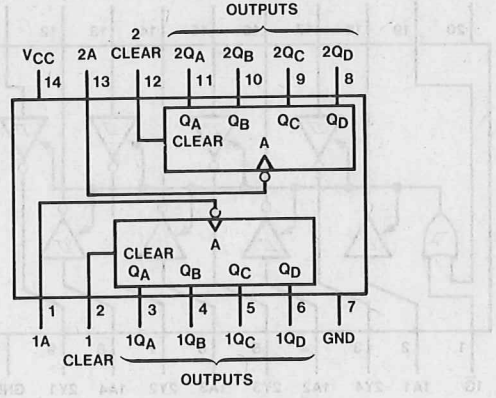

See page 6-234

**54LS390 (J,W); 74LS390 (N)**

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**Dual 4-Bit Binary Counters**

## 393

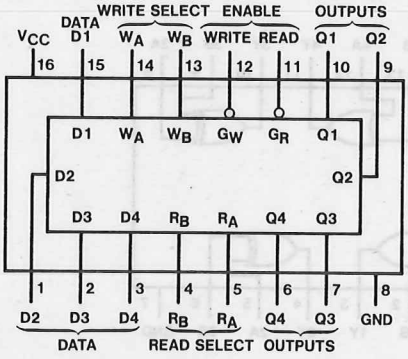



See page 6-234

**54LS393 (J,W); 74LS393 (N)**

**4-by-4 Register Files**

## 670 TRI-STATE® Outputs

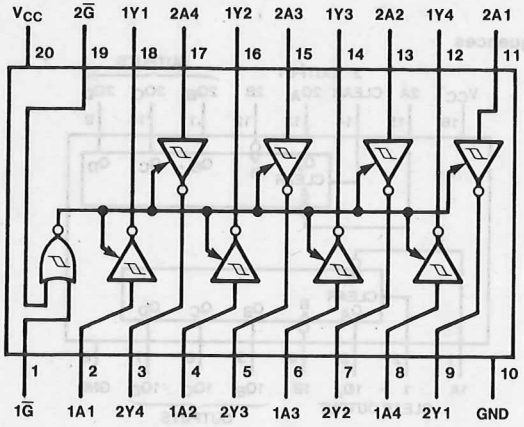



See page 6-239

54LS670 (J,W); 74LS670 (N)

**Buffers/Line Drivers/Line Receivers**

## 940 Octal TRI-STATE®

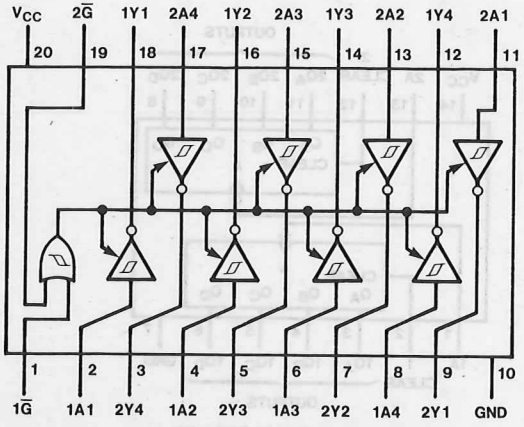



See page 5-53

54S940 (J); 74S940 (N)

**Buffers/Line Drivers/Line Receivers**

## 941 Octal TRI-STATE®

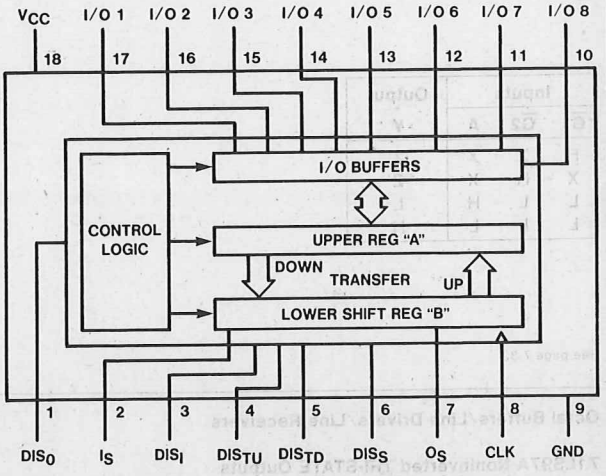



See page 5-53

54S941 (J); 74S941 (N)

**Dual Rank 8-Bit TRI-STATE Shift Register**

**952 Synchronous Clear**
**962 Exchange Data Between Registers A & B**




54LS952 (J)
54LS962 (J)

74LS952 (N)
74LS962 (N)

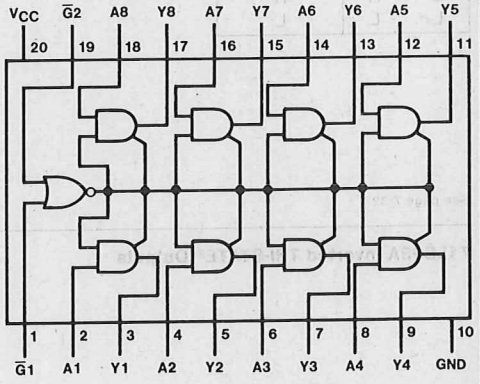
See page 6-243

3

**Octal Buffers/Line Drivers/Line Receivers**

**71LS95A Noninverted TRI-STATE® Outputs**

| Inputs | | | Output |
|---|---|---|---|
| $\overline{G}1$ | $\overline{G}2$ | A | Y |
| H | X | X | Z |
| X | H | X | Z |
| L | L | H | H |
| L | L | L | L |




71LS95A (J); 81LS95A (N)

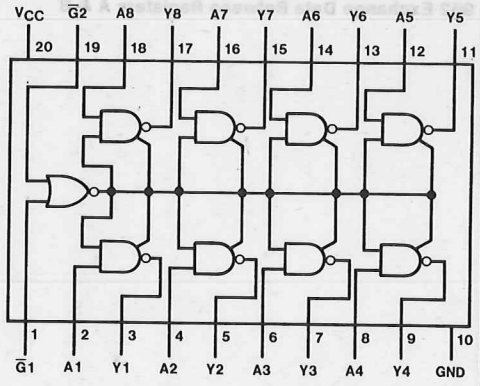
See page 7-32

## Octal Buffers/Line Drivers/Line Receivers

### 71LS96A Inverted TRI-STATE Outputs

| Inputs | | | Output |
|---|---|---|---|
| $\overline{G}1$ | $\overline{G}2$ | A | Y |
| H | X | X | Z |
| X | H | X | Z |
| L | L | H | L |
| L | L | L | H |

See page 7-32



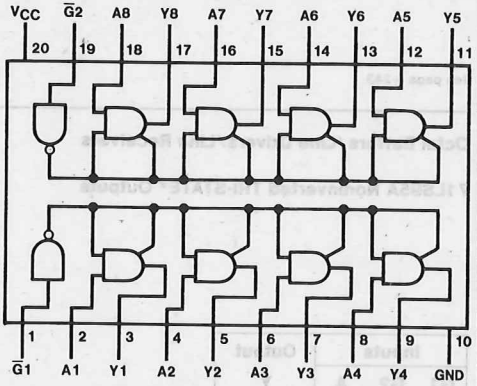

71LS96A (J); 81LS96A (N)

## Octal Buffers/Line Drivers/Line Receivers

### 71LS97A Noninverted TRI-STATE Outputs

| Inputs | | Output |
|---|---|---|
| $\overline{G}$ | A | Y |
| H | X | Z |
| L | H | H |
| L | L | L |

See page 7-32

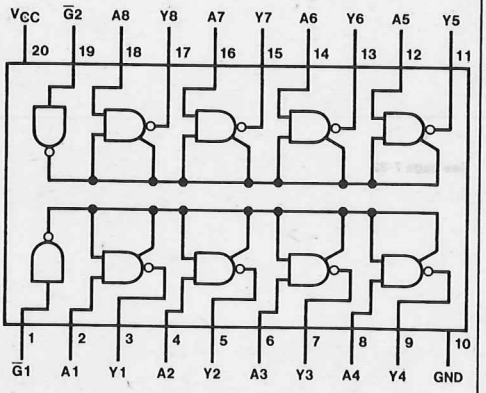



71LS97A (J); 81LS97A (N)

### 71LS98A Inverted TRI-STATE® Outputs

| Inputs | | Output |
|---|---|---|
| $\overline{G}$ | A | Y |
| H | X | Z |
| L | H | L |
| L | L | H |

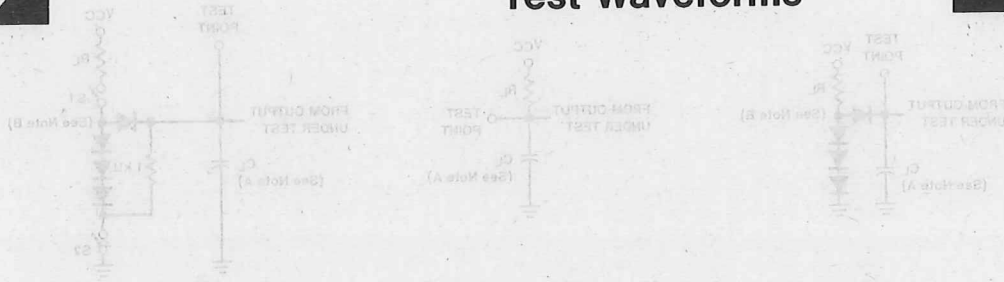
See page 7-32



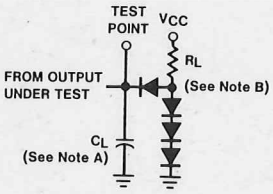

71LS98A (J); 81LS98A (N)

# Test Waveforms

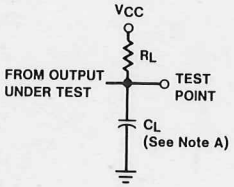




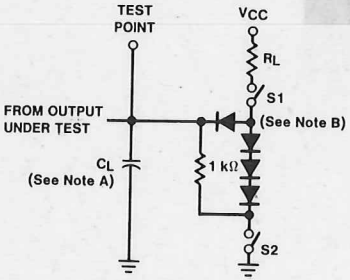
## Parameter Measurement Information




**Load Circuit for Bi-State Totem-Pole Outputs**

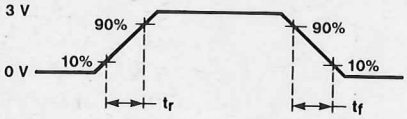



**Load Circuit for Open-Collector Outputs**




**Load Circuit for TRI-STATE® Outputs**

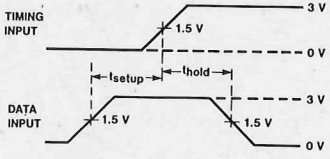
**Note A.** $C_L$ includes probe and jig capacitance.
**Note B.** All diodes are 1N916 or 1N3064.



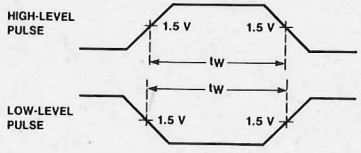

**Input Waveform**

**54/74 $t_r \leq 7$ ns, $t_f \leq 7$ ns**
**54H/74H $t_r \leq 7$ ns, $t_f \leq 7$ ns**
**54S/74S $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns**

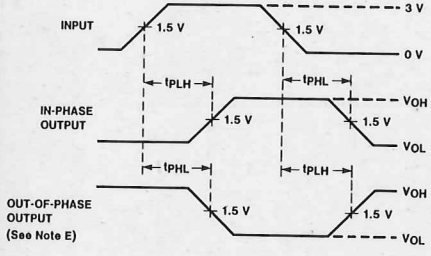
**Generator: Zout $\approx 50\ \Omega$**
**PRR $\leq$ 1 MHz**



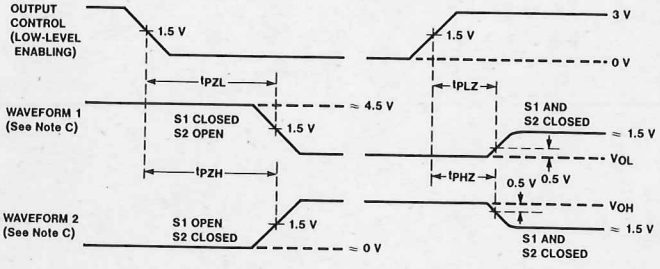

**Voltage Waveforms Setup and Hold Times**




**Voltage Waveforms Pulse Widths**



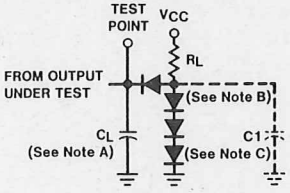

**Voltage Waveforms Propagation Delay Times**



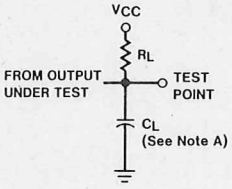

**Voltage Waveforms Enable and Disable Times, TRI-STATE® Outputs**

**Note C.** Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
**Note D.** In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
**Note E.** When measuring propagation delay times of Tri-state outputs, switches S1 and S2 are closed.

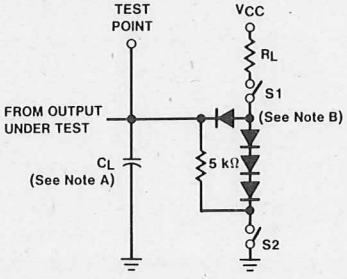
## Parameter Measurement Information




Load Circuit for Bi-State Totem-Pole Outputs

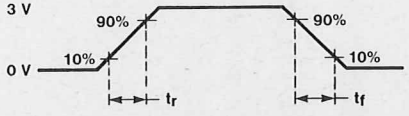



Load Circuit for Open-Collector Outputs




Load Circuit for TRI-STATE® Outputs

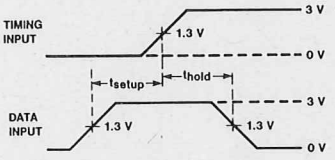
**Note A.** $C_L$ includes probe and jig capacitance.
**Note B.** All diodes are 1N916 or 1N3064.
**Note C.** C1 (30 pF) is used for testing Series 54L/74L devices only.



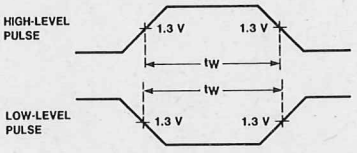

Input Waveform

**54LS/74LS: $t_r \leq 6$ ns, $t_f \leq 6$ ns**
**54L/74L gates and inverters: $t_r \leq 60$ ns, $t_f \leq 60$ ns**
**54L/74L flip-flops and MSI: $t_r \leq 25$ ns, $t_f \leq 25$ ns**

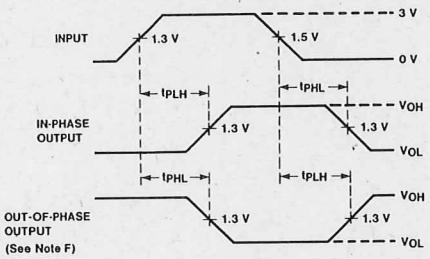
**Generator: Zout ≈ 50 Ω**
**PRR ≤ 1 MHz**



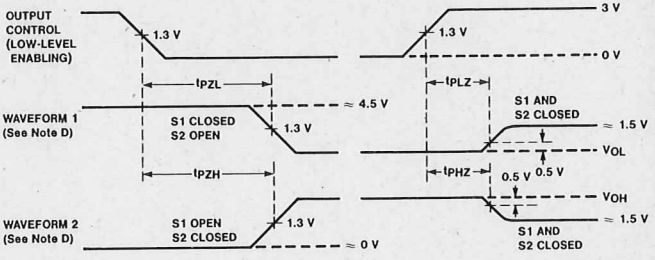

Voltage Waveforms Setup and Hold Times




Voltage Waveforms Pulse Widths



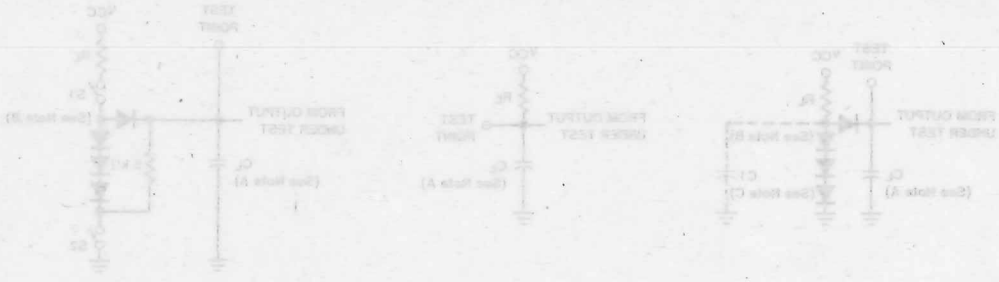

Voltage Waveforms Propagation Delay Times




Voltage Waveforms Enable and Disable Times, TRI-STATE® Outputs

**Note D.** Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
**Note E.** In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
**Note F.** When measuring propagation delay times of Tri-state outputs, switches S1 and S2 are closed.

## Parameter Measurement Information



Load Circuit for Totem-Pole Outputs

Load Circuit for Open-Collector Outputs

Load Circuit for 3-STATE and Open-Collector Outputs

Note A: $C_L$ includes probe and jig capacitance.

Note B: All diodes are 1N3064 or 1N3600.

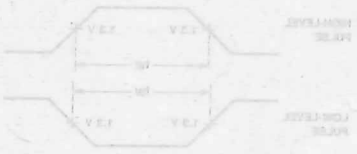
Note C: $C_1$ (50 pF) is used for testing Series 54L/74L devices only.



Input Waveform

54LS/74LS: $t_r \leq 8$ ns, $t_f \leq 8$ ns
54L/74L gates and inverters: $t_r \leq 60$ ns, $t_f \leq 60$ ns
54L/74L flip-flops and MSI: $t_r \leq 25$ ns, $t_f \leq 25$ ns

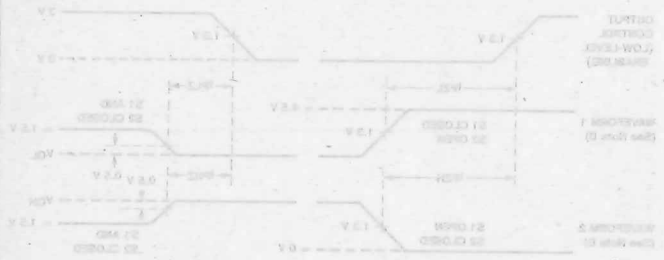
Generator: $Z_{out} \approx 50\ \Omega$
PRR $\leq$ 1 MHz



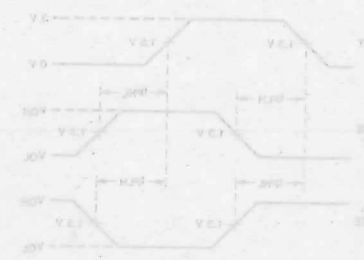
Voltage Waveforms
Pulse Widths



Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Enable and Disable Times, 3-STATE Outputs



Voltage Waveforms
Propagation Delay Times

Note D: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Note E: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Note F: Worst-case propagation delay times (or enable outputs, switches S1 and S2 are closed.

# Section 5
# 54/74 SSI Device Specifications

5


| TEMPERATURE RANGE −55°C to +125°C | TEMPERATURE RANGE 0°C to +70°C | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| DM5400 (H, L, LS, S) | DM7400 (H, L, LS, S) | Quad 2-Input NAND Gates | 5-4 |
| DM5401 (H, L, LS) | DM7401 (H, L, LS) | Quad 2-Input NAND Gates with Open-Collector Outputs | 5-6 |
| DM5402 (L, LS, S) | DM7402 (L, LS, S) | Quad 2-Input NOR Gates | 5-8 |
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| DM5409 (L, LS, S) | DM7409 (L, LS, S) | Quad 2-Input AND Gates with Open-Collector Outputs | 5-14 |
| DM5410 (H, L, LS, S) | DM7410 (H, L, LS, S) | Triple 3-Input NAND Gates | 5-4 |
| DM5411 (H, L, LS, S) | DM7411 (H, L, LS, S) | Triple 3-Input AND Gates | 5-12 |
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| DM5414 (LS) | DM7414 (LS) | Hex Schmitt Triggers | 5-16 |
| DM54LS15 (S) | DM74LS15 (S) | Triple 3-Input AND Gates with Open-Collector Outputs | 5-14 |
| DM5416 | DM7416 | Hex Buffers with Open Collector High-Voltage Outputs | 5-10 |
| DM5417 | DM7417 | Hex Buffers with Open Collector High-Voltage Outputs | 5-10 |
| DM5420 (H, L, LS, S) | DM7420 (H, L, LS, S) | Dual 4-Input NAND Gates | 5-4 |
| DM54H21 (LS) | DM74H21 (LS) | Dual 4-Input AND Gates | 5-12 |
| DM54LS22 (S) | DM74LS22 (S) | Dual 4-Input NAND Gates with Open-Collector Outputs | 5-6 |
| DM5423 | DM7423 | Expandable Dual 4-Input NOR Gates | 5-18 |
| DM5425 | DM7425 | Dual 4-Input NOR Gates | 5-8 |
| DM5426 (L, LS) | DM7426 (L, LS) | Quad 2-Input High Voltage NAND Gates | 5-10 |
| DM5427 (LS) | DM7427 (LS) | Triple 3-Input NOR Gates | 5-8 |
| DM5430 (H, L, LS, S) | DM7430 (H, L, LS, S) | 8-Input NAND Gates | 5-4 |
| DM5432 (L, LS, S) | DM7432 (L, LS, S) | Quad 2-Input OR Gates | 5-20 |
| DM5437 (LS) | DM7437 (LS) | Quad 2-Input NAND Buffers | 5-22 |
| DM5438 (LS) | DM7438 (LS) | Quad 2-Input NAND Buffers with Open-Collector Outputs | 5-10 |
| DM5440 (H, LS, S) | DM7440 (H, LS, S) | Dual 4-Input NAND Buffers | 5-22 |
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| DM5451 (L, LS, S) | DM7451 (L, LS, S) | Dual 2-Wide 2-Input AND-OR-INVERT Gates | 5-24 |
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| DM5474 | DM7474 | Dual D Positive-Edge-Triggered Flip-Flops with Preset and Clear | 5-29 |
| DM54H74 | DM74H74 | Dual D Positive-Edge-Triggered Flip-Flops with Preset and Clear | 5-38 |

| TEMPERATURE RANGE −55°C to +125°C | TEMPERATURE RANGE 0°C to +70°C | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
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| DM54L86 | DM74L86 | Quad EXCLUSIVE-OR Gates | 5-40 |
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| DM54S113 | DM74S113 | Dual J-K Negative-Edge-Triggered Flip Flops with Preset | 5-35 |
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| DM54S114 | DM74S114 | Dual J-K Negative-Edge-Triggered Flip Flops with Preset, Common Clear and Common Clock | 5-35 |
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| DM54L123A | DM74L123A | Dual Retriggerable One Shots with Clear | 5-46 |
| DM54LS123 | DM74LS123 | Dual Retriggerable One Shots with Clear | 5-46 |
| DM54125 | DM74125 | TRI-STATE® Quad Buffers | 5-48 |
| DM54LS125A | DM74LS125A | TRI-STATE Quad Buffers | 5-48 |
| DM54126 | DM74126 | TRI-STATE Quad Buffers | 5-48 |
| DM54LS126A | DM74LS126A | TRI-STATE Quad Buffers | 5-48 |
| DM54132 (LS) | DM74132 (LS) | Quad 2-Input NAND Schmitt Triggers | 5-16 |
| DM54S133 | DM74S133 | 13-Input NAND Gates | 5-4 |
| DM54S134 | DM74S134 | TRI-STATE 12-Input NAND Gates | 5-48 |
| DM54S135 | DM74S135 | Quad EXCLUSIVE-OR/NOR Gates | 5-50 |
| DM54LS136 | DM74LS136 | Quad EXCLUSIVE-OR Gates with Open-Collector Outputs | 5-52 |
| DM54S136 | DM74S136 | Quad EXCLUSIVE-OR Gates with Open-Collector Outputs | 5-52 |
| DM54S140 | DM74S140 | Dual 50-Ohm Line Drivers | 5-22 |
| DM54LS221 | DM74LS221 | Dual One Shots with Schmitt-Trigger Inputs | 5-44 |
| DM54LS240 | DM74LS240 | Octal TRI-STATE Buffers/Line Drivers/Line Receivers | 5-53 |
| DM54S240 | DM74S240 | Octal TRI-STATE Buffers/Line Drivers/Line Receivers | 5-53 |
| DM54LS241 | DM74LS241 | Octal TRI-STATE Buffers/Line Drivers/Line Receivers | 5-53 |
| DM54S241 | DM74S241 | Octal TRI-STATE Buffers/Line Drivers/Line Receivers | 5-53 |
| DM54LS242 | DM74LS242 | Quad Bus Transceivers | 5-57 |
| DM54S242 | DM74S242 | Quad Bus Transceivers | 5-57 |
| DM54LS243 | DM74LS243 | Quad Bus Transceivers | 5-57 |
| DM54S243 | DM74S243 | Quad Bus Transceivers | 5-57 |

| TEMPERATURE RANGE −55°C to +125°C | TEMPERATURE RANGE 0°C to +70°C | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| DM54LS244 | DM74LS244 | Octal TRI-STATE® Buffers/Line Drivers/Line Receivers | 5-53 |
| DM54S244 | DM74S244 | Octal TRI-STATE Buffers/Line Drivers/Line Receivers | 5-53 |
| DM54LS245 | DM74LS245 | Octal Bus Transceiver | 5-60 |
| DM54LS266 | DM74LS266 | Quad EXCLUSIVE-NOR Gates with Open-Collector Outputs | 5-52 |
| DM54LS279 | DM74LS279 | Quad $\overline{S}$-$\overline{R}$ Latches | 5-63 |
| DM54365 (LS) | DM74365 (LS) | TRI-STATE Hex Buffers | 5-64 |
| DM54366 (LS) | DM74366 (LS) | TRI-STATE Hex Buffers | 5-64 |
| DM54367 (LS) | DM74367 (LS) | TRI-STATE Hex Buffers | 5-64 |
| DM54368 (LS) | DM74368 (LS) | TRI-STATE Hex Buffers | 5-64 |
| DM54LS386 | DM74LS386 | Quad EXCLUSIVE-OR Gates | 5-40 |
| DM54S940 | DM74S940 | Octal TRI-STATE Buffers/Line Drivers/Line Receivers | 5-53 |
| DM54S941 | DM74S941 | Octal TRI-STATE Buffers/Line Drivers/Line Receivers | 5-53 |

## Max Ratings/Operating Conditions

| Ratings | | 54/74 Series | 54H/74H Series | 54L/74L Series | 54LS/74LS Series | 54S/74S Series | Units |
|---|---|---|---|---|---|---|---|
| Maximum Allowable Supply Voltage | | 7 | 7 | 8 | 7 | 7 | V |
| Guaranteed Operating Supply Voltage Range | 54 | 4.50 to 5.50 | | | | | V |
| | 74 | 4.75 to 5.25 | | | | | |
| Maximum Input Voltage | | 5.5 | 5.5 | 5.5 | 7 | 5.5 | V |
| Maximum Voltage to Open-Collector Outputs* | | 7 | 7 | 8 | 7 | 7 | V |
| Operating Free-Air Temperature Range | 54 | −55 to +125 | | | | | °C |
| | 74 | 0 to +70 | | | | | |
| Storage Temperature Range | | −65 to +150 | | | | | °C |

* Except for selected high voltage types.

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## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

| Parameter | | Conditions | | | DM54/74 00, 04 10, 20, 30 | | | DM54/74 H00, H04 H10, H20, H30 | | | DM54/74 L00, L04 L10, L20, L30 | | | DM54/74 LS00, LS04 LS10, LS20, LS30 | | | DM54/74 S00, S04, S10 S20, S30, S133 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ(1) | Max | Min | Typ(1) | Max | Min | Typ(1) | Max | Min | Typ(1) | Max | Min | Typ(1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.8 | | | 0.7 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.7 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −8 mA | | | | | | | −1.5 | | | N/A | | | | | | | V |
| | | | $I_I$ = −12 mA | | | | −1.5 | | | | | | N/A | | | | | | | |
| | | | $I_I$ = −18 mA | | | | | | | | | | N/A | | | −1.5 | | | −1.2 | |
| $I_{OH}$ | High Level Output Current | | | | | | −400 | | | −500 | | | −200 | | | −400 | | | −1000 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.4 | 3.4 | | 2.4 | 3.5 | | 2.4 | 3.3 | | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.4 | 3.4 | | 2.4 | 3.5 | | 2.4 | 3.2 | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | | | 20 | | | 2 | | | 4 | | | 20 | mA |
| | | | | DM74 | | | 16 | | | 20 | | | 3.6 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.15 | 0.3 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | DM74 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 4 mA | DM74 | | | | | | | | | | | | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | 1 | | | 0.1 | | | | | | 1 | mA |
| | | | $V_I$ = 7 V | | | | | | | | | | | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | 50 | | | 10 | | | | | | | μA |
| | | | $V_I$ = 2.7 V | | | | | | | | | | | | | 20 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | | | | | | −0.18 | | | | | | | mA |
| | | | $V_I$ = 0.4 V | LS30 | | | | | | | | | | | | −0.4 | | | | |
| | | | | Others | | | −1.6 | | | −2 | | | | | | −0.36 | | | | |
| | | | $V_I$ = 0.5 V | | | | | | | | | | | | | | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −20 | | −55 | −40 | | −100 | −3 | | −15 | −20 | | −100 | −40 | | −100 | mA |
| | | | | DM74 | −18 | | −55 | −40 | | −100 | −3 | | −15 | −20 | | −100 | −40 | | −100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | See Table | | | | | | | | | | | | | | | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54H/DM74H, DM54LS/DM74LS and DM54S/DM74S, duration of short circuit should not exceed one second.

## Supply Currents

| Device | $I_{CCH}$ (mA) Total With Outputs High | | $I_{CCL}$ (mA) Total With Outputs Low | |
|---|---|---|---|---|
| | Typ | Max | Typ | Max |
| 00 | 4 | 8 | 12 | 22 |
| 04 | 6 | 12 | 18 | 33 |
| 10 | 3 | 6 | 9 | 16.5 |
| 20 | 2 | 4 | 6 | 11 |
| 30 | 1 | 2 | 3 | 6 |
| H00 | 10 | 16.8 | 26 | 40 |
| H04 | 16 | 26 | 40 | 58 |
| H10 | 7.5 | 12.6 | 19.5 | 30 |
| H20 | 5 | 8.4 | 13 | 20 |
| H30 | 2.5 | 4.2 | 6.5 | 10 |
| L00 | 0.44 | 0.8 | 1.16 | 2.04 |
| L04 | 0.60 | 1.2 | 1.74 | 3.06 |
| L10 | 0.33 | 0.6 | 0.87 | 1.53 |
| L20 | 0.22 | 0.4 | 0.58 | 1.02 |
| L30 | 0.11 | 0.2 | 0.29 | 0.51 |
| LS00 | 0.8 | 1.6 | 2.4 | 4.4 |
| LS04 | 1.2 | 2.4 | 3.6 | 6.6 |
| LS10 | 0.6 | 1.2 | 1.8 | 3.3 |
| LS20 | 0.4 | 0.8 | 1.2 | 2.2 |
| LS30 | 0.35 | 0.5 | 0.6 | 1.1 |
| S00 | 10 | 16 | 20 | 36 |
| S04 | 15 | 24 | 30 | 54 |
| S10 | 7.5 | 12 | 15 | 27 |
| S20 | 5 | 8 | 10 | 18 |
| S30 | 3 | 5 | 5.5 | 10 |
| S133 | 3 | 5 | 5.5 | 10 |

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Device | Conditions | $t_{PLH}$ (ns) Propagation Delay Time, Low-To-High Output | | | $t_{PHL}$ (ns) Propagation Delay Time, High-To-Low Output | | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max |
| 00, 10 | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 11 | 22 | | 7 | 15 |
| 04, 20 | | | 12 | 22 | | 8 | 15 |
| 30 | | | 13 | 22 | | 8 | 15 |
| H00 | $C_L$ = 25 pF, $R_L$ = 280 Ω | | 5.9 | 10 | | 6.2 | 10 |
| H04 | | | 6 | 10 | | 6.5 | 10 |
| H10 | | | 5.9 | 10 | | 6.3 | 10 |
| H20 | | | 6 | 10 | | 7 | 10 |
| H30 | | | 6.8 | 10 | | 8.9 | 12 |
| L00, L04 L10, L20 | $C_L$ = 50 pF, $R_L$ = 4 kΩ | | 35 | 60 | | 31 | 60 |
| L30 | | | 35 | 60 | | 70 | 100 |
| LS00, LS04 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 3 | 5 | 10 | 3 | 5 | 10 |
| LS10, LS20 | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 4 | 8 | 15 | 4 | 8 | 15 |
| LS30 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 4 | 7 | 12 | 4 | 7 | 15 |
| | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 5 | 9 | 18 | 5 | 11 | 20 |
| S00, S04 | $C_L$ = 15 pF, $R_L$ = 280 Ω | 2 | 3 | 4.5 | 2 | 3 | 5 |
| S10, S20 | $C_L$ = 50 pF, $R_L$ = 280 Ω | 2 | 4.5 | 7 | 2 | 5 | 8 |
| S30, S133 | $C_L$ = 15 pF, $R_L$ = 280 Ω | 2 | 4 | 6 | 2 | 4.5 | 7 |
| | $C_L$ = 50 pF, $R_L$ = 280 Ω | 2 | 5.5 | 8 | 3 | 6.5 | 10 |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 01, 03 05 | | | DM54/74 H01 | | | DM54/74 L01, L03 L05 | | | DM54/74 LS01, LS03 LS05, LS12, LS22 | | | DM54/74 S03 S05, S22 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.8 | | | 0.6 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.6 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −8 mA | | | | | | | −1.5 | | | N/A | | | | | | | V |
| | | | $I_I$ = −12 mA | | | | −1.5 | | | | | | N/A | | | | | | | |
| | | | $I_I$ = −18 mA | | | | | | | | | | N/A | | | −1.5 | | | −1.2 | |
| $I_{CEX}$ | High Level Output Current | $V_{CC}$ = Min, $V_{IL}$ = Max, $V_{OH}$ = 5.5 V | | | | | 250 | | | 250 | | | 50 | | | 100 | | | 250 | μA |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | | | 20 | | | 2 | | | 4 | | | 20 | mA |
| | | | | DM74 | | | 16 | | | 20 | | | 3.6 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.15 | 0.3 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | DM74 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 4 mA | DM74 | | | | | | | | | | | | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | 1 | | | 0.1 | | | | | | 1 | mA |
| | | | $V_I$ = 7 V | | | | | | | | | | | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | 50 | | | 10 | | | | | | | μA |
| | | | $V_I$ = 2.7 V | | | | | | | | | | | | | 20 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | | | | | | −0.18 | | | | | | | mA |
| | | | $V_I$ = 0.4 V | | | | −1.6 | | | −2 | | | | | | −0.36 | | | | |
| | | | $V_I$ = 0.5 V | | | | | | | | | | | | | | | | −2 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | See Table | | | | | | | | | | | | | | | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C

## Supply Current

| Device | $I_{CCH}$ (mA) Total With Outputs High | | $I_{CCL}$ (mA) Total With Outputs Low | |
|---|---|---|---|---|
| | Typ | Max | Typ | Max |
| 01 | 4 | 8 | 12 | 22 |
| 03 | 4 | 8 | 12 | 22 |
| 05 | 6 | 12 | 18 | 33 |
| H01 | 6.8 | 10 | 26 | 40 |
| L01 | 0.44 | 0.8 | 1.16 | 2.04 |
| L03 | 0.44 | 0.8 | 1.16 | 2.04 |
| L05 | 0.66 | 1.20 | 1.74 | 3.06 |
| LS01 | 0.8 | 1.6 | 2.4 | 4.4 |
| LS03 | 0.8 | 1.6 | 2.4 | 4.4 |
| LS05 | 1.2 | 2.4 | 3.6 | 6.6 |
| LS12 | 0.7 | 1.4 | 1.8 | 3.3 |
| LS22 | 0.4 | 0.8 | 1.2 | 2.2 |
| S03 | 6 | 13.2 | 20 | 36 |
| S05 | 9 | 19.8 | 30 | 54 |
| S22 | 3 | 6.6 | 10 | 18 |

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Device | Conditions | $t_{PLH}$ (ns) Propagation Delay Time, Low-To-High Output | | | $t_{PHL}$ (ns) Propagation Delay Time, High-To-Low Output | | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max |
| 01, 03 | $C_L$ = 15 pF, $R_L$ = 4 kΩ for $t_{PLH}$ | | 35 | 45 | | 8 | 15 |
| 05 | $R_L$ = 400 Ω for $t_{PHL}$ | | 40 | 55 | | 8 | 15 |
| H01 | $C_L$ = 25 pF, $R_L$ = 280 Ω | | 10 | 15 | | 7.5 | 12 |
| L01, L03, L05 | $C_L$ = 50 pF, $R_L$ = 4 kΩ | | 60 | 90 | | 33 | 60 |
| LS01, LS03 LS05, LS12 LS22 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 6 | 12 | 20 | 3 | 7 | 15 |
| | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 20 | 32 | 45 | 4 | 10 | 20 |
| S03, S05 S22 | $C_L$ = 15 pF, $R_L$ = 280 Ω | 2 | 5 | 7.5 | 2 | 4.5 | 7 |
| | $C_L$ = 50 pF, $R_L$ = 280 Ω | 3 | 7.5 | 11 | 3 | 7 | 11 |

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## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

| Parameter | | | Conditions | | | DM54/74 02, 25, 27 | | | DM54/74 L02 | | | DM54/74 LS02, LS27 | | | DM54/74 S02 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | DM54 | | | 0.8 | | | 0.7 | | | 0.8 | | | 0.8 | V |
| | | | | | DM74 | | | 0.8 | | | 0.7 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | N/A | | | | | | | V |
| | | | | $I_I$ = −18 mA | | | | | | | N/A | | | −1.5 | | | −1.2 | |
| $I_{OH}$ | High Level Output Current | | | | 25, 27 | | | −800 | | | | | | | | | | μA |
| | | | | | Others | | | −400 | | | −200 | | | −400 | | | −1000 | |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IL}$ = Max, $I_{OH}$ = Max | LS27 | | | | | | | | 2.4 | | | | | | V |
| | | | | Others | DM54 | 2.4 | 3.4 | | 2.4 | 3.3 | | 2.5 | 3.4 | | 2.5 | 3.4 | | |
| | | | | | DM74 | 2.4 | 3.4 | | 2.4 | 3.2 | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 16 | | | 2 | | | 4 | | | 20 | mA |
| | | | | | DM74 | | | 16 | | | 3.6 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | 0.15 | 0.3 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | | DM74 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| | | | | $I_{OL}$ = 4 mA | DM74 | | | | | | | | | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | 0.1 | | | | | | 1 | mA |
| | | | | $V_I$ = 7 V | | | | | | | | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | Data Inputs | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | 10 | | | | | | | μA |
| | | Strobe of 25 | | | | | | 160 | | | | | | | | | | |
| | | All Inputs | | $V_I$ = 2.7 V | | | | | | | | | | 20 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | All Inputs | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | | | −0.18 | | | | | | | mA |
| | | Data Inputs | | $V_I$ = 0.4 V | | | | −1.6 | | | | | | −0.36 | | | | |
| | | Strobe of 25 | | | | | | −6.4 | | | | | | | | | | |
| | | All Inputs | | $V_I$ = 0.5 V | | | | | | | | | | | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | DM54 | −20 | | −55 | −3 | | −15 | −20 | | −100 | −40 | | −100 | mA |
| | | | | | DM74 | −18 | | −55 | −3 | | −15 | −20 | | −100 | −40 | | −100 | |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max | | | See Table | | | | | | | | | | | | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/DM74LS and DM54S/74S, duration of short circuit should not exceed one second.

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Device | Conditions | $t_{PLH}$ (ns) Propagation Delay Time, Low-To-High Output | | | $t_{PHL}$ (ns) Propagation Delay Time, High-To-Low Output | | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max |
| 02 | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 12 | 22 | | 8 | 15 |
| 25 | | | 13 | 22 | | 8 | 15 |
| 27 | | | 7 | 11 | | 10 | 15 |
| L02 | $C_L$ = 50 pF, $R_L$ = 4 kΩ | | 31 | 60 | | 35 | 60 |
| LS02 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 3 | 9 | 13 | 3 | 5 | 10 |
| | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 4 | 12 | 18 | 4 | 8 | 15 |
| LS27 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 3 | 9 | 13 | 3 | 5 | 10 |
| | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 5 | 12 | 18 | 4 | 8 | 15 |
| S02 | $C_L$ = 15 pF, $R_L$ = 280 Ω | 1.5 | 3.5 | 5.5 | 1.5 | 3.5 | 5.5 |
| | $C_L$ = 50 pF, $R_L$ = 280 Ω | 2 | 5 | 7.5 | 2 | 5 | 7.5 |

## Supply Currents

| Device | $I_{CCH}$ (mA) Total With Outputs High | | $I_{CCL}$ (mA) Total With Outputs Low | |
|---|---|---|---|---|
| | Typ | Max | Typ | Max |
| 02 | 8 | 16 | 14 | 27 |
| 25 | 8 | 16 | 10 | 19 |
| 27 | 10 | 16 | 16 | 26 |
| L02 | 0.8 | 1.6 | 1.4 | 2.6 |
| LS02 | 1.6 | 3.2 | 2.8 | 5.4 |
| LS27 | 2.0 | 4 | 3.4 | 6.8 |
| S02 | 17 | 29 | 26 | 45 |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

| Parameter | | Conditions | | | DM54/74 06, 07, 16,17 | | | DM54/74 26 | | | DM54/74 38 | | | DM54/74 L26 | | | DM54/74 LS26 | | | DM54/74 LS38 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ(1) | Max | Min | Typ(1) | Max | Min | Typ(1) | Max | Min | Typ(1) | Max | Min | Typ(1) | Max | Min | Typ(1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.8 | | | 0.8 | | | 0.7 | | | 0.7 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.8 | | | 0.7 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | | | −1.5 | | | N/A | | | | | | | V |
| | | | $I_I$ = −18 mA | | | | | | | | | | | | | N/A | | | −1.5 | | | −1.5 | |
| $I_{CEX}$ | High Level Output Current | $V_{CC}$ = Min, $V_I$ = (2) | $V_{OH}$ = 12 V | | | | | | | 50 | | | | | | 200 | | | 50 | | | | μA |
| | | | $V_{OH}$ = Max | | | | 250 | | | 1000 | | | 250 | | | | | | 1000 | | | 250 | |
| $V_{OH}$ | High Level Output Voltage | | | 06, 07 | | | 30 | | | | | | | | | | | | | | | | V |
| | | | | 16, 17 | | | 15 | | | | | | | | | | | | | | | | |
| | | | | Others | | | | | | 15 | | | 5.5 | | | 15 | | | 15 | | | 5.5 | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 30 | | | 16 | | | 48 | | | 2 | | | 4 | | | 12 | mA |
| | | | | DM74 | | | 40 | | | 16 | | | 48 | | | 3.6 | | | 8 | | | 24 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_I$ = (2) | $I_{OL}$ = Max | DM54 | | | 0.7 | | | 0.4 | | | 0.4 | | 0.15 | 0.3 | | 0.25 | 0.4 | | | 0.4 | V |
| | | | | DM74 | | | 0.7 | | | 0.4 | | | 0.4 | | | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 4 mA | DM74 | | | | | | | | | | | | | | 0.25 | 0.4 | | | | |
| | | | $I_{OL}$ = 12 mA | DM74 | | | | | | | | | | | | | | | | | | 0.4 | |
| | | | $I_{OL}$ = 16 mA | | | | 0.4 | | | | | | | | | | | | | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | 1 | | | 1 | | | 0.1 | | | | | | | mA |
| | | | $V_I$ = 7 V | | | | | | | | | | | | | | | | 0.1 | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | 40 | | | 40 | | | 10 | | | | | | | μA |
| | | | $V_I$ = 2.7 V | | | | | | | | | | | | | | | | 20 | | | 20 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | | | | | | | | | −0.18 | | | | | | | mA |
| | | | $V_I$ = 0.4 V | | | | −1.6 | | | −1.6 | | | −1.6 | | | | | | −0.36 | | | −0.36 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | See Table | | | | | | | | | | | | | | | | | | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** The input voltage is $V_{IH}$ = 2 V or $V_{IL}$ = max, as appropriate.

## Supply Currents

| Device | $I_{CCH}$ (mA) Total With Outputs High | | $I_{CCL}$ (mA) Total With Outputs Low | |
|---|---|---|---|---|
| | Typ | Max | Typ | Max |
| 06, 16 | 30 | 42 | 27 | 38 |
| 07, 17 | 29 | 41 | 21 | 30 |
| 26 | 4 | 8 | 12 | 22 |
| 38 | 5 | 8.5 | 34 | 54 |
| L26 | 0.48 | 0.8 | 1.32 | 2.04 |
| LS26 | 0.8 | 1.6 | 2.4 | 4.4 |
| LS38 | 0.9 | 2 | 6 | 12 |

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Device | Conditions | $t_{PLH}$ (ns) Propagation Delay Time, Low-To-High Output | | | $t_{PHL}$ (ns) Propagation Delay Time, High-To-Low Output | | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max |
| 06, 16 | $C_L$ = 15 pF, $R_L$ = 110 Ω | | 10 | 15 | | 15 | 23 |
| 07, 17 | | | 6 | 10 | | 20 | 30 |
| 26 | $C_L$ = 15 pF, $R_L$ = 1 kΩ | | 16 | 24 | | 11 | 17 |
| 38 | $C_L$ = 45 pF, $R_L$ = 133 kΩ | | 14 | 22 | | 11 | 18 |
| L26 | $C_L$ = 15 pF, $R_L$ = 4 kΩ | | 40 | 90 | | 25 | 60 |
| LS26 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 17 | 32 | | 15 | 28 |
| LS38 | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 14 | 22 | | 12 | 22 |
| LS38 | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 37 | 48 | | 22 | 29 |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

| Parameter | | Conditions | | | DM54/74 08, 11 | | | DM54/74 H08, H11, H21 | | | DM54/74 L08, L11 | | | DM54/74 LS08, LS11, LS21 | | | DM54/74 S08, S11 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.8 | | | 0.7 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.7 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −8 mA | | | | | | | −1.5 | | | N/A | | | | | | | V |
| | | | $I_I$ = −12 mA | | | | −1.5 | | | | | | N/A | | | | | | | |
| | | | $I_I$ = −18 mA | | | | | | | | | | N/A | | | −1.5 | | | −1.2 | |
| $I_{OH}$ | High Level Output Current | | | | | | −800 | | | −500 | | | −200 | | | −400 | | | −1000 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $I_{OH}$ = Max | | DM54 | 2.4 | 3.4 | | 2.4 | 3.4 | | 2.4 | 3.3 | | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.4 | 3.4 | | 2.4 | 3.4 | | 2.4 | 3.2 | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | | | 20 | | | 2 | | | 4 | | | 20 | mA |
| | | | | DM74 | | | 16 | | | 20 | | | 3.6 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.15 | 0.3 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | DM74 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 4 mA | DM74 | | | | | | | | | | | 0.25 | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | 1 | | | 0.1 | | | | | | 1 | mA |
| | | | $V_I$ = 7 V | | | | | | | | | | | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | 50 | | | 10 | | | | | | | μA |
| | | | $V_I$ = 2.7 V | | | | | | | | | | | | | 20 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | | | | | | −0.18 | | | | | | | mA |
| | | | $V_I$ = 0.4 V | | | | −1.6 | | | −2 | | | | | | −0.36 | | | | |
| | | | $V_I$ = 0.5 V | | | | | | | | | | | | | | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −20 | | −55 | −40 | | −100 | −3 | | −15 | −20 | | −100 | −40 | | −100 | mA |
| | | | | DM74 | −18 | | −55 | −40 | | −100 | −3 | | −15 | −20 | | −100 | −40 | | −100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | See Table | | | | | | | | | | | | | | | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54H/DM74H, DM54LS/DM74LS and DM54S/DM74S, duration of short circuit should not exceed one second.

## Supply Currents

| Device | $I_{CCH}$ (mA) Total With Outputs High | | $I_{CCL}$ (mA) Total With Outputs Low | |
|---|---|---|---|---|
| | Typ | Max | Typ | Max |
| 08 | 11 | 21 | 20 | 33 |
| 11 | 8 | 15 | 14 | 22 |
| H08 | 28 | 40 | 42 | 64 |
| H11 | 18 | 30 | 30 | 48 |
| H21 | 12 | 20 | 20 | 32 |
| L08 | 1.1 | 2.1 | 2.0 | 3.3 |
| L11 | 1.0 | 1.5 | 1.6 | 2.2 |
| LS08 | 2.4 | 4.8 | 4.4 | 8.8 |
| LS11 | 1.8 | 3.6 | 3.3 | 6.6 |
| LS21 | 1.2 | 2.4 | 2.2 | 4.4 |
| S08 | 18 | 32 | 32 | 57 |
| S11 | 13.5 | 24 | 24 | 42 |

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Device | Conditions | $t_{PLH}$ (ns) Propagation Delay Time Low-To-High Level Output | | | $t_{PHL}$ (ns) Propagation Delay Time, High-To-Low Level Output | | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max |
| 08, 11 | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 17.5 | 27 | | 12 | 19 |
| H08, H11 H21 | $C_L$ = 25 pF, $R_L$ = 280 Ω | | 7.6 | 12 | | 8.8 | 12 |
| L08 | $C_L$ = 50 pF | | 45 | 90 | | 45 | 90 |
| L11 | $R_L$ = 4 kΩ | | 40 | 80 | | 45 | 90 |
| LS08, LS11 LS21 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 4 | 8 | 13 | 3 | 7.5 | 11 |
| | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 6 | 11 | 18 | 5 | 11 | 18 |
| S08, S11 | $C_L$ = 15 pF, $R_L$ = 280 Ω | 2.5 | 4.5 | 7 | 2.5 | 5 | 7.5 |
| | $C_L$ = 50 pF, $R_L$ = 280 Ω | 3 | 6 | 9 | 3 | 7.5 | 11 |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

| Parameter | | Conditions | | | DM54/74 09 | | | DM54/74 L09 | | | DM54/DM74 LS09, LS15 | | | DM54/74 S09, S15 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.7 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.7 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | N/A | | | | | | | V |
| | | | $I_I$ = −18 mA | | | | | | | N/A | | | −1.5 | | | −1.2 | |
| $I_{CEX}$ | High Level Output Current | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{OH}$ = 5.5 V | | | | | 250 | | | 50 | | | 100 | | | 250 | μA |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | | | 2 | | | 4 | | | 20 | mA |
| | | | | DM74 | | | 16 | | | 3.6 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | 0.15 | 0.3 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | DM74 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 4 mA | DM74 | | | | | | | | | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | 0.1 | | | | | | 1 | mA |
| | | | $V_I$ = 7 V | | | | | | | | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | 10 | | | | | | | μA |
| | | | $V_I$ = 2.7 V | | | | | | | | | | 20 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | | | −0.18 | | | | | | | mA |
| | | | $V_I$ = 0.4 V | | | | −1.6 | | | | | | −0.36 | | | | |
| | | | $V_I$ = 0.5 V | | | | | | | | | | | | | −2 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | See Table | | | | | | | | | | | | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## Supply Currents

| Device | $I_{CCH}$ (mA) Total With Outputs High | | $I_{CCL}$ (mA) Total With Outputs Low | |
|---|---|---|---|---|
| | Typ | Max | Typ | Max |
| 09 | 11 | 21 | 20 | 33 |
| L09 | 1.1 | 2.1 | 2 | 3.3 |
| LS09 | 2.4 | 4.8 | 4.4 | 8.8 |
| LS15 | 1.8 | 3.6 | 3.3 | 6.6 |
| S09 | 18 | 32 | 32 | 57 |
| S15 | 10.5 | 19.5 | 24 | 42 |

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Device | Conditions | $t_{PLH}$ (ns) Propagation Delay Time, Low-To-High Level Output | | | $t_{PHL}$ (ns) Propagation Delay Time, High-To-Low Level Output | | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max |
| 09 | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 21 | 32 | | 16 | 24 |
| L09 | $C_L$ = 15 pF, $R_L$ = 4 kΩ | | 50 | 110 | | 50 | 110 |
| LS09, LS15 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 5 | 13 | 20 | 4 | 10 | 15 |
| | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 8 | 20 | 30 | 6 | 18 | 27 |
| S09 | $C_L$ = 15 pF, $R_L$ = 280 Ω | 3 | 6.5 | 10 | 3 | 6.5 | 10 |
| | $C_L$ = 50 pF, $R_L$ = 280 Ω | 4 | 9 | 18 | 4 | 9 | 18 |
| S15 | $C_L$ = 15 pF, $R_L$ = 280 Ω | 2 | 5.5 | 8.5 | 2 | 6 | 9 |
| | $C_L$ = 50 pF, $R_L$ = 280 Ω | 3 | 8.5 | 13 | 3 | 8 | 12 |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

| Parameter | | | Conditions | | | DM54/74 13 Min | DM54/74 13 Typ (1) | DM54/74 13 Max | DM54/74 14 Min | DM54/74 14 Typ (1) | DM54/74 14 Max | DM54/74 132 Min | DM54/74 132 Typ (1) | DM54/74 132 Max | DM54/74 LS13, LS14, LS132 Min | DM54/74 LS13, LS14, LS132 Typ (1) | DM54/74 LS13, LS14, LS132 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{T+}$ | Positive-Going Threshold Voltage | | $V_{CC}$ = 5 V | | | 1.5 | 1.7 | 2 | 1.5 | 1.7 | 2 | 1.5 | 1.7 | 2 | 1.4 | 1.6 | 1.9 | V |
| $V_{T-}$ | Negative-Going Threshold Voltage | | $V_{CC}$ = 5 V | | | 0.6 | 0.9 | 1.1 | 0.6 | 0.9 | 1.1 | 0.6 | 0.9 | 1.1 | 0.5 | 0.8 | 1.0 | V |
| $V_{T+}$ $V_{T-}$ | Hysteresis | | $V_{CC}$ = 5 V | | | 0.4 | 0.8 | | 0.4 | 0.8 | | 0.4 | 0.8 | | 0.4 | 0.8 | | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | | | −1.5 | | | | V |
| | | | | $I_I$ = −18 mA | | | | | | | | | | | | | −1.5 | |
| $I_{OH}$ | High Level Output Current | | | | | | | −800 | | | −800 | | | −800 | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_I$ = $V_{T-}$ Min, $I_{OH}$ = Max | | DM54 | 2.4 | 3.4 | | 2.4 | 3.4 | | 2.4 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | | DM74 | 2.4 | 3.4 | | 2.4 | 3.4 | | 2.4 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 16 | | | 16 | | | 16 | | | 4 | mA |
| | | | | | DM74 | | | 16 | | | 16 | | | 16 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_I$ = $V_{T+}$ Max | $I_{OL}$ = 4 mA | | | | | | | | | | | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$ = 8 mA | DM74 | | | | | | | | | | | 0.35 | 0.5 | |
| | | | | $I_{OL}$ = 16 mA | | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.2 | 0.4 | | | | |
| $I_{T+}$ | Input Current at Positive-Going Threshold | | $V_{CC}$ = 5 V, $V_I$ = $V_{T+}$ | | | | −0.65 | | | −0.43 | | | −0.43 | | | −0.14 | | mA |
| $I_{T-}$ | Input Current at Negative-Going Threshold | | $V_{CC}$ = 5 V, $V_I$ = $V_{T-}$ | | | | −0.85 | | | −0.56 | | | −0.56 | | | −0.18 | | mA |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | 1 | | | 1 | | | | mA |
| | | | | $V_I$ = 7.0 V | | | | | | | | | | | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | 40 | | | 40 | | | | μA |
| | | | | $V_I$ = 2.7 V | | | | | | | | | | | | | 20 | |
| $I_{IL}$ | Low Level Input Current | | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −1.0 | −1.6 | | −0.8 | −1.2 | | −0.8 | −1.2 | | | −0.4 | mA |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | | −18 | | −55 | −18 | | −55 | −18 | | −55 | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current | Total Output High | $V_{CC}$ = Max | $V_I$ = 0 V | LS13 | | | | | | | | | | | 2.9 | 6 | mA |
| | | | | | LS14 | | | | | | | | | | | 8.6 | 16 | |
| | | | | | LS132 | | | | | | | | | | | 5.9 | 11 | |
| | | | | | Others | | 14 | 23 | | 22 | 36 | | 15 | 24 | | | | |
| | | Total Output Low | | $V_I$ = 4.5 V | LS13 | | | | | | | | | | | 4.1 | 7 | |
| | | | | | LS14 | | | | | | | | | | | 12 | 21 | |
| | | | | | LS132 | | | | | | | | | | | 8.2 | 14 | |
| | | | | | Others | | 20 | 32 | | 39 | 60 | | 26 | 40 | | | | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/DM74LS, duration of short circuit should not exceed one second.

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Device | Conditions | $t_{PLH}$ (ns) Propagation Delay Time, Low-To-High Level Output | | | $t_{PHL}$ (ns) Propagation Delay Time, High-To-Low Level Output | | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max |
| 13 | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 18 | 27 | | 15 | 22 |
| 14, 132 | | | 15 | 22 | | 15 | 22 |
| LS13, LS14, LS132 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 5 | 15 | 22 | 5 | 15 | 22 |
| | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 8 | 18 | 25 | 10 | 21 | 33 |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

| Parameter | | | Conditions | | DM54/74 23 Min | DM54/74 23 Typ (1) | DM54/74 23 Max | DM54/74 50, 53 Min | DM54/74 50, 53 Typ (1) | DM54/74 50, 53 Max | DM54/74 H50 Min | DM54/74 H50 Typ (1) | DM54/74 H50 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.8 | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = −8 mA | | | | | | | | | −1.5 | V |
| | | | | $I_I$ = −12 mA | | | −1.5 | | | −1.5 | | | | |
| $I_{OH}$ | High Level Output Current | | | | | | −800 | | | −400 | | | −500 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_I$ = (2), $I_{OH}$ = Max | | 2.4 | 3.4 | | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| $I_{OL}$ | Low Level Output Current | | | | | | 16 | | | 16 | | | 20 | mA |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_I$ = (2), $I_{OL}$ = Max | | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | Data Inputs | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | | | 40 | | | 50 | μA |
| | | Strobe of 23 | | | | | 160 | | | N/A | | | N/A | |
| $I_{IL}$ | Low Level Input Current | Data Inputs | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −1.6 | | | −1.6 | | | −2 | mA |
| | | Strobe of 23 | | | | | −6.4 | | | N/A | | | N/A | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (3) | DM54 | −20 | | −55 | −20 | | −55 | −40 | | −100 | mA |
| | | | | DM74 | −18 | | −55 | −18 | | −55 | −40 | | −100 | |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max | | See Table | | | | | | | | | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** The input voltage is $V_{IH}$ = 2 V or $V_{IL}$ = 0.8 V, as appropriate.

**Note 3:** Not more than one output should be shorted at a time, and for the DM54H/DM74H, duration of short circuit should not exceed one second.

## Electrical Characteristics using expander inputs, $V_{CC}$ = Min, $T_A$ = Min (unless otherwise noted) (4), (5)

| Device | $I_{\overline{X}}$ (mA) Expander Current | | | | $V_{BE(Q)}$ (V) Base-Emitter Voltage of Output Transistor Q | | | | $V_{OH}$ (V) High Level Output Voltage | | | | $V_{OL}$ (V) Low Level Output Voltage | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Conditions | Min | Typ (1) | Max | Conditions | Min | Typ (1) | Max | Conditions | Min | Typ (1) | Max | Conditions | Min | Typ (1) | Max |
| DM5423<br>DM5450<br>DM5453 | $V_{\overline{X}X}$ = 0.4 V<br>$I_{OL}$ = 16 mA | | | −3.5<br>−2.9<br>−2.9 | $I_X + I_{\overline{X}}$ = 410 μA<br>$R_{\overline{X}X}$ = 0<br>$I_{OL}$ = 16 mA | | | 1.1 | $I_X$ = 150 μA<br>$I_{\overline{X}}$ = −150 μA<br>$I_{OH}$ = −400 μA | 2.4 | 3.4 | | $I_X + I_{\overline{X}}$ = 300 μA<br>$R_{\overline{X}X}$ = 138 Ω<br>$I_{OL}$ = 16 mA | | 0.2 | 0.4 |
| DM7423<br>DM7450<br>DM7453 | $V_{\overline{X}X}$ = 0.4 V<br>$I_{OL}$ = 16 mA | | | −3.5<br>−3.1<br>−3.1 | $I_X + I_{\overline{X}}$ = 620 μA<br>$R_{\overline{X}X}$ = 0<br>$I_{OL}$ = 16 mA | | | 1.0 | $I_X$ = 270 μA<br>$I_{\overline{X}}$ = −270 μA<br>$I_{OH}$ = −400 μA | 2.4 | 3.4 | | $I_X + I_{\overline{X}}$ = 430 μA<br>$R_{\overline{X}X}$ = 130 Ω<br>$I_{OL}$ = 16 mA | | 0.2 | 0.4 |
| DM54H50 | $V_{\overline{X}}$ = 1.4 V | | | −5.85 | $I_X + I_{\overline{X}}$ = 700 μA | | | 1.1 | $I_X$ = 320 μA | 2.4 | 3.4 | | $I_X + I_{\overline{X}}$ = 470 μA | | 0.2 | 0.4 |
| DM74H50 | $V_{\overline{X}}$ = 1.4 V | | | −6.3 | $I_X + I_{\overline{X}}$ = 1.1 mA | | | 1.0 | $I_X$ = 570 μA | 2.4 | 3.4 | | $I_X + I_{\overline{X}}$ = 600 μA | | 0.2 | 0.4 |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 4:** The 23, 50, and 53 are designed for use with up to four 60 expanders.
**Note 5:** The H50 is designed for use with a H62 expander.

## Supply Currents

| Device | $I_{CCH}$ (mA) Total With Outputs High | | $I_{CCL}$ (mA) Total With Outputs Low | |
|---|---|---|---|---|
| | Typ | Max | Typ | Max |
| 23 | 8 | 16 | 10 | 19 |
| 50 | 4 | 8 | 7.4 | 14 |
| 53 | 4 | 8 | 5.1 | 9.5 |
| H50 | 8.2 | 12.8 | 15.2 | 24 |

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Device | Conditions | $t_{PLH}$ (ns) Propagation Delay Time, Low-To-High Level Output | | | $t_{PHL}$ (ns) Propagation Delay Time, High-To-Low Level Output | | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max |
| 23, 50, 53 | $C_L$ = 15 pF, $R_L$ = 400 Ω<br>Expander Pins Open | | 13 | 22 | | 8 | 15 |
| 50 | $C_L$ = 15 pF, $R_L$ = 400 Ω<br>From Input of 60 Expander | | 15 | 30 | | 10 | 20 |
| H50 | $C_L$ = 25 pF, $R_L$ = 280 Ω<br>Expander Pins Open | | 6.8 | 11 | | 6.2 | 11 |
| H50 | $C_L$ = 25 pF, $R_L$ = 280 Ω<br>C = 15 pF, (GND to $\overline{X}$ of H50) | | 11 | | | 7.4 | |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

| Parameter | | | Conditions | | | DM54/74 32 | | | DM54/74 L32 | | | DM54/74 LS32 | | | DM54/74 S32 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | DM54 | | | 0.8 | | | 0.7 | | | 0.8 | | | 0.8 | V |
| | | | | | DM74 | | | 0.8 | | | 0.7 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = − 12 mA | | | | −1.5 | | | N/A | | | | | | | V |
| | | | | $I_I$ = −18 mA | | | | | | | N/A | | | −1.5 | | | −1.2 | |
| $I_{OH}$ | High Level Output Current | | | | | | | −800 | | | −200 | | | −400 | | | −1000 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $I_{OH}$ = Max | | DM54 | 2.4 | 3.4 | | 2.4 | 2.8 | | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | | DM74 | 2.4 | 3.4 | | 2.4 | 2.8 | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 16 | | | 2 | | | 4 | | | 20 | mA |
| | | | | | DM74 | | | 16 | | | 3.6 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | 0.15 | 0.3 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | | DM74 | | 0.2 | 0.4 | | | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| | | | | $I_{OL}$ = 4 mA | DM74 | | | | | | | | 0.25 | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | 0.1 | | | | | | 1 | mA |
| | | | | $V_I$ = 7 V | | | | | | | | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | 10 | | | | | | | μA |
| | | | | $V_I$ = 2.7 V | | | | | | | | | | 20 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | | −0.12 | −0.18 | | | | | | | mA |
| | | | | $V_I$ = 0.4 V | | | | −1.6 | | | | | | −0.36 | | | | |
| | | | | $V_I$ = 0.5 V | | | | | | | | | | | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | DM54 | −20 | | −55 | −3 | −9 | −15 | −20 | | −100 | −40 | | −100 | mA |
| | | | | | DM74 | −18 | | −55 | −3 | −9 | −15 | −20 | | −100 | −40 | | −100 | |
| $I_{CC}$ | Supply Current | Total, Outputs High | $V_{CC}$ = Max | | | | 15 | 22 | | 1.5 | 2.2 | | 3.1 | 6.2 | | 18 | 32 | mA |
| | | Total, Outputs Low | | | | | 23 | 38 | | 2.3 | 3.8 | | 4.9 | 9.8 | | 38 | 68 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at one time, and for DM54LS/DM74LS and DM54S/74S duration of short circuit should not exceed one second.

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C.

| Device | Conditions | $t_{PLH}$ (ns) Propagation Delay Time, Low-To-High Level Output | | | $t_{PHL}$ (ns) Propagation Delay Time, High-To-Low Level Output | | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max |
| 32 | $C_L$ = 15 pF<br>$R_L$ = 400 Ω | | 10 | 15 | | 14 | 22 |
| L32 | $C_L$ =50 pF<br>$R_L$ = 4 kΩ | | 40 | 80 | | 50 | 100 |
| LS32 | $C_L$ = 15 pF<br>$R_L$ = 2 kΩ | 3 | 7 | 11 | 3 | 7 | 11 |
| | $C_L$ = 50 pF<br>$R_L$ = 2 kΩ | 4 | 10 | 15 | 4 | 10 | 15 |
| S32 | $C_L$ = 15 pF<br>$R_L$ = 280 Ω | 2 | 4 | 7 | 2 | 4 | 7 |
| | $C_L$ = 50 pF<br>$R_L$ = 280 Ω | 2 | 5 | 9 | 2 | 5 | 9 |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

| Parameter | | Conditions | | | DM54/74 37, 40 | | | DM54/74 H40 | | | DM54/74 LS37, LS40 | | | DM54/74 S40, S140 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.8 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −8 mA | | | | | | | −1.5 | | | | | | | V |
| | | | $I_I$ = −12 mA | | | | −1.5 | | | | | | | | | | |
| | | | $I_I$ = −18 mA | | | | | | | | | | −1.5 | | | −1.2 | |
| $I_{OH}$ | High Level Output Current | | | Others | | | −1.2 | | | −1.5 | | | −1.2 | | | −3 | mA |
| | | | | S140 | | | | | | | | | | | | −40 | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min | $I_{OH}$ = Max, $V_{IL}$ = Max | DM54 | 2.4 | 3.3 | | 2.4 | 3.4 | | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.4 | 3.3 | | 2.4 | 3.4 | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| | | | $V_{IL}$ = 0.5 V, $R_O$ = 50 Ω to GND, S140 Only | | | | | | | | | | | 2 | | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 48 | | | 60 | | | 12 | | | 60 | mA |
| | | | | DM74 | | | 48 | | | 60 | | | 24 | | | 60 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | DM74 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 12 mA | DM74 | | | | | | | | 0.25 | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | 1 | | | | | | 1 | mA |
| | | | $V_I$ = 7 V | | | | | | | | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | 100 | | | | | | | μA |
| | | | $V_I$ = 2.7 V | | | | | | | | | | 20 | | | 100 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.4 V | | | | −1.6 | | | −4 | | | −0.36 | | | | mA |
| | | | $V_I$ = 0.5 V | | | | | | | | | | | | | −4 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −20 | | −70 | −40 | | −125 | −20 | | −100 | −50 | | −225 | mA |
| | | | | DM74 | −18 | | −70 | −40 | | −125 | −20 | | −100 | −50 | | −225 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | See Table | | | | | | | | | | | | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second for 37, LS37, 40, H40 or LS40; or 100 milliseconds for S40 and S140.

## Supply Currents

| Device | $I_{CCH}$ (mA) Total With Outputs High | | $I_{CCL}$ (mA) Total With Outputs Low | |
|---|---|---|---|---|
| | Typ | Max | Typ | Max |
| 37 | 9 | 15.5 | 34 | 54 |
| 40 | 4 | 8 | 17 | 27 |
| H40 | 10.4 | 16 | 25 | 40 |
| LS37 | 0.9 | 2 | 6 | 12 |
| LS40 | 0.45 | 1 | 3 | 6 |
| S40 | 10 | 18 | 25 | 44 |
| S140 | 10 | 18 | 25 | 44 |

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Device | Conditions | $t_{PLH}$ (ns) Propagation Delay Time, Low-To-High Level Output | | | $t_{PHL}$ (ns) Propagation Delay Time, High-To-Low Level Output | | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max |
| 37 | $C_L$ = 45 pF, $R_L$ = 133 Ω | | 13 | 22 | | 8 | 15 |
| 40 | $C_L$ = 15 pF, $R_L$ = 133 Ω | | 13 | 22 | | 8 | 15 |
| H40 | $C_L$ = 25 pF, $R_L$ = 93 Ω | | 8.5 | 12 | | 6.5 | 12 |
| LS37, LS40 | $C_L$ = 45 pF, $R_L$ = 667 Ω | 3 | 10 | 15 | 3 | 10 | 15 |
| | $C_L$ = 150 pF, $R_L$ = 667 Ω | 4 | 13 | 18 | 4 | 16 | 21 |
| S40, S140 | $C_L$ = 50 pF, $R_L$ = 93 Ω | 2 | 4 | 6.5 | 2 | 4 | 6.5 |
| | $C_L$ = 150 pF, $R_L$ = 93 Ω | 3 | 6 | 9 | 3 | 6 | 9 |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

| Parameter | | Conditions | | | DM54/74 | | | | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 51, 54 | | | L51, L54 L55 | | | LS51, LS54 LS55 | | | S51, S64 | | | |
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.7 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.7 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −8 mA | | | | | | | N/A | | | | | | | V |
| | | | $I_I$ = −12 mA | | | | −1.5 | | | N/A | | | | | | | |
| | | | $I_I$ = −18 mA | | | | | | | N/A | | | −1.5 | | | −1.2 | |
| $I_{OH}$ | High Level Output Current | | | | | | −400 | | | −200 | | | −400 | | | −1000 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IL}$ = Max, $I_{OH}$ = Max | LS54 | | | | | | | | 2.4 | | | | | | V |
| | | | Others | DM54 | 2.4 | 3.4 | | 2.4 | 3.3 | | 2.5 | 3.4 | | 2.5 | 3.4 | | |
| | | | | DM74 | 2.4 | 3.4 | | 2.4 | 3.2 | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | | | 2 | | | 4 | | | 20 | mA |
| | | | | DM74 | | | 16 | | | 3.6 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | 0.15 | 0.3 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | DM74 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 4 mA | DM74 | | | | | | | | 0.25 | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | 0.1 | | | | | | 1 | mA |
| | | | $V_I$ = 7 V | | | | | | | | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | 10 | | | | | | | μA |
| | | | $V_I$ = 2.7 V | | | | | | | | | | 20 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | | | −0.18 | | | | | | | mA |
| | | | $V_I$ = 0.4 V | | | | −1.6 | | | | | | −0.36 | | | | |
| | | | $V_I$ = 0.5 V | | | | | | | | | | | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −20 | | −55 | −3 | | −15 | −20 | | −100 | −40 | | −100 | mA |
| | | | | DM74 | −18 | | −55 | −3 | | −15 | −20 | | −100 | −40 | | −100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | See Table | | | | | | | | | | | | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/DM74LS and DM54S/DM74S, duration of the short circuit should not exceed one second.

## Supply Currents

| Device | $I_{CCH}$ (mA) Total With Outputs High | | $I_{CCL}$ (mA) Total With Outputs Low | |
|---|---|---|---|---|
| | Typ | Max | Typ | Max |
| 51 | 4 | 8 | 7.4 | 14 |
| 54 | 4 | 8 | 5.1 | 9.5 |
| L51 | 0.44 | 0.8 | 0.76 | 1.3 |
| L54 | 0.39 | 0.8 | 0.60 | 0.99 |
| L55 | 0.22 | 0.4 | 0.38 | 0.65 |
| LS51 | 0.8 | 1.6 | 1.4 | 2.8 |
| LS54 | 0.8 | 1.6 | 1.0 | 2 |
| LS55 | 0.4 | 0.8 | 0.7 | 1.3 |
| S51 | 8.2 | 17.8 | 13.6 | 22 |
| S64 | 7 | 12.5 | 8.5 | 16 |

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Device | Conditions | $t_{PLH}$ (ns) Propagation Delay Time, Low-To-High Level Output | | | $t_{PHL}$ (ns) Propagation Delay Time, High-To-Low Level Output | | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max |
| 51, 54 | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 13 | 22 | | 8 | 15 |
| L51, L54, L55 | $C_L$ = 50 pF, $R_L$ = 4 kΩ | | 50 | 90 | | 35 | 60 |
| LS51 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 3 | 9 | 13 | 2 | 6 | 12 |
| | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 4 | 12 | 18 | 3 | 8 | 15 |
| LS54 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 5 | 15 | 20 | 3 | 7 | 13 |
| | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 6 | 18 | 25 | 4 | 10 | 18 |
| LS55 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 3 | 9 | 13 | 2 | 6 | 12 |
| | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 4 | 12 | 18 | 3 | 10 | 18 |
| S51, S64 | $C_L$ = 15 pF, $R_L$ = 280 Ω | 2 | 3.5 | 5.5 | 2 | 3.5 | 5.5 |
| | $C_L$ = 50 pF, $R_L$ = 280 Ω | 3 | 5 | 8 | 3 | 5.5 | 8 |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | DM54 60 | | | Conditions | DM74 60 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ (1) | Max | | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | 2 | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | | | | 0.8 | V |
| $V_{\overline{X}X(ON)}$ | On-State Voltage Between Expander Outputs | $V_{CC}$ = 4.5 V, $V_{IH}$ = 2 V, $V_X$ = 1.1 V, $I_{\overline{X}}$ = 3.5 mA, $T_A$ = −55°C | | | 0.4 | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_X$ = 1 V, $I_{\overline{X}}$ = 3.5 mA, $T_A$ = 0°C | | | 0.4 | V |
| $I_{X(ON)}$ | On-State Expander Current | $V_{CC}$ = 4.5 V, $V_{IH}$ = 2 V, $V_X$ = 1.1 V, $I_{\overline{X}}$ = 0, $T_A$ = −55°C | −0.3 | | | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_X$ = 1 V, $I_{\overline{X}}$ = 0, $T_A$ = 0°C | −0.43 | | | mA |
| $I_{\overline{X}(OFF)}$ | Off-State Expander Current | $V_{CC}$ = 4.5 V, $V_{IL}$ = 0.8 V, $V_{\overline{X}}$ = 4.5 V, $R_X$ = 1.2 kΩ, $T_A$ = −55°C | | | 150 | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, $V_{\overline{X}}$ = 4.5 V, $R_X$ = 1.2 kΩ, $T_A$ = 0°C | | | 270 | μA |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = 5.5 V, $V_I$ = 5.5 V | | | 1 | $V_{CC}$ = 5.25 V, $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = 5.5 V, $V_I$ = 2.4 V | | | 40 | $V_{CC}$ = 5.25 V, $V_I$ = 2.4 V | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = 5.5 V, $V_I$ = 0.4 V | | | −1.6 | $V_{CC}$ = 5.25 V, $V_I$ = 0.4 V | | | −1.6 | mA |
| $I_{CC(ON)}$ | Supply Current, Expander On | $V_{CC}$ = 5.5 V, $V_I$ = 4.5 V, $V_X$ = 0.85 V, $I_{\overline{X}}$ = 0 | | 1.2 | 2.5 | $V_{CC}$ = 5.25 V, $V_I$ = 4.5 V, $V_X$ = 0.85 V, $I_{\overline{X}}$ = 0 | | 1.2 | 2.5 | mA |
| $I_{CC(OFF)}$ | Supply Current, Expander Off | $V_{CC}$ = 5.5 V, $V_I$ = 0, $V_X$ = 0.85 V, $I_{\overline{X}}$ = 0 | | 2 | 4 | $V_{CC}$ = 5.25 V, $V_I$ = 0, $V_X$ = 0.85 V, $I_{\overline{X}}$ = 0 | | 2 | 4 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | DM54 H62 Min | DM54 H62 Typ (1) | DM54 H62 Max | Conditions | DM74 H62 Min | DM74 H62 Typ (1) | DM74 H62 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | | | | 0.8 | V |
| $V_{\overline{X}X(ON)}$ | On-State Voltage Between Expander Outputs | | $V_{CC}$ = 4.5 V, $V_{IH}$ = 2 V, $V_X$ = 1 V, $I_{\overline{X}}$ = 5.85 mA, $T_A$ = −55°C | | | 0.4 | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_X$ = 1 V, $I_{\overline{X}}$ = 6.3 mA, $T_A$ = 0°C | | | 0.4 | V |
| | | | $V_{CC}$ = 5.5 V, $V_{IH}$ = 2 V, $V_X$ = 1 V, $I_{\overline{X}}$ = 7.85 mA, $T_A$ = 125°C | | | 0.4 | $V_{CC}$ = 5.25 V, $V_{IH}$ = 2 V, $V_X$ = 1 V, $I_{\overline{X}}$ = 7.4 mA, $T_A$ = 70°C | | | 0.4 | |
| $I_{X(ON)}$ | On-State Expander Current | | $V_{CC}$ = 4.5 V, $V_{IH}$ = 2 V, $V_X$ = 1 V, $I_{\overline{X}}$ = 0, $T_A$ = −55°C | −470 | | | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_X$ = 1 V, $I_{\overline{X}}$ = 0, $T_A$ = 0°C | −600 | | | μA |
| $I_{\overline{X}(OFF)}$ | Off-State Expander Current | | $V_{CC}$ = 4.5 V, $V_{IL}$ = 0.8 V, $V_{\overline{X}}$ = 4.5 V, $R_X$ = 575 Ω, $T_A$ = −55°C | | | 320 | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, $V_{\overline{X}}$ = 4.5 V, $R_X$ = 575 Ω, $T_A$ = 0°C | | | 570 | μA |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = 5.5 V, $V_I$ = 5.5 V | | | 1 | $V_{CC}$ = 5.25 V, $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | | $V_{CC}$ = 5.5 V, $V_I$ = 2.4 V | | | 50 | $V_{CC}$ = 5.25 V, $V_I$ = 2.4 V | | | 50 | μA |
| $I_{IL}$ | Low Level Input Current | | $V_{CC}$ = 5.5 V, $V_I$ = 0.4 V | | | −2 | $V_{CC}$ = 5.25 V, $V_I$ = 0.4 V | | | −2 | mA |
| $I_{CC(ON)}$ | Supply Current, Expander On | H60 | $V_{CC}$ = 5.5 V, $V_I$ = 4.5 V, $V_X$ = 0.85 V, $I_{\overline{X}}$ = 0 | | 1.9 | 3.5 | $V_{CC}$ = 5.25 V, $V_I$ = 4.5 V, $V_X$ = 0.85 V, $I_{\overline{X}}$ = 0 | | 1.9 | 3.5 | mA |
| | | H62 | | | 3.8 | 7 | | | 3.8 | 7 | |
| $I_{CC(OFF)}$ | Supply Current, Expander Off | H60 | $V_{CC}$ = 5.5 V, $V_I$ = 0, $V_X$ = 0.85 V, $I_{\overline{X}}$ = 0 | | 3 | 4.5 | $V_{CC}$ = 5.25 V, $V_I$ = 0, $V_X$ = 0.85 V, $I_{\overline{X}}$ = 0 | | 3 | 4.5 | mA |
| | | H62 | | | 6 | 9 | | | 6 | 9 | |
| $C_{\overline{X}}$ | Expander Output Capacitance | H60 | $V_{CC}$, Inputs and X Open; f = 1 MHz | | 5.4 | | $V_{CC}$, Inputs and X Open; f = 1 MHz | | 5.4 | | pF |
| | | H62 | | | 6.0 | | | | 6.0 | | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V (except $C_{\overline{X}}$), $T_A$ = 25°C.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

| Parameter | | Conditions | DM54/74 S65 | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | −1.2 | V |
| $I_{CEX}$ | High Level Output Current | $V_{CC}$ = Min, $V_{IL}$ = 0.8 V, $V_{OH}$ = 5.5 V | | | 250 | μA |
| $I_{OL}$ | Low Level Output Current | | | | 20 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $I_{OL}$ = 20 mA | | | 0.5 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | 50 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.5 V | | | −2 | mA |
| $I_{CCH}$ | Supply Current, Output High | $V_{CC}$ = Max | | 6 | 11 | mA |
| $I_{CCL}$ | Supply Current, Output Low | $V_{CC}$ = Max | | 8.5 | 16 | mA |

Note 1: All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | DM54/74 S65 | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-To-High Level Output | $C_L$ = 15 pF, $R_L$ = 280 Ω | 2 | 5 | 7.5 | ns |
| | | $C_L$ = 50 pF, $R_L$ = 280 Ω | 3 | 8 | 12 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | $C_L$ = 15 pF, $R_L$ = 280 Ω | 2 | 5.5 | 8.5 | ns |
| | | $C_L$ = 50 pF, $R_L$ = 280 Ω | 3 | 6.5 | 10 | ns |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

| Parameter | | | Conditions | | DM54/74 | | | | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 70 | | | 72, 73, 76, 107 | | | 74 | | | 109 | | | |
| | | | | | Min | Typ(1) | Max | Min | Typ(1) | Max | Min | Typ(1) | Max | Min | Typ(1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.8 | | | 0.8 | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | | −400 | | | −400 | | | −400 | | | −1200 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | 2.4 | 3.4 | | 2.4 | 3.4 | | 2.4 | 3.4 | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | | 16 | | | 16 | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$= 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | | | 1 | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | D, J, K, or $\overline{K}$ | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | | | 40 | | | 40 | | | 40 | μA |
| | | Clear | | | | | 80 | | | 80 | | | 120 | | | 160 | |
| | | Preset | | | | | 80 | | | 80 | | | 40 | | | 80 | |
| | | Clock | | | | | 40 | | | 80 | | | 80 | | | 80 | |
| $I_{IL}$ | Low Level Input Current | D, J, K, or $\overline{K}$ | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −1.6 | | | −1.6 | | | −1.6 | | | −1.6 | mA |
| | | Clear (2) | | | | | −3.2 | | | −3.2 | | | −3.2 | | | −4.8 | |
| | | Preset (2) | | | | | −3.2 | | | −3.2 | | | −1.6 | | | −3.2 | |
| | | Clock | | | | | −1.6 | | | −3.2 | | | −3.2 | | | −3.2 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (3) | DM54 | −20 | | −57 | −20 | | −55 | −20 | | −55 | −30 | −55 | −85 | mA |
| | | | | DM74 | −18 | | −57 | −18 | | −55 | −18 | | −55 | −30 | −55 | −85 | |
| $I_{CC}$ | Supply Currrent (Average per Flip-Flop) | | $V_{CC}$ = Max (4) | | | 13 | 26 | | 9 | 17 | | 8.5 | 15 | | 10 | 15 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Clear is tested with Preset high and Preset is tested with Clear high.

**Note 3:** Not more than one output should be shorted at a time.

**Note 4:** With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input is at 4.5 V for the 70, and is grounded for all the others.

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | DM54/74 | | | | | | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Conditions | 70 | | | 72, 73, 76, 107 | | | Conditions | 74 | | | 109 | | | |
| | | | | | Min | Typ | Max | Min | Typ | Max | | Min | Typ | Max | Min | Typ | Max | |
| $f_{MAX}$ | Clock Frequency | | | $C_L$ = 15 pF, $R_L$ = 400 Ω | 20 | 35 | | 15 | 20 | | $C_L$ = 15 pF, $R_L$ = 400 Ω | 20 | 25 | | 30 | 40 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Preset (as applicable) | Q | | | | 50 | | 16 | 25 | | | | 25 | | 9 | 14 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | $\overline{Q}$ | | | | 50 | | 25 | 40 | | | | 40 | | 18 | 29 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Clear (as applicable) | $\overline{Q}$ | | | | 50 | | 16 | 25 | | | | 25 | | 9 | 14 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Q | | | | 50 | | 25 | 40 | | | | 40 | | 17 | 25 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Clock | Q or $\overline{Q}$ | | | 27 | 50 | | 16 | 25 | | | 14 | 25 | | 12 | 18 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 18 | 50 | | 25 | 40 | | | 20 | 40 | | 19 | 28 | |
| $t_W$ | Pulse Width | Clock High | | | 20 | | | 20 | | | | 30 | | | 20 | | | ns |
| | | Clock Low | | | 30 | | | 47 | | | | 37 | | | 20 | | | |
| | | Preset or Clear Low | | | 25 | | | 25 | | | | 30 | | | 20 | | | |
| $t_{SETUP}$ | Input Setup Time (4) | | | | 20↑ | | | 0↑ | | | | 20↑ | | | 15↑ | | | ns |
| $t_{HOLD}$ | Input Hold Time (4) | | | | 5↑ | | | 0↑ | | | | 5↑ | | | 10↑ | | | ns |

**Note 4:** ↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

| Parameter | | | Conditions | | DM54/74 | | | | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | L71, L72 | | | L73 | | | L74 | | | L78 | | | |
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | Clock Input | | | | | 0.6 | | | 0.6 | | | 0.7 | | | 0.6 | V |
| | | All Other Inputs | | | | | 0.7 | | | 0.7 | | | 0.7 | | | 0.7 | |
| $I_{OH}$ | High Level Output Current | | | | | | −200 | | | −200 | | | −200 | | | −200 | μA |
| $V_{OH}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | DM54 | 2.4 | 3.3 | | 2.4 | 3.3 | | 2.4 | 3.3 | | 2.4 | 3.3 | | V |
| | | | | DM74 | 2.4 | 3.2 | | 2.4 | 3.2 | | 2.4 | 3.2 | | 2.4 | 3.2 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 2 | | | 2 | | | 2 | | | 2 | mA |
| | | | | DM74 | | | 3.6 | | | 3.6 | | | 3.6 | | | 3.6 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OL}$ = Max | DM54 | | 0.15 | 0.3 | | 0.15 | 0.3 | | 0.15 | 0.3 | | 0.15 | 0.3 | V |
| | | | | DM74 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.2 | 0.4 | |
| $I_I$ | Input Current at Maximum Input Voltage | R, S, J, K, or D | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 100 | | | 100 | | | 100 | | | 100 | μA |
| | | Clear | | | | | 200 | | | 200 | | | 300 | | | 400 | |
| | | Preset | | | | | 200 | | | 200 | | | 200 | | | 200 | |
| | | Clock | | | | | 200 | | | 200 | | | 200 | | | 400 | |
| $I_{IH}$ | High Level Input Current | R, S, J, K, or D | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 10 | | | 10 | | | 10 | | | 10 | μA |
| | | Clear | | | | | 20 | | | 20 | | | 30 | | | 40 | |
| | | Preset | | | | | 20 | | | 20 | | | 20 | | | 20 | |
| | | Clock | | | | | −200 | | | −200 | | | 20 | | | −400 | |
| $I_{IL}$ | Low Level Input Current | R, S, J, K, or D | $V_{CC}$ = Max, $V_I$ = 0.3 V | | | | −0.18 | | | −0.18 | | | −0.18 | | | −0.18 | mA |
| | | Clear | | | | | −0.36 | | | −0.36 | | | −0.36 | | | −0.72 | |
| | | Preset | | | | | −0.36 | | | −0.36 | | | −0.18 | | | −0.36 | |
| | | Clock | | | | | −0.36 | | | −0.36 | | | −0.36 | | | −0.72 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max | | −3 | −9 | −15 | −3 | −9 | −15 | −3 | −9 | −15 | −3 | −9 | −15 | mA |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (2) | | | 0.76 | 1.44 | | 1.52 | 2.88 | | 1.6 | 3.0 | | 1.52 | 2.88 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | | To (Output) | Conditions | DM54/74 | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | L71, L72, L73, L78 | | | L74 | | | |
| | | | | | | | Min | Typ | Max | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | | | | $C_L$ = 50 pF, $R_L$ = 4 kΩ | 6 | 11 | | 6 | 11 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Preset or Clear | | Q or $\overline{Q}$ | | | 35 | 75 | | 40 | 60 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Preset or Clear | (Clock High) | $\overline{Q}$ or Q | | | 60 | 150 | | 60 | 120 | ns |
| | | | | (Clock Low) | | | | | 150 | | 60 | 120 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock | | Q or $\overline{Q}$ | | 10 | 35 | 75 | 10 | 50 | 90 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 10 | 60 | 150 | 10 | 60 | 120 | |
| $t_W$ | Pulse Width | Clock High | | | | | 100 | | | 75 | | | ns |
| | | Clock Low | | | | | 100 | | | 75 | | | |
| | | Clear or Preset Low | | | | | 100 | | | 75 | | | |
| $t_{SETUP}$ | Setup Time (3) | | | | | | 0↑ | | | 50↑ | | | ns |
| $t_{HOLD}$ | Hold Time (3) | | | | | | 0↓ | | | 15↑ | | | ns |

**Note 3:** ↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge ↓ for the falling edge.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

| Parameter | | | Conditions | | | DM54/74 LS73A, LS76A, LS107A LS112A, LS113A | | | LS74A | | | LS78A, LS114A | | | LS109A | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | DM54 | | | 0.8 | | | 0.8 | | | 0.8 | | | 0.8 | V |
| | | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | | −1.5 | | | −1.5 | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | | | −400 | | | −400 | | | −400 | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = −400 μA | | DM54 | 2.5 | 3.4 | | 2.5 | 3.4 | | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | | DM74 | 2.7 | 3.4 | | 2.7 | 3.4 | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 4 | | | 4 | | | 4 | | | 4 | mA |
| | | | | | DM74 | | | 8 | | | 8 | | | 8 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | 0.25 | 0.4 | | 0.25 | 0.4 | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | | | DM74 | | 0.35 | 0.5 | | 0.35 | 0.5 | | 0.35 | 0.5 | | 0.35 | 0.5 | |
| | | | | $I_{OL}$ = 4 mA | DM74 | | 0.25 | 0.4 | | 0.25 | 0.4 | | 0.25 | 0.4 | | 0.25 | 0.4 | |
| $I_I$ | Input Current at Maximum Input Voltage | D, J, K, or $\overline{K}$ | $V_{CC}$ = Max | $V_I$ = 7 V | | | | 0.1 | | | 0.1 | | | 0.1 | | | 0.1 | mA |
| | | Clear | | | | | | 0.3 | | | 0.2 | | | 0.6 | | | 0.2 | |
| | | Preset | | | | | | 0.3 | | | 0.2 | | | 0.3 | | | 0.2 | |
| | | Clock | | | | | | 0.4 | | | 0.1 | | | 0.8 | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | D, J, K or $\overline{K}$ | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | | 20 | | | 20 | | | 20 | | | 20 | μA |
| | | Clear | | | | | | 60 | | | 40 | | | 120 | | | 40 | |
| | | Preset | | | | | | 60 | | | 40 | | | 60 | | | 40 | |
| | | Clock | | | | | | 80 | | | 20 | | | 160 | | | 20 | |
| $I_{IL}$ | Low Level Input Current | D, J, K or $\overline{K}$ | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | | −0.4 | | | −0.4 | | | −0.4 | | | −0.4 | mA |
| | | Clear | | | | | | −0.8 | | | −0.8 | | | −1.6 | | | −0.8 | |
| | | Preset | | | | | | −0.8 | | | −0.8 | | | −0.8 | | | −0.8 | |
| | | Clock | | | | | | −0.8 | | | −0.4 | | | −1.6 | | | −0.4 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | | −20 | | −100 | −20 | | −100 | −20 | | −100 | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (3) | | | | 4 | 6 | | 4 | 8 | | 4 | 6 | | 4 | 8 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

**Note 3:** With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | To (Output) | Conditions | DM54/74 | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | LS73A, LS76A, LS78A, LS107A LS112A, LS113A, LS114A | | | LS74A | | | LS109A | | | |
| | | | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 30 | 45 | | 25 | 33 | | 25 | 33 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clear, Preset, or Clock (as appropriate) | Q or $\overline{Q}$ | | | 15 | 20 | | 17 | 25 | | 17 | 25 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 11 | 20 | | 22 | 30 | | 22 | 30 | ns |
| $t_W$ | Pulse Width | Clock High | | | | 20 | | | 18 | | | 18 | | | ns |
| | | Preset or Clear Low | | | | 25 | | | 15 | | | 15 | | | |
| $t_{SETUP}$ | Setup Time (5) | High Level Data | | | | 20↓ | | | 20↑ | | | 25↑ | | | ns |
| | | Low Level Data | | | | 20↓ | | | 20↑ | | | 20↑ | | | |
| $t_{HOLD}$ | Hold Time (5) | | | | | 0↓ | | | 0↑ | | | 0↑ | | | ns |
| $f_{MAX}$ | Maximum Clock Frequency | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 25 | 40 | | 20 | 28 | | 20 | 28 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clear, Preset, or Clock (as appropriate) | Q or $\overline{Q}$ | | | 18 | 24 | | 23 | 35 | | 23 | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 21 | 28 | | 26 | 35 | | 26 | 35 | ns |
| $t_W$ | Pulse Width | Clock High | | | | 25 | | | 25 | | | 25 | | | ns |
| | | Preset or Clear Low | | | | 30 | | | 20 | | | 20 | | | |
| $t_{SETUP}$ | Setup Time (5) | High Level Data | | | | 25↓ | | | 25↑ | | | 30↑ | | | ns |
| | | Low Level Data | | | | 25↓ | | | 25↑ | | | 25↑ | | | |
| $t_{HOLD}$ | Hold Time (5) | | | | | 5↓ | | | 0↑ | | | 0↑ | | | ns |

**Note 5:** ↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

| Parameter | | | Conditions | | DM54/74 S74 Min | S74 Typ (1) | S74 Max | S112 Min | S112 Typ (1) | S112 Max | S113 Min | S113 Typ (1) | S113 Max | S114 Min | S114 Typ (1) | S114 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.8 | | | 0.8 | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | −1.2 | | | −1.2 | | | −1.2 | | | −1.2 | V |
| $I_{OH}$ | High Level Output Current | | | | | | −1 | | | −1 | | | −1 | | | −1 | mA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −1 mA | DM54 | 2.5 | 3.4 | | 2.5 | 3.4 | | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.7 | 3.4 | | 2.7 | 3.4 | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | | | 20 | | | 20 | | | 20 | | | 20 | mA |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 20 mA | | | | 0.5 | | | 0.5 | | | 0.5 | | | 0.5 | V |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | | | 1 | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | J, K, or D | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | 50 | | | 50 | | | 50 | | | 50 | μA |
| | | Clear | | | | | 150 | | | 100 | | | N/A | | | 200 | |
| | | Preset | | | | | 100 | | | 100 | | | 100 | | | 100 | |
| | | Clock | | | | | 100 | | | 100 | | | 100 | | | 200 | |
| $I_{IL}$ | Low Level Input Current | J, K, or D | $V_{CC}$ = Max, $V_I$ = 0.5 V | | | | −2 | | | −1.6 | | | −1.6 | | | −1.6 | mA |
| | | Clear (2) | | | | | −6 | | | −7 | | | N/A | | | −14 | |
| | | Preset (2) | | | | | −4 | | | −7 | | | −7 | | | −7 | |
| | | Clock | | | | | −4 | | | −4 | | | −4 | | | −8 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (3) | | −40 | | −100 | −40 | | −100 | −40 | | −100 | −40 | | −100 | mA |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (4) | | | 30 | 50 | | 30 | 50 | | 30 | 50 | | 30 | 50 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Clear tested w/ preset high and preset tested w/ clear high.

**Note 3:** Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

**Note 4:** With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | | To (Output) | Conditions | DM54/74 S74 Min | DM54/74 S74 Typ | DM54/74 S74 Max | DM54/74 S112, S113, S114 Min | DM54/74 S112, S113, S114 Typ | DM54/74 S112, S113, S114 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | | | | | $C_L$ = 15 pF, $R_L$ = 280 Ω | 75 | 110 | | 80 | 125 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Preset or Clear | | Q or $\overline{Q}$ | | | 4 | 6 | | 4 | 7 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Preset or Clear | (Clock High) | $\overline{Q}$ or Q | | | 9 | 13.5 | | 5 | 7 | ns |
| | | | | (Clock Low) | | | | 5 | 8 | | 5 | 7 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock | | Q or $\overline{Q}$ | | | 6 | 9 | | 4 | 7 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | | 6 | 9 | | 5 | 7 | |
| $t_W$ | Pulse Width | Clock High | | | | | 6 | | | 6 | | | ns |
| | | CLock Low | | | | | 7.3 | | | 6.5 | | | |
| | | Clear or Preset Low | | | | | 7 | | | 8 | | | |
| $t_{SETUP}$ | Input Setup Time (4) | High Level Data | | | | | 3↑ | | | 3↓ | | | ns |
| | | Low Level Data | | | | | 3↑ | | | 3↓ | | | |
| $t_{HOLD}$ | Input Hold Time (4) | | | | | | 2↑ | | | 0↓ | | | ns |

**Note 4:** ↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

## Switching Characteristics (Continued)

| Parameter | | | From (Input) | | To (Output) | Conditions | DM54/74 | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | S74 | | | S112, S113, S114 | | | |
| | | | | | | | Min | Typ | Max | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | 65 | 95 | | 60 | 80 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Preset or Clear | | Q or $\overline{Q}$ | | | 6 | 9 | | 6 | 9 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Preset or Clear | (Clock High) | $\overline{Q}$ or Q | | | 12 | 16 | | 8 | 12 | ns |
| | | | | (Clock Low) | | | | 8 | 12 | | 8 | 12 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock | | Q or $\overline{Q}$ | | | 8 | 12 | | 6 | 9 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | | 9 | 13 | | 8 | 12 | |
| $t_W$ | Pulse Width | Clock High | | | | | 8 | | | 8 | | | ns |
| | | CLock Low | | | | | 9 | | | 8 | | | |
| | | Clear or Preset Low | | | | | 9 | | | 10 | | | |
| $t_{SETUP}$ | Input Setup Time (4) | High Level Data | | | | | 3↑ | | | 3↓ | | | ns |
| | | Low Level Data | | | | | 3↑ | | | 3↓ | | | |
| $t_{HOLD}$ | Input Hold Time (4) | | | | | | 2↑ | | | 0↓ | | | ns |

**Note 4:** ↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

| Parameter | | | Conditions | | DM54/74 H74 Min | DM54/74 H74 Typ (1) | DM54/74 H74 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −8 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | | −1000 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | 2.4 | 3.4 | | V |
| $I_{OL}$ | Low Level Output Current | | | | | | 20 | mA |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 20 mA | | | 0.2 | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | D | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 50 | μA |
| | | Clear | | | | | 150 | |
| | | Preset | | | | | 100 | |
| | | Clock | | | | | 100 | |
| $I_{IL}$ | Low Level Input Current | D | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −2 | mA |
| | | Clear | | | | | −4 | |
| | | Preset | | | | | −2 | |
| | | Clock | | | | | −4 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | −40 | | −100 | mA |
| $I_{CC}$ | Supply Current (Average per Flip-Flop) | | $V_{CC}$ = Max (3) | DM54 | | 15 | 21 | mA |
| | | | | DM74 | | 15 | 25 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

**Note 3:** With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | To (Output) | Conditions | DM54/74 H74 Min | DM54/74 H74 Typ | DM54/74 H74 Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | | | | $C_L$ = 25 pF, $R_L$ = 280 Ω | 35 | 43 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Preset (as applicable) | Q | | | | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $\overline{Q}$ | | | | 30 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clear (as applicable) | $\overline{Q}$ | | | | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | Q | | | | 30 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Output | | Clock | Q or $\overline{Q}$ | | | 8.5 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 13 | 20 | |
| $t_w$ | Pulse Width | Clock High | | | | 15 | | | ns |
| | | Clock Low | | | | 13.5 | | | |
| | | Clear or Preset Low | | | | 25 | | | |
| $t_{SETUP}$ | Setup Time (4) | High Level Data | | | | 10↑ | | | ns |
| | | Low Level Data | | | | 15↑ | | | |
| $t_{HOLD}$ | Hold time (4) | | | | | 5↑ | | | ns |

**Note 4:** ↑ The arrow indicates the edge of the clock pulse used for reference; ↑ for the rising edge, ↓ for the falling edge.

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## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

| Parameter | | Conditions | | | DM54/74 86 | | | DM54/74 L86 | | | DM54/74 LS86, LS386 | | | DM54/74 S86 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.7 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.7 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | N/A | | | | | | | V |
| | | | $I_I$ = −18 mA | | | | | | | N/A | | | −1.5 | | | −1.2 | |
| $I_{OH}$ | High Level Output Current | | | | | | −800 | | | −200 | | | −400 | | | −1000 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.4 | 3.4 | | 2.4 | 3.3 | | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.4 | 3.4 | | 2.4 | 3.2 | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | | | 2 | | | 4 | | | 20 | mA |
| | | | | DM74 | | | 16 | | | 3.6 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | 0.15 | 0.3 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | DM74 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 4 mA | DM74 | | | | | | | | 0.25 | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | 0.2 | | | | | | 1 | mA |
| | | | $V_I$ = 7 V | | | | | | | | | | 0.2 | | | | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | 20 | | | | | | | μA |
| | | | $V_I$ = 2.7 V | | | | | | | | | | 40 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | | | −0.36 | | | | | | | mA |
| | | | $V_I$ = 0.4 V | | | | −1.6 | | | | | | −0.6 | | | | |
| | | | $V_I$ = 0.5 V | | | | | | | | | | | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −20 | | −55 | −3 | | −15 | −20 | | −100 | −40 | | −100 | mA |
| | | | | DM74 | −18 | | −55 | −3 | | −15 | −20 | | −100 | −40 | | −100 | |
| $I_{CCH}$ | Supply Current, All Outputs High | $V_{CC}$ = Max (3) | | DM54 | | 30 | 43 | | 2.2 | 4.4 | | 6.1 | 10 | | 35 | 50 | mA |
| | | | | DM74 | | 30 | 50 | | 2.2 | 4.4 | | 6.1 | 10 | | 35 | 50 | |
| $I_{CCL}$ | Supply Current, All Outputs Low | $V_{CC}$ = Max (4) | | | | 36 | 57 | | 3.8 | 6.68 | | | | | 50 | 75 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/DM74LS and DM54S/DM74S, duration of short circuit should not exceed one second.

**Note 3:** $I_{CCH}$ is measured with all outputs open, one input of each gate at 4.5 V, and the other inputs grounded.

**Note 4:** $I_{CCL}$ is measured with all outputs open and all inputs at 4.5 V.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Device | Conditions | | $t_{PLH}$ (ns) Propagation Delay Time, Low-To-High Level Output | | | $t_{PHL}$ (ns) Propagation Delay Time, High-To-Low Level Output | | |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max |
| 86 | $C_L$ = 15 pF, $R_L$ = 400 Ω | Other Input Low | | 15 | 23 | | 11 | 17 |
| | | Other Input High | | 18 | 30 | | 13 | 22 |
| L86 | $C_L$ = 50 pF, $R_L$ = 4 kΩ | Other Input Low | | 37 | 60 | | 21 | 60 |
| | | Other Input High | | 25 | 60 | | 35 | 60 |
| LS86 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | Other Input Low | | 12 | 18 | | 10 | 17 |
| | | Other Input High | | 7 | 10 | | 6 | 12 |
| LS86 | $C_L$ = 50 pF, $R_L$ = 2 kΩ | Other Input Low | | 15 | 23 | | 14 | 21 |
| | | Other Input High | | 10 | 15 | | 10 | 15 |
| LS386 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | Other Input Low | | 12 | 18 | | 10 | 17 |
| | | Other Input High | | 7 | 10 | | 6 | 12 |
| LS386 | $C_L$ = 50 pF, $R_L$ = 2 kΩ | Other Input Low | | 15 | 23 | | 14 | 21 |
| | | Other Input High | | 10 | 15 | | 10 | 15 |
| S86 | $C_L$ = 15 pF, $R_L$ = 280 Ω | Other Input Low | | 7 | 10.5 | | 6.5 | 10 |
| | | Other Input High | | 7 | 10.5 | | 6.5 | 10 |
| S86 | $C_L$ = 50 pF, $R_L$ = 280 Ω | Other Input Low | | 9 | 14 | | 9 | 13 |
| | | Other Input High | | 9 | 14 | | 9 | 13 |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | DM54/74 | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | H103 | | | H106 | | | H108 | | | |
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −8 mA | | | −1.5 | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −500 | | | −500 | | | −500 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OH}$ = −500 μA | 2.4 | 3.4 | | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 20 | | | 20 | | | 20 | mA |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 20 mA | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | 1 | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | Any J or K | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | 50 | | | 50 | | | 50 | μA |
| | | Clear | | | | 100 | | | 100 | | | 200 | |
| | | Preset | | | | N/A | | | 100 | | | 100 | |
| | | Clock | | 0 | | −1 | 0 | | −1 | 0 | | −1 | mA |
| $I_{IL}$ | Low Level Input Current | Any J or K | $V_{CC}$ = Max, $V_I$ = 0.4 V | | −1 | −2 | | −1 | −2 | | −1 | −2 | mA |
| | | Clear | | | −1 | −2 | | −1 | −2 | | −2 | −4 | |
| | | Preset | | | | N/A | | −1 | −2 | | −1 | −2 | |
| | | Clock | | | −3 | −4.8 | | −3 | −4.8 | | −6 | −9.6 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | −40 | | −100 | −40 | | −100 | −40 | | −100 | mA |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (3) | | 40 | 76 | | 40 | 76 | | 40 | 76 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

**Note 3:** With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | | To (Output) | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | | | | | $C_L$ = 25 pF, $R_L$ = 280 Ω | 40 | 50 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Preset or Clear | | Q or $\overline{Q}$ | | | 8 | 12 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Preset or Clear | Clock High | $\overline{Q}$ or Q | | | 15 | 20 | ns |
| | | | | Clock Low | | | | 23 | 35 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock | | Q or $\overline{Q}$ | | | 10 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | | 16 | 20 | |
| $t_W$ | Pulse Width | Clock High | | | | | 10 | | | ns |
| | | Clock Low | | | | | 15 | | | |
| | | Clear or Preset Low | | | | | 16 | | | |
| $t_{SETUP}$ | Setup Time (4) | High Level Data | | | | | 10↓ | | | ns |
| | | Low Level Data | | | | | 13↓ | | | |
| $t_{HOLD}$ | Hold Time (4) | | | | | | 0↓ | | | ns |

**Note 4:** ↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

5

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 121 | | | DM54/74 LS221 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{T+}$ | Positive-Going Threshold Voltage at A Input | $V_{CC}$ = Min | | | | 1.4 | 2 | | 1.0 | 2 | V |
| $V_{T-}$ | Negative-Going Threshold Voltage at A Input | $V_{CC}$ = Min | | DM54 | 0.8 | 1.4 | | 0.8 | 1.0 | | V |
| | | | | DM74 | 0.8 | 1.4 | | 0.8 | 1.0 | | |
| $V_{T+}$ | Positive-Going Threshold Voltage at B Input | $V_{CC}$ = Min | | | | 1.55 | 2 | | 1.0 | 2 | V |
| $V_{T-}$ | Negative-Going Threshold Voltage at B Input | $V_{CC}$ = Min | | DM54 | 0.8 | 1.35 | | 0.8 | 0.9 | | V |
| | | | | DM74 | 0.8 | 1.35 | | 0.8 | 0.9 | | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | | V |
| | | | $I_I$ = −18 mA | | | | | | | −1.5 | |
| $I_{OH}$ | High Level Output Current | | | | | | −400 | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = −400 μA | | DM54 | 2.4 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.4 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | | | 4 | mA |
| | | | | DM74 | | | 16 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min | $I_{OL}$ = 4 mA | | | | | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 8 mA | DM74 | | | | | 0.35 | 0.5 | |
| | | | $I_{OL}$ = 16 mA | | | 0.2 | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | | mA |
| | | | $V_I$ = 7 V | | | | | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_O$ = 2.4 V | A1 or A2 | | | 40 | | | | μA |
| | | | | B | | | 80 | | | | |
| | | | $V_I$ = 2.7 V | All | | | | | | 20 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | A1 or A2 | | | −1.6 | | | −.4 | mA |
| | | | | B | | | −3.2 | | | −.8 | |
| | | | | Clear | | | N/A | | | −0.8 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −20 | | −55 | −20 | | −100 | mA |
| | | | | DM74 | −18 | | −55 | −20 | | −100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | Quiescent | | 13 | 25 | | 4.7 | 11 | mA |
| | | | | Triggered | | 23 | 40 | | 19 | 27 | |

**Note 1:** All typical values are $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS221/DM74LS221, duration of short circuit should not exceed one second.

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | To (Output) | DM54/74 121 Conditions | | Min | Typ | Max | DM54LS/74LS LS221 Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | A1 or A2 | Q | $C_L$ = 15 pF, $R_L$ = 400 Ω | $C_{EXT}$ = 80 pF, $R_{INT}$ to $V_{CC}$ | | 45 | 70 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | $C_{EXT}$ = 80 pF, $R_{EXT}$ = 2 kΩ | | 45 | 70 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | B | Q | | | | 35 | 55 | | | | 35 | 55 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clear | $\overline{Q}$ | | | | | N/A | | | | 45 | 65 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | A1 or A2 | $\overline{Q}$ | | | | 50 | 80 | | | | 50 | 80 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | B | $\overline{Q}$ | | | | 40 | 65 | | | | 40 | 65 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clear | Q | | | | | N/A | | | | 40 | 55 | ns |
| $t_{W(OUT)}$ | Output Pulse Width | Internal Timing Resistor (1) | A1, A2 or B | Q or $\overline{Q}$ | | $C_{EXT}$ = 80 pF, $R_{INT}$ to $V_{CC}$ | 70 | 110 | 150 | | $C_{EXT}$ = 80 pF, $R_{EXT}$ = 2 kΩ | 70 | 120 | 150 | ns |
| | | Zero-Timing Capacitance | | | | $C_{EXT}$ = 0, $R_{INT}$ to $V_{CC}$ | | 30 | 50 | | $C_{EXT}$ = 0, $R_{EXT}$ = 2 kΩ | 20 | 47 | 70 | |
| | | External Timing Resistor | | | | $C_{EXT}$ = 100 pF, $R_{EXT}$ = 10 kΩ | 600 | 700 | 800 | | $C_{EXT}$ = 100 pF, $R_{EXT}$ = 10 kΩ | 600 | 670 | 750 | |
| | | | | | | $C_{EXT}$ = 1 μF, $R_{EXT}$ = 10 kΩ | 6 | 7 | 8 | | $C_{EXT}$ = 1 μF, $R_{EXT}$ = 10 kΩ | 6 | 6.7 | 7.5 | ms |
| $t_{W(IN)}$ | Input Pulse Width | | | | | | 50 | | | | | 40 | | | ns |
| $t_{W(CLEAR)}$ | Clear Pulse Width | | | | | | N/A | | | | | 40 | | | ns |
| dv/dt | Rate of Rise or Fall of Input Pulse | Schmitt Input, B | | | | | 1 | | | | | 1 | | | V/s |
| | | Logic Input, A | | | | | 1 | | | | | 1 | | | V/μs |
| $R_{EXT}$ | External Timing Resistance | | | | | DM54 | 1.4 | | 30 | | DM54 | 1.4 | | 70 | kΩ |
| | | | | | | DM74 | 1.4 | | 40 | | DM74 | 1.4 | | 100 | |
| $C_{EXT}$ | External Timing Capacitance | | | | | | 0 | | 1000 | | | 0 | | 1000 | μF |
| $t_{SETUP}$ | Clear-Inactive State Setup Time | | | | | | | | N/A | | | 15 | | | ns |
| | Duty Cycle | | | | | $R_T$ = 2 kΩ | | | 67 | | $R_T$ = 2 kΩ | | | 67 | % |
| | | | | | | $R_T$ = Max $R_{EXT}$ | | | 90 | | $R_T$ = Max $R_T$ | | | 90 | |

**Note 1:** Use of internal timing resistor applies to DM54/74121 only.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM54/74 123 | | | DM54/74 L123A | | | DM54/74 LS122, LS123 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | DM54 | | | 0.8 | | | 0.7 | | | 0.8 | V |
| | | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | N/A | | | | V |
| | | | | $I_I$ = −18 mA | | | | | | | N/A | | | −1.5 | |
| $I_{OH}$ | High Level Output Current | | | | | | | −800 | | | −200 | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $I_{OH}$ = Max (3) | | DM54 | 2.4 | 3.4 | | 2.4 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | | DM74 | 2.4 | 3.4 | | 2.4 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 16 | | | 2.0 | | | 4 | mA |
| | | | | | DM74 | | | 16 | | | 3.6 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min (3) | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | 0.22 | 0.3 | | 0.25 | 0.4 | V |
| | | | | | DM74 | | 0.2 | 0.4 | | | 0.4 | | 0.35 | 0.5 | |
| | | | | $I_{OL}$ = 4 mA | DM74 | | | | | | | | 0.25 | 0.4 | |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | 0.1 | | | | mA |
| | | | | $V_I$ = 7 V | | | | | | | | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | Data Inputs | $V_{CC}$ = Max | | $V_I$ = 2.4 V | | | 40 | | | 10 | | | | μA |
| | | | | | $V_I$ = 2.7 V | | | | | | | | | 20 | |
| | | Clear Input | | | $V_I$ = 2.4 V | | | 80 | | | 10 | | | | |
| | | | | | $V_I$ = 2.7 V | | | | | | | | | 20 | |
| $I_{IL}$ | Low Level Input Current | Data Inputs | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | | −1.6 | | | −0.18 | | | −0.4 | mA |
| | | Clear Input | | | | | | −1.6 | | | −0.18 | | | −0.4 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) (3) | | | −10 | | −40 | −2.5 | | −12 | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current (Quiescent or Triggered) | | $V_{CC}$ = Max (4) (5) (6) | | LS122 | | | | | | | | 6 | 11 | mA |
| | | | | | Others | | 46 | 66 | | 5 | 7.5 | | 12 | 20 | |

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | To (Output) | DM54/74 123 Conditions | Min | Typ | Max | DM54/74 L123A Conditions | Min | Typ | Max | DM54/74 LS122, LS123 Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | A | Q | $C_{EXT}$ = 0, $R_{EXT}$ = 5 kΩ, $C_L$ = 15 pF, $R_L$ = 400 Ω | | 22 | 33 | $C_{EXT}$ = 0, $R_{EXT}$ = 32 kΩ, $C_L$ = 50 pF, $R_L$ = 4 kΩ | | 120 | 175 | $C_{EXT}$ = 0, $R_{EXT}$ = 5 kΩ, $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 22 | 33 | ns |
| | | | B | | | | 19 | 28 | | | 86 | 135 | | | 29 | 44 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | A | $\overline{Q}$ | | | 30 | 40 | | | 120 | 180 | | | 30 | 45 | ns |
| | | | B | | | | 27 | 36 | | | 86 | 135 | | | 37 | 56 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clear | Q | | | 18 | 27 | | | 45 | 65 | | | 18 | 27 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | | $\overline{Q}$ | | | 30 | 40 | | | 95 | 140 | | | 30 | 45 | |
| $t_{WQ(MIN)}$ | Minimum Width of Pulse at Output Q | | A or B | Q | | | 45 | 65 | | | 220 | 330 | | | 116 | 200 | ns |
| $t_{WQ}$ | Width of Pulse at Output Q | | A or B | Q | $C_{EXT}$ = 1000 pF, $R_{EXT}$ = 10 kΩ, $C_L$ = 15 pF, $R_L$ = 400 Ω | 3.08 | 3.42 | 3.76 | $C_{EXT}$ = 1000 pF, $R_{EXT}$ = 100 kΩ, $C_L$ = 50 pF, $R_L$ = 4 kΩ | 30.6 | 34.0 | 37.4 | $C_{EXT}$ = 1000 pF, $R_{EXT}$ = 10 kΩ, $C_L$ = 15 pF, $R_L$ = 2 kΩ | 4 | 4.5 | 5 | μs |
| $t_W$ | Pulse Width | A or B Inputs High | | | | 40 | | | | 130 | | | | 40 | | | ns |
| | | A or B Inputs Low | | | | 40 | | | | 130 | | | | 40 | | | |
| | | Clear Low | | | | 40 | | | | 130 | | | | 40 | | | |
| $R_{EXT}$ | External Timing Resistance | DM54 | | | | 5 | | 25 | | 5 | | 200 | | 5 | | 180 | kΩ |
| | | DM74 | | | | 5 | | 50 | | 5 | | 400 | | 5 | | 260 | |
| $C_{EXT}$ | External Capacitance | | | | | No Restriction | | | | No Restriction | | | | No Restriction | | | |
| $C_{WIRE}$ | Wiring Capacitance at $R_{EXT}/C_{EXT}$ Terminal | DM54 | | | | | | 50 | | | | 40 | | | | 50 | pF |
| | | DM74 | | | | | | 50 | | | | 50 | | | | 50 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

**Note 3:** Ground $R_{EXT}/C_{EXT}$ and Input A, apply 2.4 V to the B Input to measure the following: $V_{OH}$ or $I_{OS}$ at the Q output or $V_{OL}$ at the $\overline{Q}$ output.

**Note 4:** Quiescent $I_{CC}$ is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, $C_{EXT}$ = 0.02 μF, and $R_{EXT}$ = 25 kΩ.

**Note 5:** $I_{CC}$ is measured in the triggered state with 2.4 V applied to all clear and B inputs. A inputs grounded, all outputs open, $C_{EXT}$ = 0.02 μF, and $R_{EXT}$ = 25 kΩ.

**Note 6:** With all outputs open and 4.5 V applied to all data and clear inputs, $I_{CC}$ is measured after a momentary ground, then 4.5 V, is applied to clock (LS122, LS123).

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 125, 126 | | | DM54/74 LS125A, LS126A | | | DM54/74 S134 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Inut Voltage | | | DM54 | | | 0.8 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | | | | | V |
| | | | $I_I$ = −18 mA | | | | | | | −1.5 | | | −1.2 | |
| $I_{OH}$ | High Level Output Current | | | DM54 | | | −2.0 | | | −1.0 | | | −6.5 | mA |
| | | | | DM74 | | | −5.2 | | | −2.6 | | | −6.5 | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.4 | 3.3 | | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| | | | | DM74 | 2.4 | 3.1 | | 2.4 | 3.1 | | 2.4 | 3.2 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | | | 12 | | | 20 | mA |
| | | | | DM74 | | | 16 | | | 24 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | | 0.4 | | | 0.4 | | | 0.5 | V |
| | | | | DM74 | | | 0.4 | | | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 12 mA | DM74 | | | | | | 0.4 | | | | |
| $I_{O(OFF)}$ | Off-State (High Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V | $V_{IL}$ = 0.8 V | $V_O$ = 0.4 V | | | | | | −20 | | | | μA |
| | | | | $V_O$ = 2.4 V | | | | | | 20 | | | | |
| | | | $V_{IL}$ = 0.8 V | $V_O$ = 0.4 V | | | −40 | | | | | | | |
| | | | | $V_O$ = 0.5 V | | | | | | | | | −50 | |
| | | | | $V_O$ = 2.4 V | | | 40 | | | | | | 50 | |
| $I_{I(OFF)}$ | Off-State (High Impedance State) Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V (0.5 V for DM54S/74S) | | | | | −40 | | | −20 | | | −50 | μA |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | | | | 1 | mA |
| | | | $V_I$ = 7.0 V | | | | | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | | | | | μA |
| | | | $V_I$ = 2.7 V | | | | | | | 20 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.4 V | | | | −1.6 | | | −0.4 | | | | mA |
| | | | $V_I$ = 0.5 V | | | | | | | | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −30 | | −70 | −20 | | −100 | −40 | | −100 | mA |
| | | | | DM74 | −28 | | −70 | −20 | | −100 | −40 | | −100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | See Table | | | | | | | | | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/DM74LS and DM54S/74S, duration of short circuit should not exceed one second.

## Supply Currents

| Device | Conditions | | $I_{CC}$ (mA) | | |
|---|---|---|---|---|---|
| | Data Inputs | Output Controls | Min | Typ (1) | Max |
| 125 | 0 V | 4.5 V | | 32 | 54 |
| 126 | 0 V | 0 V | | 36 | 62 |
| LS125A | 0 V | 4.5 V | | 11 | 20 |
| LS126A | 0 V | 0 V | | 12 | 22 |
| S134 | 0 V | 0 V | | 7 | 13 |
| | 5 V | 0 V | | 9 | 16 |
| | 5 V | 5 V | | 14 | 25 |

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Paramater | | Conditions | DM54/74 125 Min | DM54/74 125 Typ | DM54/74 125 Max | DM54/74 126 Min | DM54/74 126 Typ | DM54/74 126 Max | Conditions | DM54/74 S134 Min | DM54/74 S134 Typ | DM54/74 S134 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $C_L$ = 50 pF, $R_L$ = 400 Ω | | 10 | 15 | | 10 | 15 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 4 | 6 | ns |
| | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 5.5 | 9 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | 12 | 18 | | 12 | 18 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 5 | 7.5 | ns |
| | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 7 | 11 | |
| $t_{ZH}$ | Output Enable Time to High Level | | | 12 | 18 | | 13 | 19 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 13 | 19.5 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | 16 | 25 | | 16 | 25 | | | 14 | 21 | ns |
| $t_{HZ}$ | Output Disable Time From High Level | $C_L$ = 5 pF, $R_L$ = 400 Ω | | 5 | 8 | | 10 | 16 | $C_L$ = 5 pF, $R_L$ = 280 Ω | | 5.5 | 8.5 | ns |
| $t_{LZ}$ | Output Disable Time From Low Level | | | 9 | 14 | | 14 | 20 | | | 9 | 14 | ns |

## Switching Characteristics (Continued)

| Parameter | | Conditions | DM54LS/74LS LS125A Min | LS125A Typ | LS125A Max | LS126A Min | LS126A Typ | LS126A Max | Conditions | DM54LS/74LS LS125A Min | LS125A Typ | LS125A Max | LS126A Min | LS126A Typ | LS126A Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low to High Level Output | $C_L$ = 50 pF, $R_L$ = 667 Ω | | 10 | 15 | | 10 | 15 | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 14 | 21 | | 14 | 21 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | 10 | 18 | | 10 | 18 | | | 15 | 22 | | 15 | 22 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | | | 19 | 25 | | 22 | 30 | | | 23 | 35 | | 24 | 36 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | 16 | 25 | | 19 | 30 | | | 26 | 40 | | 28 | 42 | ns |
| $t_{HZ}$ | Output Disable Time From High Level | $C_L$ = 5 pF, $R_L$ = 667 Ω | | 10 | 20 | | 10 | 25 | | | | | | | | ns |
| $t_{LZ}$ | Output Disable Time From Low Level | | | 12 | 20 | | 14 | 25 | | | | | | | | ns |

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## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM54/74 S135 Min | DM54/74 S135 Typ (1) | DM54/74 S135 Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | −1.2 | V |
| $I_{OH}$ | High Level Output Current | | | | | −1 | mA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −1 mA | DM54 | 2.5 | 3.4 | | V |
| | | | DM74 | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | | 20 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = 20 mA | | | | 0.5 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | 50 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.5 V | | | | −2 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −40 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | | 65 | 99 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

**Note 3:** $I_{CC}$ is measured with the inputs grounded and the outputs open.

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter (4) | | From (Input) | Conditions | | DM54/74 S135 Min | DM54/74 S135 Typ | DM54/74 S135 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A or B | B or A = L, C = L | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 8.5 | 13 | ns |
| | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 11.5 | 16 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 11 | 15 | |
| | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 14 | 18 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A or B | B or A = H, C = L | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 8 | 12 | ns |
| | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 11 | 15 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 9 | 13.5 | |
| | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 12 | 16.5 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A or B | B or A = L, C = H | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 10 | 15 | ns |
| | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 13 | 18 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 6.5 | 10 | |
| | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 9.5 | 13 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A or B | B or A = H, C = H | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 8.5 | 12 | ns |
| | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 11.5 | 15 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 7 | 11 | |
| | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 10 | 14 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | C | A = B | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 8 | 12 | ns |
| | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 11 | 15 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 9.5 | 14.5 | |
| | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 12.5 | 17.5 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | C | A ≠ B | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 7.5 | 11.5 | ns |
| | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 10.5 | 14.5 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 8 | 12 | |
| | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 11 | 15 | |

5

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| | Parameter | Conditions | | | DM54/74 LS136, LS266 | | | DM54/74 S136 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | | −1.5 | | | −1.2 | V |
| $I_{CEX}$ | High Level Output Current | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $V_{OH}$ = 5.5 V | | | | | 100 | | | 250 | μA |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 4 | | | 20 | mA |
| | | | | DM74 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | DM74 | | 0.35 | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 4 mA | DM74 | | | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | | | | 1 | mA |
| | | | $V_I$ = 7 V | | | | 0.2 | | | | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | | 40 | | | 50 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.4 V | | | | −0.6 | | | | mA |
| | | | $V_I$ = 0.5 V | | | | | | | −2 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (2) | | LS136 | | 6.1 | 10 | | | | mA |
| | | | | Others | | 8 | 13 | | 50 | 75 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** $I_{CC}$ is measured with one input of each gate at 4.5 V, the other inputs grounded, and the outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| | Parameter | From (Input) | Conditions | | DM54/74 LS136, LS266 | | DM54/74 S136 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Typ | Max | Conditions | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A or B | Other Input Low | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 18 | 30 | $C_L$ = 15 pF, $R_L$ = 280 Ω | 8 | 12.5 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | 18 | 30 | | 7.5 | 12 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A or B | Other Input High | | 18 | 30 | | 8 | 12.5 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | 18 | 30 | | 7.5 | 12 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A or B | Other Input Low | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 21 | 36 | $C_L$ = 50 pF, $R_L$ = 280 Ω | 10 | 14.5 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | 24 | 40 | | 9.5 | 14 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A or B | Other Input High | | 21 | 36 | | 10 | 14.5 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | 24 | 40 | | 9.5 | 14 | |

# Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

## General Description

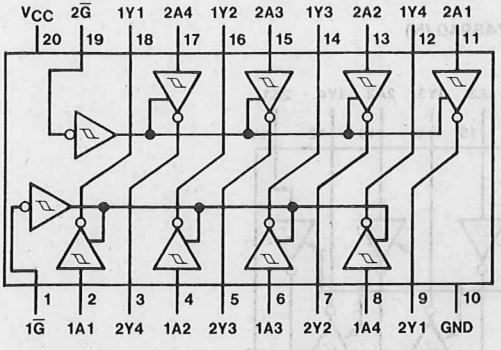
These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE® buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs, and can be used to drive terminated lines down to 133 Ω.

## Features

- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at inputs improves noise margins

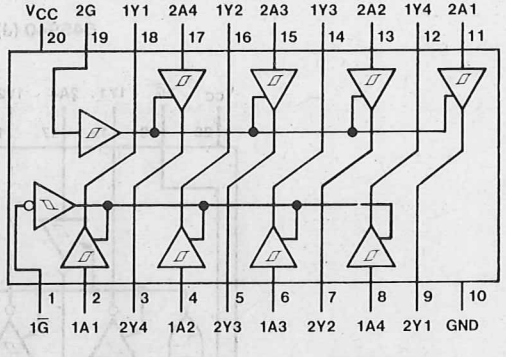
| | Typical $I_{OL}$ (Sink Current) | Typical $I_{OH}$ (Source Current) | Typical Propagation Delay Times | | Typical Enable/ Disable Times | Typical Power Dissipation (Enabled) | |
|---|---|---|---|---|---|---|---|
| | | | Inverting | Noninverting | | Inverting | Noninverting |
| 54LS | 12 mA | −12 mA | 10.5 ns | 12 ns | 18 ns | 130 mW | 135 mW |
| 74LS | 24 mA | −15 mA | 10.5 ns | 12 ns | 18 ns | 130 mW | 135 mW |
| 54S | 48 mA | −12 mA | 4.5 ns | 6 ns | 9 ns | 450 mW | 538 mW |
| 74S | 64 mA | −15 mA | 4.5 ns | 6 ns | 9 ns | 450 mW | 538 mW |

## Connection Diagrams



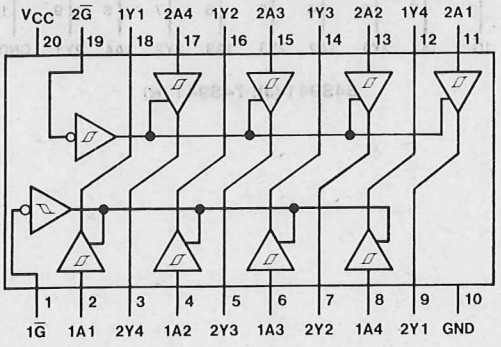

**54LS240 (J)**
**54S240 (J)**

**74LS240 (N)**
**74S240 (N)**




**54LS241 (J)**
**54S241 (J)**

**74LS241 (N)**
**74S241 (N)**

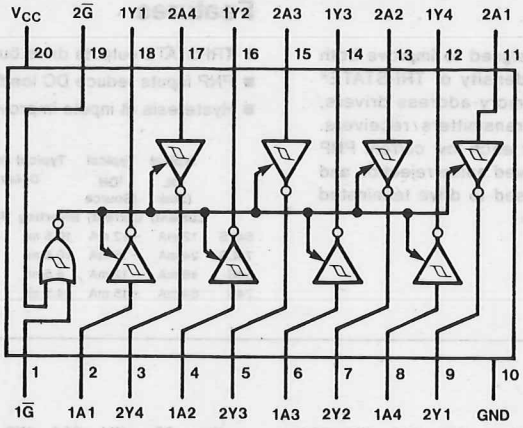



**54LS244 (J)**
**54S244 (J)**

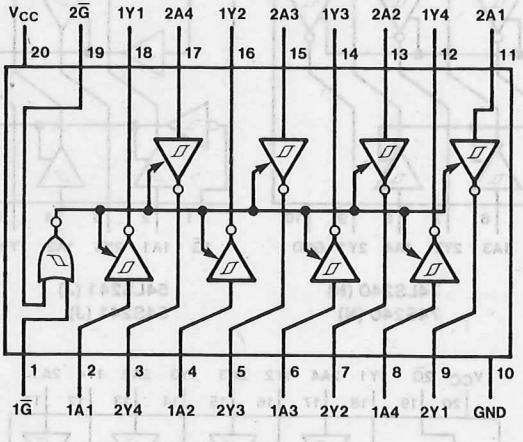
**74LS244 (N)**
**74S244 (N)**

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## Connection Diagrams (Continued)




**54S940 (J); 74S940 (N)**




**54S941 (J); 74S941 (N)**

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM54/74 LS240, LS241 LS244 | | | DM54/74 S240, S241, S244 S940, S941 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | | −1.5 | | | −1.2 | V |
| | Hysteresis ($V_{T+} - V_{T-}$) | | $V_{CC}$ = Min | | | 0.2 | 0.4 | | 0.2 | 0.4 | | V |
| $I_{OH}$ | High Level Output Current | | | | DM54 | | | −12 | | | −12 | mA |
| | | | | | DM74 | | | −15 | | | −15 | |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −1 mA | | | 2.7 | | | 2.7 | | | V |
| | | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −3 mA | | | 2.4 | 3.4 | | 2.4 | 3.4 | | |
| | | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.5 V, $I_{OH}$ = Max | | | 2 | | | 2 | | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 12 | | | 48 | mA |
| | | | | | DM74 | | | 24 | | | 64 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2 V | $I_{OL}$ = 12 mA | | | | 0.4 | | | | V |
| | | | | $I_{OL}$ = Max | DM54 | | | 0.4 | | | 0.55 | |
| | | | | | DM74 | | | 0.5 | | | | |
| $I_{OZH}$ | Off-State Output Current High Level Voltage Applied | | $V_{CC}$ = Max, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2 V | $V_O$ = 2.7 V | | | | 20 | | | | μA |
| | | | | $V_O$ = 2.4 V | | | | | | | 50 | |
| $I_{OZL}$ | Off-State Output Current, Low Level Voltage Applied | | | $V_O$ = 0.4 V | | | | −20 | | | | |
| | | | | $V_O$ = 0.5 V | | | | | | | −50 | |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max | $V_I$ = 7 V | | | | 0.1 | | | | mA |
| | | | | $V_I$ = 5.5 V | | | | | | | 1 | |
| $I_{IH}$ | High Level Input Current | | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | | 20 | | | 50 | μA |
| $I_{IL}$ | Low Level Input Current | | $V_{CC}$ = Max | $V_I$ = 0.4 V | | | | −0.2 | | | | mA |
| | | | | $V_I$ = 0.5 V | Any A | | | | | | −400 | μA |
| | | | | | Any G | | | | | | −2 | mA |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | | −40 | | −225 | −50 | | −225 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max Outputs Open | Outputs High | LS240, 241, 244 | | | 13 | 23 | | | | mA |
| | | | | S240 S940 | DM54 | | | | | 80 | 123 | |
| | | | | | DM74 | | | | | 80 | 135 | |
| | | | | S241, 244 S941 | DM54 | | | | | 95 | 147 | |
| | | | | | DM74 | | | | | 95 | 160 | |
| | | | Outputs Low | LS240 | | | 26 | 44 | | | | |
| | | | | LS241, 244 | | | 27 | 46 | | | | |
| | | | | S240 S940 | DM54 | | | | | 100 | 145 | |
| | | | | | DM74 | | | | | 100 | 150 | |
| | | | | S241, 244 S941 | DM54 | | | | | 120 | 170 | |
| | | | | | DM74 | | | | | 120 | 180 | |
| | | | Outputs Disabled | LS240 | | | 29 | 50 | | | | |
| | | | | LS241, 244 | | | 32 | 54 | | | | |
| | | | | S240 S940 | DM54 | | | | | 100 | 145 | |
| | | | | | DM74 | | | | | 100 | 150 | |
| | | | | S241, 244 S941 | DM54 | | | | | 120 | 170 | |
| | | | | | DM74 | | | | | 120 | 180 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time and duration should not exceed one second.

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## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| | Parameter | Conditions | | | DM54/74 LS240, LS241 LS244 | | | DM54/74 S240, S241, S244 S940, S941 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $t_{pLH}$ | Propagation Delay Time Low to High Level Output | $C_L$ = 45 pF | $R_L$ = 667 Ω | LS240 | 3 | 9 | 14 | | | | ns |
| | | | | LS241, 244 | 5 | 12 | 18 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 2 | 4.5 | 7 | |
| | | | | S241, 244, 941 | | | | 2 | 6 | 9 | |
| $t_{pHL}$ | Propagation Delay Time High to Low Level Output | $C_L$ = 45 pF | $R_L$ = 667 Ω | LS240 | 5 | 12 | 18 | | | | ns |
| | | | | LS241, 244 | 7 | 12 | 18 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 2 | 4.5 | 7 | |
| | | | | S241, 244, 941 | | | | 2 | 6 | 9 | |
| $t_{pZL}$ | Output Enable Time to Low Level | $C_L$ = 45 pF | $R_L$ = 667 Ω | LS240 | 10 | 20 | 30 | | | | ns |
| | | | | LS241, 244 | 10 | 20 | 30 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 3 | 10 | 15 | |
| | | | | S241, 244, 941 | | | | 3 | 10 | 15 | |
| $t_{pZH}$ | Output Enable Time to High Level | $C_L$ = 45 pF | $R_L$ = 667 Ω | LS240 | 5 | 15 | 23 | | | | ns |
| | | | | LS241, 244 | 10 | 15 | 23 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 2 | 6.5 | 10 | |
| | | | | S241, 244, 941 | | | | 3 | 8 | 12 | |
| $t_{pLZ}$ | Output Disable Time from Low Level | $C_L$ = 5 pF | $R_L$ = 667 Ω | LS240 | 7 | 15 | 25 | | | | ns |
| | | | | LS241, 244 | 8 | 15 | 25 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 4 | 10 | 15 | |
| | | | | S241, 244, 941 | | | | 2 | 10 | 15 | |
| $t_{pHZ}$ | Output Disable Time from High Level | $C_L$ = 5 pF | $R_L$ = 667 Ω | LS240 | 5 | 10 | 18 | | | | ns |
| | | | | LS241, 244 | 5 | 10 | 18 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 2 | 6 | 9 | |
| | | | | S241, 244, 941 | | | | 2 | 6 | 9 | |
| $t_{pLH}$ | Propagation Delay Time Low to High Level Output | $C_L$ = 150 pF | $R_L$ = 667 Ω | LS240 | 5 | 11 | 18 | | | | ns |
| | | | | LS241, 244 | 6 | 14 | 21 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 3 | 7 | 10 | |
| | | | | S241, 244, 941 | | | | 4 | 9 | 12 | |
| $t_{pHL}$ | Progapation Delay Time High to Low Level Output | $C_L$ = 150 pF | $R_L$ = 667 Ω | LS240 | 6 | 15 | 22 | | | | ns |
| | | | | LS241, 244 | 6 | 15 | 22 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 3 | 7 | 10 | |
| | | | | S241, 244, 941 | | | | 4 | 9 | 12 | |
| $t_{pZL}$ | Output Enable Time to Low Level | $C_L$ = 150 pF | $R_L$ = 667 Ω | LS240 | 12 | 22 | 33 | | | | ns |
| | | | | LS241, 244 | 12 | 22 | 33 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 6 | 14 | 21 | |
| | | | | S241, 244, 941 | | | | 6 | 14 | 21 | |
| $t_{pZH}$ | Output Enable Time to High Level | $C_L$ = 150 pF | $R_L$ = 667 Ω | LS240 | 6 | 18 | 26 | | | | ns |
| | | | | LS241, 244 | 11 | 18 | 26 | | | | |
| | | | $R_L$ = 90 Ω | S240, 940 | | | | 4 | 9 | 12 | |
| | | | | S241, 244, 941 | | | | 4 | 10 | 15 | |

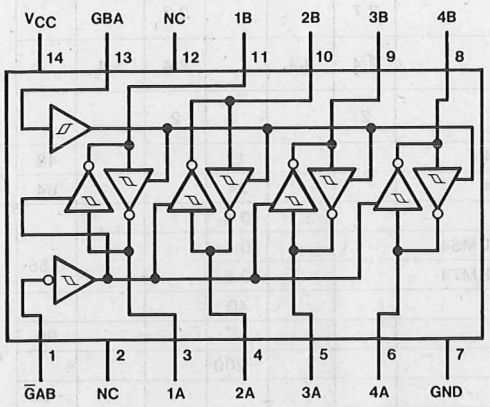
# Quadruple Bus Transceivers

## General Description

These four data line transceivers are designed for asynchronous two-way communications between data buses. They can be used to drive terminated lines down to 133 ohms.

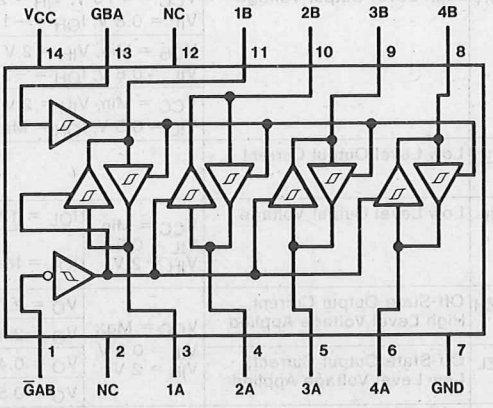
- Two-Way Asynchronous Communication Between Data Buses
- P-N-P Inputs Reduce D-C Loading
- Hysteresis (Typically 400 mV) at Inputs Improves Noise Margin

## Connection Diagrams




54LS242 (J)
54S242 (J)

74LS242 (N)
74S242 (N)




54LS243 (J)
54S243 (J)

74LS243 (N)
74S243 (N)

## Truth Table

| Control Inputs | | LS242 S242 Data Port Status | | LS243 S243 Data Port Status | |
|---|---|---|---|---|---|
| $\overline{G}AB$ | GBA | A | B | A | B |
| H | H | $\overline{O}$ | I | O | I |
| L | H | * | * | * | * |
| H | L | ISOLATED | | ISOLATED | |
| L | L | I | $\overline{O}$ | I | O |

*Possibly destructive oscillation may occur if the transceivers are enabled in both directions at once.

I = Input, O = Output, $\overline{O}$ = Inverting Output.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM54/74 LS242, LS243 Min | DM54/74 LS242, LS243 Typ (1) | DM54/74 LS242, LS243 Max | DM54/74 S242, S243 Min | DM54/74 S242, S243 Typ (1) | DM54/74 S242, S243 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | | −1.5 | | | −1.2 | V |
| | Hysteresis ($V_{T+}-V_{T-}$) | | $V_{CC}$ = Min | | | 0.2 | 0.4 | | 0.2 | 0.4 | | V |
| $I_{OH}$ | High Level Output Current | | | | DM54 | | | −12 | | | −12 | mA |
| | | | | | DM74 | | | −15 | | | −15 | |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −1 mA | | | 2.7 | | | 2.7 | | | V |
| | | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −3 mA | | | 2.4 | 3.4 | | 2.4 | 3.4 | | |
| | | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.5 V, $I_{OH}$ = Max | | | 2 | | | 2 | | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 12 | | | 48 | mA |
| | | | | | DM74 | | | 24 | | | 64 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2 V | $I_{OL}$ = 12 mA | | | | 0.4 | | | | V |
| | | | | $I_{OL}$ = Max | DM54 | | | 0.4 | | | 0.55 | |
| | | | | | DM74 | | | 0.5 | | | | |
| $I_{OZH}$ | Off-State Output Current, High Level Voltage Applied | | $V_{CC}$ = Max, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2 V | $V_O$ = 2.7 V | | | | 40 | | | | μA |
| | | | | $V_O$ = 2.4 V | | | | | | | 50 | |
| $I_{OZL}$ | Off-State Output Current, Low Level Voltage Applied | | | $V_O$ = 0.4 V | | | | −200 | | | | |
| | | | | $V_O$ = 0.5 V | | | | | | | −50 | |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max | $V_I$ = 5.5 V | A or B | | | 0.1 | | | | mA |
| | | | | $V_I$ = 7 V | Any G | | | 0.1 | | | | |
| | | | | $V_I$ = 5.5 V | Any | | | | | | 1 | |
| $I_{IH}$ | High Level Input Current | | $V_{CC}$ = Max | $V_I$ = 2.7 V | | | | 20 | | | 50 | μA |
| $I_{IL}$ | Low Level Input Current | | $V_{CC}$ = Max | $V_I$ = 0.4 V | | | | −0.2 | | | | mA |
| | | | | $V_I$ = 0.5 V | Any A | | | | | | −400 | μA |
| | | | | | Any G | | | | | | −2 | mA |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | | −40 | | −225 | −50 | | −225 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max, Outputs Open | Outputs High | LS242, 243 | | | 22 | 38 | | | | mA |
| | | | | S242 | DM54 | | | | | 80 | 123 | |
| | | | | | DM74 | | | | | 80 | 135 | |
| | | | | S243 | DM54 | | | | | 95 | 147 | |
| | | | | | DM74 | | | | | 95 | 160 | |
| | | | Outputs Low | LS242, 243 | | | 29 | 50 | | | | |
| | | | | S242 | DM54 | | | | | 100 | 145 | |
| | | | | | DM74 | | | | | 100 | 150 | |
| | | | | S243 | DM54 | | | | | 120 | 170 | |
| | | | | | DM74 | | | | | 120 | 180 | |
| | | | Outputs Disabled | LS242 | | | 29 | 50 | | | | |
| | | | | LS243 | | | 32 | 54 | | | | |
| | | | | S242 | DM54 | | | | | 100 | 145 | |
| | | | | | DM74 | | | | | 100 | 150 | |
| | | | | S243 | DM54 | | | | | 120 | 170 | |
| | | | | | DM74 | | | | | 120 | 180 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time and duration should not exceed one second.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | | | DM54/74 LS242, LS243 | | | DM54/74 S242, S243 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | $C_L$ = 45 pF | $R_L$ = 667 Ω | LS242 | 3 | 9 | 14 | | | | ns |
| | | | | LS243 | 5 | 12 | 18 | | | | |
| | | | $R_L$ = 90 Ω | S242 | | | | 2 | 4.5 | 7 | |
| | | | | S243 | | | | 2 | 6 | 9 | |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | $C_L$ = 45 pF | $R_L$ = 667 Ω | LS242 | 5 | 12 | 18 | | | | |
| | | | | LS243 | 7 | 12 | 18 | | | | |
| | | | $R_L$ = 90 Ω | S242 | | | | 2 | 4.5 | 7 | |
| | | | | S243 | | | | 2 | 6 | 9 | |
| $t_{PZL}$ | Output Enable Time to Low Level | $C_L$ = 45 pF | $R_L$ = 667 Ω | LS242 | 10 | 20 | 30 | | | | |
| | | | | LS243 | 10 | 20 | 30 | | | | |
| | | | $R_L$ = 90 Ω | S242 | | | | 3 | 10 | 15 | |
| | | | | S243 | | | | 3 | 10 | 15 | |
| $t_{PZH}$ | Output Enable Time to High Level | $C_L$ = 45 pF | $R_L$ = 667 Ω | LS242 | 5 | 15 | 23 | | | | |
| | | | | LS243 | 10 | 15 | 23 | | | | |
| | | | $R_L$ = 90 Ω | S242 | | | | 2 | 6.5 | 10 | |
| | | | | S243 | | | | 3 | 8 | 12 | |
| $t_{PLZ}$ | Output Disable Time from Low Level | $C_L$ = 5 pF | $R_L$ = 667 Ω | LS242 | 7 | 15 | 25 | | | | |
| | | | | LS243 | 8 | 15 | 25 | | | | |
| | | | $R_L$ = 90 Ω | S242 | | | | 4 | 10 | 15 | |
| | | | | S243 | | | | 2 | 10 | 15 | |
| $t_{PHZ}$ | Output Disable Time from High Level | $C_L$ = 5 pF | $R_L$ = 667 Ω | LS242 | 5 | 10 | 18 | | | | |
| | | | | LS243 | 5 | 10 | 18 | | | | |
| | | | $R_L$ = 90 Ω | S242 | | | | 2 | 6 | 9 | |
| | | | | S243 | | | | 2 | 6 | 9 | |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | $C_L$ = 150 pF | $R_L$ = 667 Ω | LS242 | 5 | 11 | 18 | | | | ns |
| | | | | LS243 | 6 | 14 | 21 | | | | |
| | | | $R_L$ = 90 Ω | S242 | | | | 3 | 7 | 10 | |
| | | | | S243 | | | | 4 | 9 | 12 | |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | $C_L$ = 150 pF | $R_L$ = 667 Ω | LS242 | 6 | 15 | 22 | | | | |
| | | | | LS243 | 6 | 15 | 22 | | | | |
| | | | $R_L$ = 90 Ω | S242 | | | | 3 | 7 | 10 | |
| | | | | S243 | | | | 4 | 9 | 12 | |
| $t_{PZL}$ | Output Enable Time to Low Level | $C_L$ = 150 pF | $R_L$ = 667 Ω | LS242 | 12 | 22 | 33 | | | | |
| | | | | LS243 | 12 | 22 | 33 | | | | |
| | | | $R_L$ = 90 Ω | S242 | | | | 6 | 14 | 21 | |
| | | | | S243 | | | | 6 | 14 | 21 | |
| $t_{PZH}$ | Output Enable Time to High Level | $C_L$ = 150 pF | $R_L$ = 667 Ω | LS242 | 6 | 18 | 26 | | | | |
| | | | | LS243 | 11 | 18 | 26 | | | | |
| | | | $R_L$ = 90 Ω | S242 | | | | 4 | 9 | 12 | |
| | | | | S243 | | | | 4 | 10 | 15 | |

5

# TRI-STATE® Octal Bus Transceiver

## General Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

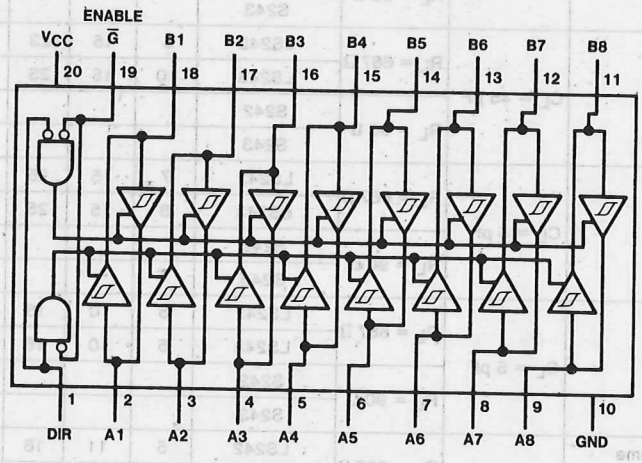
The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

## Features

- Bi-directional bus transceiver in a high-density 20-pin package
- Tri-state outputs drive bus lines directly
- P-N-P inputs reduce D-C loading on bus lines
- Hysteresis at bus inputs improve noise margins
- Typical propagation delay times, port-to-port . . . 8 ns
- Typical enable/disable times . . . 17ns

| Type | $I_{OL}$ (Sink Current) | $I_{OH}$ (Source Current) |
|---|---|---|
| 54LS245 | 12 mA | −12 mA |
| 74LS245 | 24 mA | −15 mA |

## Connection Diagram




54LS245 (J); 74LS245 (N)

## Truth Table

| Enable $\overline{G}$ | Direction Control DIR | Operation |
|---|---|---|
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

H = high level, L = low level, X = irrelevant

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 LS245 Min | DM54/74 LS245 Typ (1) | DM54/74 LS245 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | | −1.5 | V |
| | Hysteresis ($V_{T+} - V_{T-}$) | $V_{CC}$ = Min | | | 0.2 | 0.4 | | V |
| $I_{OH}$ | High Level Output Current | | | DM54 | | | −12 | mA |
| | | | | DM74 | | | −15 | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −1 mA | | | 2.7 | | | V |
| | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −3 mA | | | 2.4 | 3.4 | | |
| | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.5 V, $I_{OH}$ = Max | | | 2 | | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 12 | mA |
| | | | | DM74 | | | 24 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2 V | $I_{OL}$ = 12 mA | DM74 | | | 0.4 | V |
| | | | $I_{OL}$ = Max | DM54 | | | 0.4 | |
| | | | | DM74 | | | 0.5 | |
| $I_{OZH}$ | Off-State Output Current, High Level Voltage Applied | $V_{CC}$ = Max, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2 V | $V_O$ = 2.7 V | | | | 10 | μA |
| $I_{OZL}$ | Off-State Output Current, Low Level Voltage Applied | | $V_O$ = 0.4 V | | | | −200 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | A or B | $V_I$ = 5.5 V | | | 0.1 | mA |
| | | | DIR or $\overline{G}$ | $V_I$ = 7 V | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | | 20 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | | −0.2 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | | −40 | | −225 | mA |
| $I_{CC}$ | Supply Current | Outputs High | $V_{CC}$ = Max | | | 48 | 70 | mA |
| | | Outputs Low | | | | 62 | 90 | |
| | | Outputs at Hi-Z | | | | 64 | 95 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output shorted at a time, not to exceed one second duration.

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## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| | Parameter | Conditions | DM54/74 LS245 Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High-Level Output | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 8 | 12 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low-Level Output | | | 8 | 12 | ns |
| $t_{PZL}$ | Output Enable Time to Low Level | | | 27 | 40 | ns |
| $t_{PZH}$ | Output Enable Time to High Level | | | 25 | 40 | ns |
| $t_{PLZ}$ | Output Disable Time from Low Level | $C_L$ = 5 pF, $R_L$ = 667 Ω | | 15 | 25 | ns |
| $t_{PHZ}$ | Output Disable Time from High Level | | | 15 | 25 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High-Level Output | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 10 | 16 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low-Level Output | | | 11 | 17 | ns |
| $t_{PZL}$ | Output Enable Time to Low Level | | | 30 | 45 | ns |
| $t_{PZH}$ | Output Enable Time to High Level | | | 30 | 45 | ns |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 LS279 Min | DM54/74 LS279 Typ (1) | DM54/74 LS279 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = −400 μA | | DM54 | 2.5 | 3.5 | | V |
| | | | | DM74 | 2.7 | 3.5 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 4 | mA |
| | | | | DM74 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = 4 mA | | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 8 mA | DM74 | | 0.35 | 0.5 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 7 V | | | | | 0.1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | | 20 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | | −0.4 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | | | 3.8 | 7 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.
**Note 3:** $I_{CC}$ is measured with all $\overline{R}$ inputs grounded, all $\overline{S}$ inputs at 4.5 V, and all outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output From $\overline{S}$ Input | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 12 | 22 | ns |
| | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 15 | 25 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From $\overline{S}$ Input | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 9 | 15 | ns |
| | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 15 | 23 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From $\overline{R}$ Input | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 15 | 27 | ns |
| | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 21 | 33 | |

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## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

| Parameter | | | Conditions | | | DM54/74 365, 366, 367, 368 | | | DM54/74 LS365A, LS366A, LS367A, LS368A | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ(1) | Max | Min | Typ(1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | DM54 | | | 0.8 | | | 0.8 | V |
| | | | | | DM74 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | | V |
| | | | | $I_I$ = −18 mA | | | | | | | −1.5 | |
| $I_{OH}$ | High Level Output Current | | | | DM54 | | | −2.0 | | | −1.0 | mA |
| | | | | | DM74 | | | −5.2 | | | −2.6 | |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.4 | 3.1 | | 2.4 | 3.4 | | V |
| | | | | | DM74 | 2.4 | 3.1 | | 2.4 | 3.1 | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 32 | | | 12 | mA |
| | | | | | DM74 | | | 32 | | | 24 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = 12 mA | | | | | | | 0.4 | V |
| | | | | $I_{OL}$ = 24 mA | | | | | | | 0.5 | |
| | | | | $I_{OL}$ = 32 mA | | | | 0.4 | | | | |
| $I_{O(OFF)}$ | Off-State (High Impedance State) Output Current | | $V_{CC}$ = Max, $V_{IH}$ = 2 V | $V_O$ = 0.4 V | | | | −40 | | | −20 | μA |
| | | | | $V_O$ = 2.4 V | | | | 40 | | | | |
| | | | | $V_O$ = 2.4 V | | | | | | | 20 | |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | | mA |
| | | | | $V_I$ = 7.0 V | | | | | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | | μA |
| | | | | $V_I$ = 2.7 V | | | | | | | 20 | |
| $I_{IL}$ | Low Level Input Current | A Input | $V_{CC}$ = Max | $V_I$ = 0.5 V, Both $\overline{G}$ Inputs at 2 V | | | | −40 | | | −20 | μA |
| | | | | $V_I$ = 0.4 V, Both $\overline{G}$ Inputs at 0.4 V | | | | −1.6 | | | −0.4 | mA |
| | | $\overline{G}$ Input | | $V_I$ = 0.4 V | | | | −1.6 | | | −0.4 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | | −40 | | −115 | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (3) | 365, LS365, 367, LS367 | | | 65 | 85 | | 14 | 24 | mA |
| | | | | 366, LS366, 368, LS368 | | | 59 | 77 | | 12 | 21 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

**Note 3:** $I_{CC}$ is measured with data inputs at GND and output controls at 4.5 V.

## Switching Characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | DM54/74 Conditions | DM54/74 365, 367 Typ | DM54/74 365, 367 Max | DM54/74 366, 368 Typ | DM54/74 366, 368 Max | DM54/74 Conditions | DM54/74 LS365, LS367 Typ | DM54/74 LS365, LS367 Max | DM54/74 LS366, LS368 Typ | DM54/74 LS366, LS368 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $C_L$ = 50 pF, $R_L$ = 400 Ω | 10 | 16 | 11 | 17 | $C_L$ = 50 pF, $R_L$ = 667 Ω | 10 | 16 | 10 | 15 | ns |
| | | | | | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | 15 | 25 | 15 | 25 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | 14 | 22 | 10 | 16 | $C_L$ = 50 pF, $R_L$ = 667 Ω | 10 | 16 | 10 | 18 | ns |
| | | | | | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | 16 | 25 | 16 | 25 | |
| $t_{ZH}$ | Output Enable Time to High Level | | 21 | 35 | 21 | 35 | $C_L$ = 50 pF, $R_L$ = 667 Ω | 16 | 30 | 11 | 30 | ns |
| | | | | | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | 25 | 40 | 20 | 35 | |
| $t_{ZL}$ | Output Enable Time to Low Level | | 24 | 37 | 24 | 37 | $C_L$ = 50 pF, $R_L$ = 667 Ω | 14 | 30 | 18 | 30 | ns |
| | | | | | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | 25 | 40 | 30 | 40 | |
| $t_{HZ}$ | Output Disable Time From High Level | $C_L$ = 5 pF, $R_L$ = 400 Ω | 6 | 11 | 6 | 11 | $C_L$ = 5 pF, $R_L$ = 667 Ω | 10 | 20 | 10 | 20 | ns |
| $t_{LZ}$ | Output Disable Time From Low Level | | 16 | 27 | 16 | 27 | | 11 | 20 | 10 | 20 | ns |

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## Switching Characteristics at $V_{CC}$ = 5V, $T_A$ = 25°C

| Parameter | | DM54/74 | | | | | | DM54A/74A | | | | | | LS365, LS367, LS368, LS369 | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 365, 367 | | | 366, 368 | | | 365, 367 | | | 366, 368 | | | Conditions | | | | | | |
| | | Typ | Max | | Typ | Max | | Typ | Max | | Typ | Max | | | Typ | Max | | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | 10 | 15 | | 11 | 17 | | | | | | | | $C_L$ = 50 pF<br>$R_L$ = 667 Ω | 10 | 15 | | 10 | 15 | ns |
| | | | | | | | | | | | | | | $C_L$ = 150 pF<br>$R_L$ = 667 Ω | 15 | 25 | | 15 | 25 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | 14 | 22 | | 10 | 15 | | | | | | | | $C_L$ = 50 pF<br>$R_L$ = 667 Ω | 10 | 18 | | 10 | 18 | ns |
| | | | | | | | | | | | | | | $C_L$ = 150 pF<br>$R_L$ = 667 Ω | 15 | 25 | | 15 | 25 | |
| $t_{ZH}$ | Output Enable Time to High Level | 21 | 35 | | 21 | 35 | | | | | | | | $C_L$ = 50 pF<br>$R_L$ = 667 Ω | 15 | 30 | | 11 | 20 | ns |
| | | | | | | | | | | | | | | $C_L$ = 150 pF<br>$R_L$ = 667 Ω | 25 | 40 | | 20 | 35 | |
| $t_{ZL}$ | Output Enable Time to Low Level | 24 | 37 | | 24 | 37 | | | | | | | | $C_L$ = 50 pF<br>$R_L$ = 667 Ω | 14 | 30 | | 18 | 30 | ns |
| | | | | | | | | | | | | | | $C_L$ = 150 pF<br>$R_L$ = 667 Ω | 25 | 40 | | 30 | 40 | |
| $t_{HZ}$ | Output Disable Time From High Level | 8 | 11 | | 8 | 11 | | | | | | | | $C_L$ = 5 pF<br>$R_L$ = 667 Ω | 10 | 20 | | 10 | 20 | ns |
| $t_{LZ}$ | Output Disable Time From Low Level | 16 | 27 | | 16 | 27 | | | | | | | | | 11 | 20 | | 10 | 20 | ns |

# Section 6
# 54/74 MSI Device Specifications

6


| TEMPERATURE RANGE | | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| −55°C to +125°C | 0°C to +70°C | | |
| DM5441A | DM7441A | BCD/Decimal Decoders/Drivers | 6-4 |
| DM5442 | DM7442 | BCD/Decimal Decoders | 6-7 |
| DM54L42A | DM74L42A | BCD/Decimal Decoders | 6-7 |
| DM544LS42 | DM74LS42 | BCD/Decimal Decoders | 6-7 |
| DM5445 | DM7445 | BCD/Decimal Decoders/Drivers | 6-10 |
| DM5446A | DM7446A | BCD/7-Segment Decoders/Drivers | 6-12 |
| DM5447A | DM7447A | BCD/7-Segment Decoders/Drivers | 6-12 |
| DM54LS47 | DM74LS47 | BCD/7-Segment Decoders/Drivers | 6-12 |
| DM5448 | DM7448 | BCD/7-Segment Decoders/Drivers | 6-12 |
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# BCD/Decimal Decoders/Drivers

## General Description

The DM5441A/DM7441A is a BCD-to-decimal decoder designed to drive gas-filled NIXIE tubes. The device is also capable of driving other types of low-current lamps and relays.

An over-range decoding feature provides that if binary numbers between 10 and 15 are applied to the input, the least significant bit (0-5) will be decoded on the output.

The DM54141/DM74141 is a BCD-to-decimal decoder designed to drive cold-cathode indicator tubes.

Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the DM54141/DM74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display.

Input clamp diodes are also provided to clamp negative-voltage transitions in order to minimize transmission-line effects.

## Features

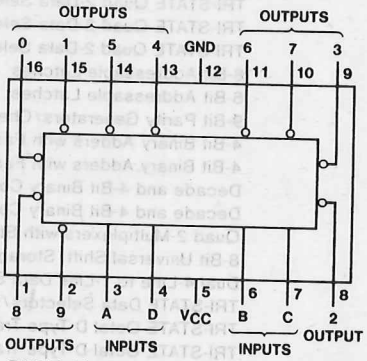
- Drive cold-cathode, numeric indicator tubes directly
- Fully decoded inputs
- Low leakage current

| | |
|---|---|
| DM54/7441A | 1.8 μA @ 50 V |
| DM54/74141 | 50 μA @ 55 V |

- Low power dissipation

| | |
|---|---|
| DM54/7441A | 105 mW typical |
| DM54/74141 | 55 mW typical |

## Connection Diagram




5441A (J,W)
54141 (J,W)

7441A (N)
74141 (N)

## Truth Tables

**5441A/7441A**

| Input | | | | Output On* |
|---|---|---|---|---|
| D | C | B | A | |
| L | L | L | L | 0 |
| L | L | L | H | 1 |
| L | L | H | L | 2 |
| L | L | H | H | 3 |
| L | H | L | L | 4 |
| L | H | L | H | 5 |
| L | H | H | L | 6 |
| L | H | H | H | 7 |
| H | L | L | L | 8 |
| H | L | L | H | 9 |
| (Over Range) | | | | |
| H | L | H | L | 0 |
| H | L | H | H | 1 |
| H | H | L | L | 2 |
| H | H | L | H | 3 |
| H | H | H | L | 4 |
| H | H | H | H | 5 |

**54141/74141**

| Input | | | | Output On* |
|---|---|---|---|---|
| D | C | B | A | |
| L | L | L | L | 0 |
| L | L | L | H | 1 |
| L | L | H | L | 2 |
| L | L | H | H | 3 |
| L | H | L | L | 4 |
| L | H | L | H | 5 |
| L | H | H | L | 6 |
| L | H | H | H | 7 |
| H | L | L | L | 8 |
| H | L | L | H | 9 |
| (Over Range) | | | | |
| H | L | H | L | None |
| H | L | H | H | None |
| H | H | L | L | None |
| H | H | L | H | None |
| H | H | H | L | None |
| H | H | H | H | None |

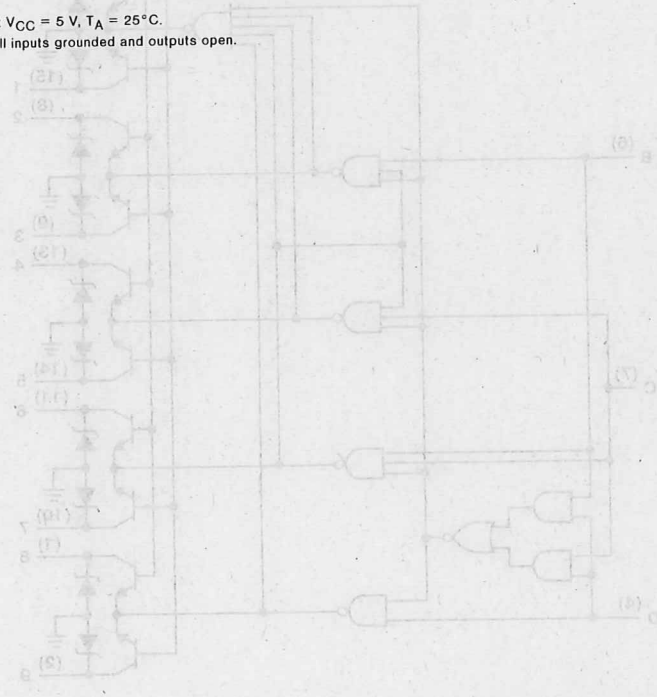
H = High Level, L = Low Level
*All other outputs are off

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 41A | | | 141 | | | |
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | | N/A | | | −1.5 | V |
| $V_{OL}$ | On-State Output Voltage | $V_{CC}$ = Min, $I_O$ = 7 mA | −55°C to +70°C | | | | 2.5 | | | 2.5 | V |
| | | | 125°C | | | | 3.0 | | | 3.0 | |
| $I_{OH}$ | Off-State Reverse Current | $V_{CC}$ = Min | $V_O$ = 50 V | $T_A$ = 125°C | | | 60 | | | | μA |
| | | | | $T_A$ = 70°C | | | 40 | | | | |
| | | | | $T_A$ = −55°C 0°C, 25°C | | | 1.8 | | | | |
| | | | $V_O$ = 55 V | | | | | | | 50 | |
| $I_{OH}$ | Off-State Reverse Current for Input Counts 10-15 | $V_{CC}$ = Min, $V_O$ = 30 V | | $T_A$ = 55°C | | | N/A | | | 5 | μA |
| | | | | $T_A$ = 70°C | | | N/A | | | 15 | |
| $V_{OH}$ | Off-State Output Voltage | $V_{CC}$ = Min | $I_O$ = 0.5 mA | | | | | 60 | | | V |
| | | | $I_O$ = 1.0 mA | | 70 | | | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | | 1 | | | 1.0 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | A Input | | 3 | 40 | | | 40 | μA |
| | | | | B, C, or D Input | | 3 | 40 | | | 80 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | A Input | | −1.0 | −1.6 | | | −1.6 | mA |
| | | | | B, C, or D Input | | −1.0 | −1.6 | | | −3.2 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (2) | | | | 21 | 36 | | 11 | 25 | mA |

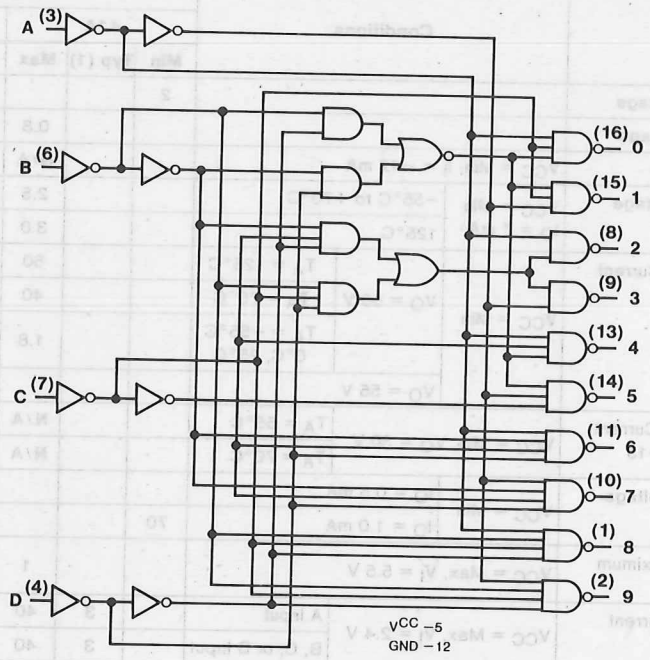
**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** $I_{CC}$ is measured with all inputs grounded and outputs open.

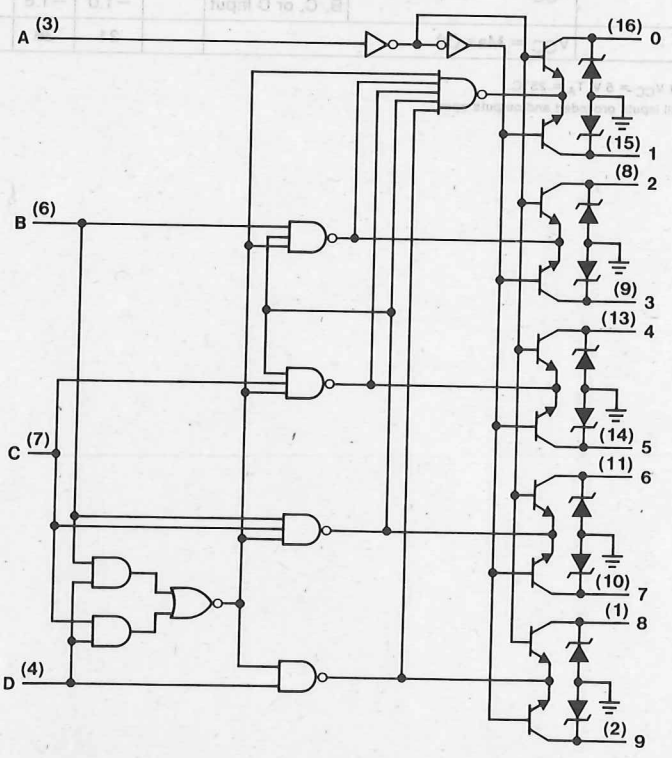


## Logic Diagrams

5441A/7441A




54141/74141



# BCD/Decimal Decoders

## General Description

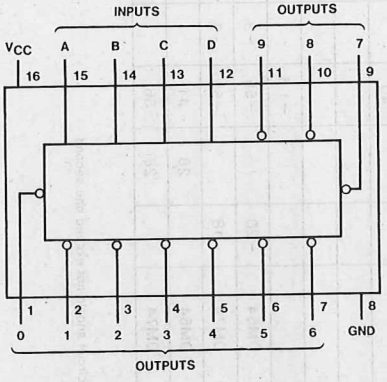
These BCD-to-decimal decoders consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of input logic ensures that all outputs remain off for all invalid (10-15) input conditions.

## Features

- Diode clamped inputs
- Also for application as 4-line-to-16-line decoders; 3-line-to-8-line decoders
- All outputs are high for invalid input conditions

| Type | Typical Power Dissipation | Typical Propagation Delay |
|---|---|---|
| 42 | 140 mW | 17 ns |
| L42A | 15 mW | 53 ns |
| LS42 | 35 mW | 17 ns |

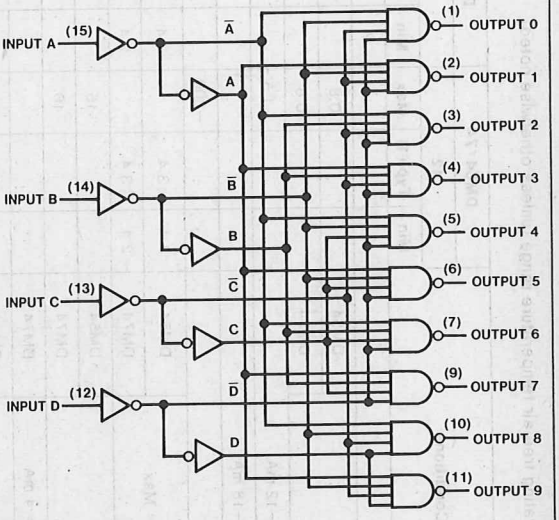
## Connection Diagram




5442 (J,W)
54L42A (J,W)
54LS42 (J,W)

7442 (N)
74L42A (N)
74LS42 (N)

## Logic Diagram




## Truth Table

| No. | 42, L42A, LS42 BCD Input D | C | B | A | All Types Decimal Output 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | L | L | L | L | L | H | H | H | H | H | H | H | H | H |
| 1 | L | L | L | H | H | L | H | H | H | H | H | H | H | H |
| 2 | L | L | H | L | H | H | L | H | H | H | H | H | H | H |
| 3 | L | L | H | H | H | H | H | L | H | H | H | H | H | H |
| 4 | L | H | L | L | H | H | H | H | L | H | H | H | H | H |
| 5 | L | H | L | H | H | H | H | H | H | L | H | H | H | H |
| 6 | L | H | H | L | H | H | H | H | H | H | L | H | H | H |
| 7 | L | H | H | H | H | H | H | H | H | H | H | L | H | H |
| 8 | H | L | L | L | H | H | H | H | H | H | H | H | L | H |
| 9 | H | L | L | H | H | H | H | H | H | H | H | H | H | L |
| INVALID | H | L | H | L | H | H | H | H | H | H | H | H | H | H |
| | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

H = High Level
L = Low Level

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## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 42 | | | DM54/74 L42A | | | DM54/74 LS42 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.7 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.7 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | N/A | | | | V |
| | | | $I_I$ = −18 mA | | | | | | | N/A | | | −1.5 | |
| $I_{OH}$ | High Level Output Current | | | | | | −800 | | | −200 | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OH}$ = Max | DM54 | 2.4 | 3.4 | | 2.4 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.4 | 3.4 | | 2.4 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | | | 2 | | | 4 | mA |
| | | | | DM74 | | | 16 | | | 3.6 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = 4 mA | DM74 | | | | | | | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | 0.15 | 0.3 | | 0.25 | 0.4 | |
| | | | | DM74 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.35 | 0.5 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | 0.1 | | | | mA |
| | | | $V_I$ = 7 V | | | | | | | | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | 10 | | | | μA |
| | | | $V_I$ = 2.7 V | | | | | | | | | | 20 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.3 V for L42A | | | | | | | −0.18 | | | | mA |
| | | | $V_I$ = 0.4 V for Others | | | | −1.6 | | | | | | −0.4 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −20 | | −55 | −3 | | −15 | −20 | | −100 | mA |
| | | | | DM74 | −18 | | −55 | −3 | | −15 | −20 | | −100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | DM54 | | 28 | 41 | | 3.0 | 5.3 | | 7 | 13 | mA |
| | | | | DM74 | | 28 | 56 | | 3.0 | 5.3 | | 7 | 13 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

**Note 3:** $I_{CC}$ is measured with all outputs open and all inputs grounded.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | DM54/74 42 Min | DM54/74 42 Typ | DM54/74 42 Max | Conditions | DM54/74 L42A Min | DM54/74 L42A Typ | DM54/74 L42A Max | Conditions | DM54/74 LS42 Min | DM54/74 LS42 Typ | DM54/74 LS42 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From A, B, C, or D Through 2 Levels of Logic | $C_L$ = 15 pF, $R_L$ = 400Ω | | 14 | 25 | $C_L$ = 50 pF, $R_L$ = 4 kΩ | | 65 | 130 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 14 | 25 | ns |
| | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 20 | 30 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From A, B, C, or D Through 3 Levels of Logic | | | 17 | 30 | | | 70 | 140 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 17 | 30 | ns |
| | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 23 | 35 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output From A, B, C, or D Through 2 Levels of Logic | | | 10 | 25 | | | 30 | 60 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 10 | 25 | ns |
| | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 15 | 30 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output From A, B, C, or D Through 3 Levels of Logic | | | 17 | 30 | | | 35 | 70 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 17 | 30 | ns |
| | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 23 | 35 | |

# BCD/Decimal Decoders/Drivers

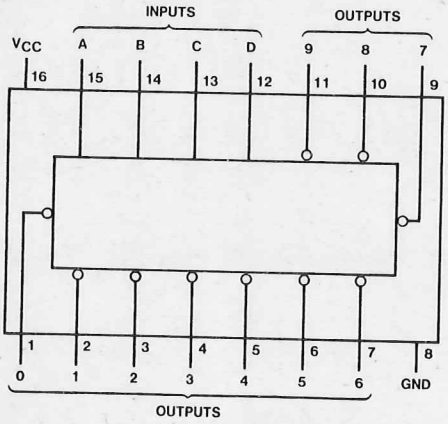
## General Description

These BCD-to-decimal decoders/drivers consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of BCD input logic ensures that all outputs remain off for all invalid (10-15) binary input conditions. These decoders feature high-performance, NPN output transistors designed for use as indicator/relay drivers, or as open-collector logic-circuit drivers. The high-breakdown output transistors are compatible for interfacing with most MOS integrated circuits.

## Features

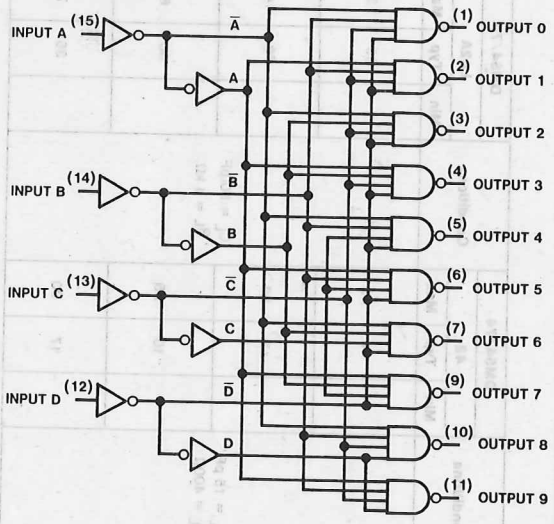
- Full decoding of input logic
- 80 mA sink-current capability
- All outputs are off for invalid BCD input conditions

## Connection Diagram




5445 (J,W) 7445 (N)
54145 (J,W) 74145 (N)

## Logic Diagram




## Truth Table

| No. | Inputs | | | | Outputs | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0 | L | L | L | L | L | H | H | H | H | H | H | H | H | H |
| 1 | L | L | L | H | H | L | H | H | H | H | H | H | H | H |
| 2 | L | L | H | L | H | H | L | H | H | H | H | H | H | H |
| 3 | L | L | H | H | H | H | H | L | H | H | H | H | H | H |
| 4 | L | H | L | L | H | H | H | H | L | H | H | H | H | H |
| 5 | L | H | L | H | H | H | H | H | H | L | H | H | H | H |
| 6 | L | H | H | L | H | H | H | H | H | H | L | H | H | H |
| 7 | L | H | H | H | H | H | H | H | H | H | H | L | H | H |
| 8 | H | L | L | L | H | H | H | H | H | H | H | H | L | H |
| 9 | H | L | L | H | H | H | H | H | H | H | H | H | H | L |
| INVALID | H | L | H | L | H | H | H | H | H | H | H | H | H | H |
| | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

H = High Level (Off), L = Low Level (On)

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 45,145 Min | DM54/74 45,145 Typ (1) | DM54/74 45,145 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | | −1.5 | V |
| $V_{O(ON)}$ | On-State Output Voltage | $V_{CC}$ Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $I_{O(ON)}$ = 80 mA | | | 0.5 | 0.9 | V |
| | | | $I_{O(ON)}$ = 20 mA | | | | 0.4 | |
| $V_{O(OFF)}$ | Off-State Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{O(OFF)}$ = 250 μA | | 45 | 30 | | | V |
| | | | | 145 | 15 | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | | −1.6 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (2) | | DM54 | | 43 | 62 | mA |
| | | | | DM74 | | 43 | 70 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** $I_{CC}$ is measured with all inputs grounded and outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | DM54/74 45, 145 Min | DM54/74 45, 145 Typ | DM54/74 45, 145 Max | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $C_L$ = 15 pF, $R_L$ = 100 Ω | | | 30 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | 30 | ns |

# BCD/7-Segment Decoders/Drivers

## General Description

The 46A, 47A and LS47 feature active-low outputs designed for driving common-anode LED's or incandescent indicators directly; and the 48, LS48 and LS49 feature active-high outputs for driving lamp buffers or common-cathode LED's. All of the circuits except the LS49 have full ripple-blanking input/output controls and a lamp test input. The LS49 features a direct blanking input. Segment identification and resultant displays are shown on a following page. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

All of the circuits except the LS49 incorporate automatic leading and/or trailing-edge, zero-blanking control (RBI and RBO). Lamp test (LT) of these devices may be performed at any time when the BI/RBO node is at a high logic level. All types (including LS49) contain an overriding blanking input (BI) which can be used to control the lamp intensity (by pulsing), or to inhibit the outputs.

## Features

- All circuit types feature lamp intensity modulation capability

**5446A/7446A, 5447A/7447A, 54LS47/74LS47**

- Open-collector outputs drive indicators directly
- Lamp-test provision
- Leading/trailing zero suppression

**5448/7448, 54LS48/74LS48**

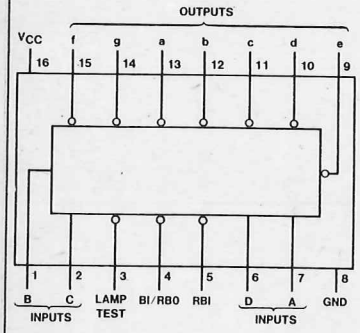
- Internal pull-ups eliminate need for external resistors
- Lamp-test provision
- Leading/trailing zero suppression

**54LS49/74LS49**

- Open-collector outputs
- Blanking input

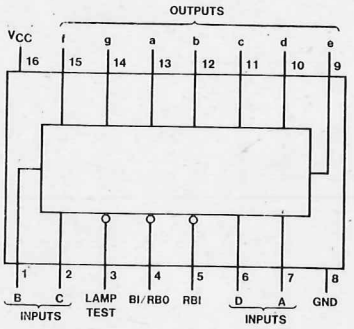
| Type | Driver Outputs | | | | Typical Power Dissipation | Packages |
|---|---|---|---|---|---|---|
| | Active Level | Output Configuration | Sink Current | Max Voltage | | |
| DM5446A | low | open-collector | 40 mA | 30 V | 320 mW | J,W |
| DM5447A | low | open-collector | 40 mA | 15 V | 320 mW | J,W |
| DM5448 | high | 2 kΩ pull-up | 6.4 mA | 5.5 V | 265 mW | J,W |
| DM54LS47 | low | open-collector | 12 mA | 15 V | 35 mW | J,W |
| DM54LS48 | high | 2 kΩ pull-up | 2 mA | 5.5 V | 125 mW | J,W |
| DM54LS49 | high | open-collector | 4 mA | 5.5 V | 40 mW | J,W |
| DM7446A | low | open-collector | 40 mA | 30 V | 320 mW | N |
| DM7447A | low | open-collector | 40 mA | 15 V | 320 mW | N |
| DM7448 | high | 2 kΩ pull-up | 6.4 mA | 5.5 V | 265 mW | N |
| DM74LS47 | low | open-collector | 24 mA | 15 V | 35 mW | N |
| DM74LS48 | high | 2 kΩ pull-up | 6 mA | 5.5 V | 125 mW | N |
| DM74LS49 | high | open-collector | 8 mA | 5.5 V | 40 mW | N |

## Connection Diagrams



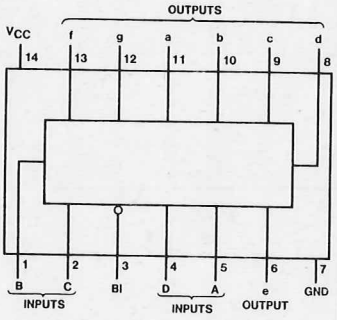

**5446A (J,W)**
**5447A (J,W)**
**54LS47 (J,W)**

**7446A (N)**
**7447A (N)**
**74LS47 (N)**




**5448A (J,W)**
**54LS48 (J,W)**

**7448A (N)**
**74LS48 (N)**




**54LS49 (J,W); 74LS49 (N)**

## Electrical Characteristcs over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM54/74 46A, 47A Min | DM54/74 46A, 47A Typ (1) | DM54/74 46A, 47A Max | DM54/74 48 Min | DM54/74 48 Typ (1) | DM54/74 48 Max | DM54/74 LS47 Min | DM54/74 LS47 Typ (1) | DM54/74 LS47 Max | DM54/74 LS48 Min | DM54/74 LS48 Typ (1) | DM54/74 LS48 Max | DM54/74 LS49 Min | DM54/74 LS49 Typ (1) | DM54/74 LS49 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | DM54 | | | 0.8 | | | 0.8 | | | 0.7 | | | 0.7 | | | 0.7 | V |
| | | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.8 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | | | | | | | | | | V |
| | | | | $I_I$ = −18 mA | | | | | | | | | | −1.5 | | | −1.5 | | | −1.5 | |
| $I_{OH}$ | High Level Output Current | a thru g | $V_{CC}$ = Min, $V_{IH}$ = 2 V | | | | | | | | −400 | | | | | | −100 | | | | μA |
| | | BI/RBO | $V_{IL}$ = Max | | | | | −200 | | | −200 | | | −50 | | | −50 | | | 250 | |
| | | | $V_{OH}$ = 5.5 V | | | | | | | | | | | | | | | | | | |
| $V_{OH}$ | High Level Output Voltage | a thru g | $V_{CC}$ = Min, $V_{IH}$ = 2 V | | | | | | 2.4 | 4.2 | | | | | 2.4 | 4.2 | | | | 5.5 | V |
| | | BI/RBO | $V_{IL}$ = Max, $I_{OH}$ = Max | | | 2.4 | 3.7 | | 2.4 | 3.7 | | 2.4 | 4.2 | | 2.4 | 4.2 | | | | N/A | |
| $I_{OL}$ | Low Level Output Current | a thru g | | | DM54 | | | 40 | | | 6.4 | | | 12 | | | 2 | | | 4 | mA |
| | | | | | DM74 | | | 40 | | | 6.4 | | | 24 | | | 6 | | | 8 | |
| | | BI/RBO | | | DM54 | | | 8 | | | 8 | | | 1.6 | | | 1.6 | | | N/A | |
| | | | | | DM74 | | | 8 | | | 8 | | | 3.2 | | | 3.2 | | | N/A | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | 0.3 | 0.4 | | 0.27 | 0.4 | | 0.25 | 0.4 | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | | | DM74 | | 0.3 | 0.4 | | 0.27 | 0.4 | | 0.35 | 0.5 | | 0.35 | 0.5 | | 0.35 | 0.5 | |
| | | | | $I_{OL}$ = Max/2 DM74 Only | | | N/A | | | N/A | | | 0.25 | 0.4 | | | N/A | | 0.25 | 0.4 | |
| | | | | $I_{OL}$ = 2 mA DM74 Only | | | N/A | | | N/A | | | | N/A | | 0.25 | 0.4 | | N/A | | |
| $I_{O(OFF)}$ | Off-State Output Current | a thru g | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $V_{O(OFF)}$ = Max | | | | 0.25 | | | | | | 0.25 | | | | | N/A | | mA |
| | | | | $V_O$ = 0.85 V | | | | | −1.3 | −2 | | | | | −1.3 | −2 | | | | | |
| $V_{O(OFF)}$ | Off-State Output Voltage | a thru g | | 46A | | | | 30 | | | | | | | | | | | | | V |
| | | | | Others | | | | 15 | | | 5.5 | | | 15 | | | 5.5 | | | 5.5 | |
| $I_I$ | Input Current at Maximum Input Voltage | Any Input Except BI/RBO | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | 1 | | | | | | | | | | mA |
| | | | | $V_I$ = 7 V | | | | | | | | | | 0.1 | | | 0.1 | | | 0.1 | |
| | | BI/RBO | | $V_I$ = 7 V | | | | | | | | | | 0.1 | | | | | | N/A | |
| $I_{IH}$ | High Level Input Current | Any Input Except BI/RBO | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | 40 | | | | | | | | | | μA |
| | | | | $V_I$ = 2.7 V | | | | | | | | | | 20 | | | 20 | | | 20 | |
| | | BI/RBO | | $V_I$ = 2.7 V | | | | | | | | | | 20 | | | | | | N/A | |
| $I_{IL}$ | Low Level Input Current | Any Input Except BI/RBO | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | | −1.6 | | | −1.6 | | | −0.36 | | | −0.36 | | | −0.36 | mA |
| | | BI/RBO | | | | | | −4 | | | −4 | | | −1 | | | −1 | | | N/A | |
| $I_{OS}$ | Short Circuit Output Current | BI/RBO | $V_{CC}$ = Max | | | | | −4 | | | −4 | −0.3 | | −2 | −0.3 | | −2 | | | N/A | mA |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (2) | | DM54 | | 60 | 85 | | 50 | 76 | | 7 | 13 | | 25 | 38 | | 8 | 15 | mA |
| | | | | | DM74 | | 60 | 103 | | 50 | 90 | | 7 | 13 | | 25 | 38 | | 8 | 15 | |

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Device | Conditions | $t_{PLH}$ and $t_{PHL}$ (ns) Propagation Delay Time From A Input | | | $t_{PLH}$ and $t_{PHL}$ (ns) Propagation Delay Time From RBI Input | | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max |
| 46A, 47A | $C_L$ = 15 pF, $R_L$ = 120 Ω | | | 100 | | | 100 |
| 48 | $C_L$ = 15 pF, $R_L$ = 1 kΩ | | | 100 | | | 100 |
| LS47 | $C_L$ = 15 pF, $R_L$ = 665 Ω | | | 100 | | | 100 |
| LS48 | $C_L$ = 15 pF, $R_L$ = 4 kΩ | | | 100 | | | |
| | $C_L$ = 15 pF, $R_L$ = 6 kΩ | | | | | | 100 |
| LS49 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | | 100 | | | |
| | $C_L$ = 15 pF, $R_L$ = 6 kΩ | | | | | | 100 |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** $I_{CC}$ is measured with all outputs open and all inputs at 4.5 V.

## Output Display

NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS




SEGMENT IDENTIFICATION



## Truth Tables

### 46A, 47A, LS47

| Decimal or Function | Inputs | | | | | | BI/RBO(1) | Outputs | | | | | | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LT | RBI | D | C | B | A | | a | b | c | d | e | f | g | |
| 0 | H | H | L | L | L | L | H | L | L | L | L | L | L | H | (2) |
| 1 | H | X | L | L | L | H | H | H | L | L | H | H | H | H | |
| 2 | H | X | L | L | H | L | H | L | L | H | L | L | H | L | |
| 3 | H | X | L | L | H | H | H | L | L | L | L | H | H | L | |
| 4 | H | X | L | H | L | L | H | H | L | L | H | H | L | L | |
| 5 | H | X | L | H | L | H | H | L | H | L | L | H | L | L | |
| 6 | H | X | L | H | H | L | H | H | H | L | L | L | L | L | |
| 7 | H | X | L | H | H | H | H | L | L | L | H | H | H | H | |
| 8 | H | X | H | L | L | L | H | L | L | L | L | L | L | L | |
| 9 | H | X | H | L | L | H | H | L | L | L | H | H | L | L | |
| 10 | H | X | H | L | H | L | H | H | H | H | L | L | H | L | |
| 11 | H | X | H | L | H | H | H | H | H | L | L | H | H | L | |
| 12 | H | X | H | H | L | L | H | H | L | H | H | H | L | L | |
| 13 | H | X | H | H | L | H | H | L | H | H | L | H | L | L | |
| 14 | H | X | H | H | H | L | H | H | H | H | L | L | L | L | |
| 15 | H | X | H | H | H | H | H | H | H | H | H | H | H | H | |
| BI | X | X | X | X | X | X | L | H | H | H | H | H | H | H | (3) |
| RBI | H | L | L | L | L | L | L | H | H | H | H | H | H | H | (4) |
| LT | L | X | X | X | X | X | H | L | L | L | L | L | L | L | (5) |

### 48, LS48

| Decimal or Function | Inputs | | | | | | BI/RBO(1) | Outputs | | | | | | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LT | RBI | D | C | B | A | | a | b | c | d | e | f | g | |
| 0 | H | H | L | L | L | L | H | H | H | H | H | H | H | L | (2) |
| 1 | H | X | L | L | L | H | H | L | H | H | L | L | L | L | |
| 2 | H | X | L | L | H | L | H | H | H | L | H | H | L | H | |
| 3 | H | X | L | L | H | H | H | H | H | H | H | L | L | H | |
| 4 | H | X | L | H | L | L | H | L | H | H | L | L | H | H | |
| 5 | H | X | L | H | L | H | H | H | L | H | H | L | H | H | |
| 6 | H | X | L | H | H | L | H | L | L | H | H | H | H | H | |
| 7 | H | X | L | H | H | H | H | H | H | H | L | L | L | L | |
| 8 | H | X | H | L | L | L | H | H | H | H | H | H | H | H | |
| 9 | H | X | H | L | L | H | H | H | H | H | L | L | H | H | |
| 10 | H | X | H | L | H | L | H | L | L | L | H | H | L | H | |
| 11 | H | X | H | L | H | H | H | L | L | H | H | L | L | H | |
| 12 | H | X | H | H | L | L | H | L | H | L | L | L | H | H | |
| 13 | H | X | H | H | L | H | H | H | L | L | H | L | H | H | |
| 14 | H | X | H | H | H | L | H | L | L | L | H | H | H | H | |
| 15 | H | X | H | H | H | H | H | L | L | L | L | L | L | L | |
| BI | X | X | X | X | X | X | L | L | L | L | L | L | L | L | (3) |
| RBI | H | L | L | L | L | L | L | L | L | L | L | L | L | L | (4) |
| LT | L | X | X | X | X | X | H | H | H | H | H | H | H | H | (5) |

**Note 1:** BI/RBO is a wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

**Note 2:** The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

**Note 3:** When a low logic level is applied directly to the blanking input (BI), all segment outputs are H (46, 47); L (48) regardless of the level of any other input.

**Note 4:** When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go H and the ripple-blanking output (RBO) goes to a low level (response condition).

**Note 5:** When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are L.

H = High level, L = Low level, X = Don't Care

## Truth Tables (Continued)

**LS49**

| Decimal or Function | Inputs | | | | | Outputs | | | | | | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D | C | B | A | BI | a | b | c | d | e | f | g | |
| 0 | L | L | L | L | H | H | H | H | H | H | H | L | (1) |
| 1 | L | L | L | H | H | L | H | H | L | L | L | L | |
| 2 | L | L | H | L | H | H | H | L | H | H | L | H | |
| 3 | L | L | H | H | H | H | H | H | H | L | L | H | |
| 4 | L | H | L | L | H | L | H | H | L | L | H | H | |
| 5 | L | H | L | H | H | H | L | H | H | L | H | H | |
| 6 | L | H | H | L | H | L | L | H | H | H | H | H | |
| 7 | L | H | H | H | H | H | H | H | L | L | L | L | |
| 8 | H | L | L | L | H | H | H | H | H | H | H | H | |
| 9 | H | L | L | H | H | H | H | H | L | L | H | H | |
| 10 | H | L | H | L | H | L | L | L | H | H | L | H | |
| 11 | H | L | H | H | H | L | L | H | H | L | L | H | |
| 12 | H | H | L | L | H | L | H | L | L | L | H | H | |
| 13 | H | H | L | H | H | H | L | L | H | L | H | H | |
| 14 | H | H | H | L | H | L | L | L | H | H | H | H | |
| 15 | H | H | H | H | H | L | L | L | L | L | L | L | |
| BI | X | X | X | X | L | L | L | L | L | L | L | L | (2) |

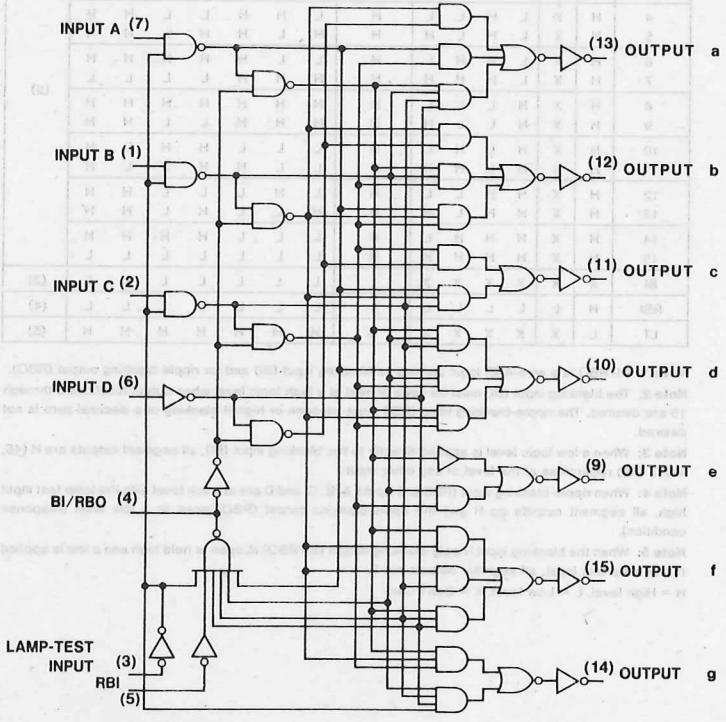
**Note 1:** The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired.

**Note 2:** When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.

H = High Level, L = Low Level, X = Don't Care

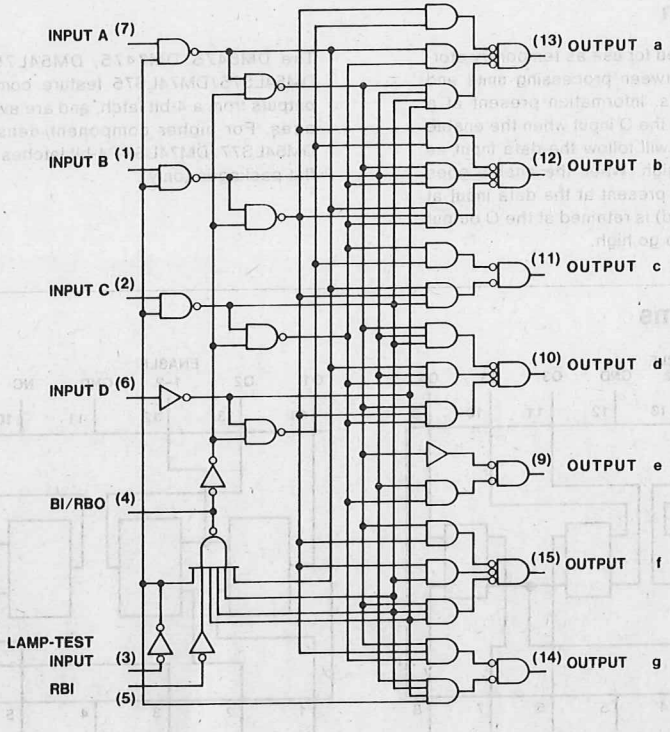
## Logic Diagrams

**46A, LS47**

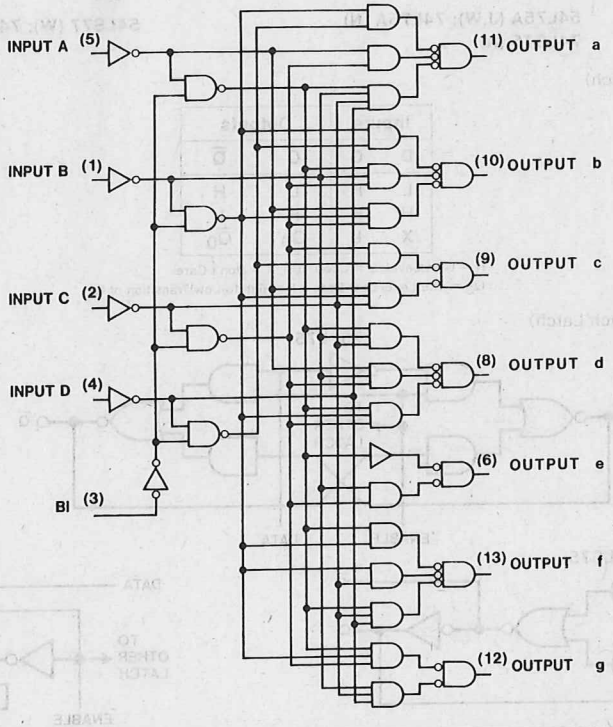


## Logic Diagrams (Continued)

48, LS48




LS49



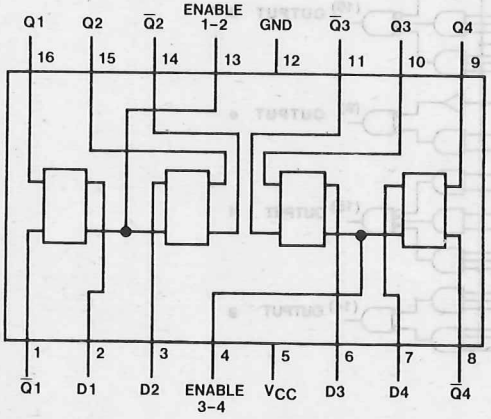
## Quad Latches

## General Description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q input when the enable (G) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

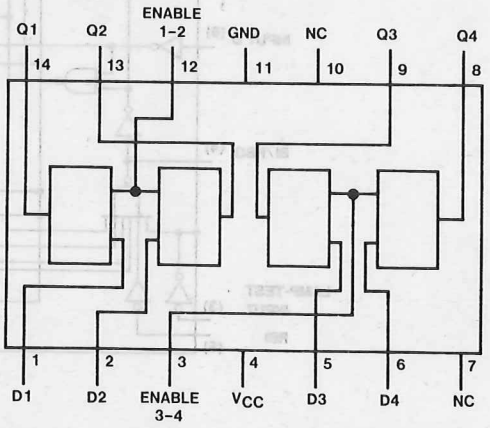
The DM5475/DM7475, DM54L75A/DM74L75A, and DM54LS75/DM74LS75 feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and are available in 16-pin packages. For higher component density applications, the DM54LS77/DM74LS77 4-bit latches are available in 14-pin flat packages (only).

## Connection Diagrams




5475 (J,W); 7475 (N)
54LS75 (J,W)

54L75A (J,W); 74L75A (N)
74LS75 (N)



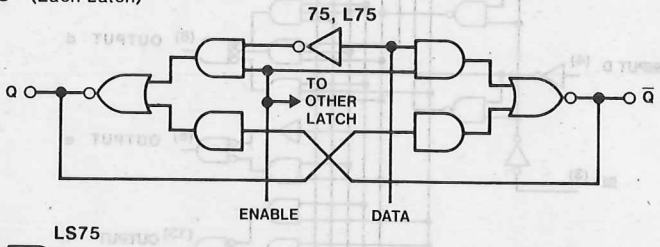

54LS77 (W); 74LS77 (W)

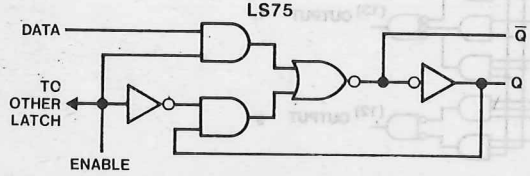
## Truth Table (Each Latch)

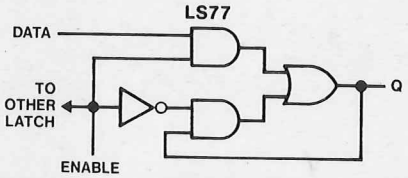
| Inputs | | Outputs | |
|---|---|---|---|
| D | G | Q | $\overline{Q}$ |
| L | H | L | H |
| H | H | H | L |
| X | L | $Q_0$ | $\overline{Q}_0$ |

H = High Level, L = Low Level, X = Don't Care
$Q_0$ = The Level of Q Before the High-to-Low Transition of G

## Logic Diagrams (Each Latch)



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 75 Min | DM54/74 75 Typ (1) | DM54/74 75 Max | DM54/74 L75A Min | DM54/74 L75A Typ (1) | DM54/74 L75A Max | DM54/74 LS75, LS77 Min | DM54/74 LS75, LS77 Typ (1) | DM54/74 LS75, LS77 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.7 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.7 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | N/A | | | | V |
| | | | $I_I$ = −18 mA | | | | | | | N/A | | | −1.5 | |
| $I_{OH}$ | High Level Output Current | | | | | | −400 | | | −200 | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.4 | 3.4 | | 2.4 | 3.4 | | 2.5 | 3.5 | | V |
| | | | | DM74 | 2.4 | 3.4 | | 2.4 | 3.4 | | 2.7 | 3.5 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | | | 2 | | | 4 | mA |
| | | | | DM74 | | | 16 | | | 3.6 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = 4 mA | DM74 | | | | | | | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | | 0.3 | | 0.25 | 0.4 | |
| | | | | DM74 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.35 | 0.5 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | D Input | | | 1 | | | 0.2 | | | | mA |
| | | | | G Input | | | 1 | | | 0.4 | | | | |
| | | | $V_I$ = 7 V | D Input | | | | | | | | | 0.1 | |
| | | | | G Input | | | | | | | | | 0.4 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | D Input | | | 80 | | | 20 | | | | μA |
| | | | | G Input | | | 80 | | | 40 | | | | |
| | | | $V_I$ = 2.7 V | D Input | | | | | | | | | 20 | |
| | | | | G Input | | | | | | | | | 80 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.3 V 54L/74L, $V_I$ = 0.4 V Others | D Input | | | −3.2 | | | −0.36 | | | −0.4 | mA |
| | | | | G Input | | | −3.2 | | | −0.72 | | | −1.6 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −20 | | −55 | −3 | −9 | −15 | −20 | | −100 | mA |
| | | | | DM74 | −18 | | −55 | −3 | −9 | −15 | −20 | | −100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | DM54 | LS75 | | | | | | | | 6.3 | 12 | mA |
| | | | | Others | | 32 | 46 | | 3.5 | 5.0 | | 6.9 | 13 | |
| | | | DM74 | LS75 | | | | | | | | 6.3 | 12 | |
| | | | | Others | | 32 | 50 | | 3.5 | 50 | | 6.9 | 13 | |

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | DM54/74 75 Conditions | DM54/74 75 Min | DM54/74 75 Typ | DM54/74 75 Max | DM54/74 L75A Conditions | DM54/74 L75A Min | DM54/74 L75A Typ | DM54/74 L75A Max | Conditions | DM54/74 LS75 Min | DM54/74 LS75 Typ | DM54/74 LS75 Max | DM54/74 LS77 Min | DM54/74 LS77 Typ | DM54/74 LS77 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | D | Q | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 16 | 30 | $C_L$ = 50 pF, $R_L$ = 4 kΩ | | 55 | 100 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 15 | 27 | | 15 | 27 | ns |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 19 | 30 | | 19 | 30 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 14 | 25 | | | 50 | 100 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 9 | 17 | | 9 | 17 | |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 14 | 25 | | 14 | 25 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | D | $\overline{Q}$ | | | 24 | 40 | | | 75 | 120 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 10 | 20 | | | N/A | ns |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 13 | 25 | | | N/A | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 7 | 15 | | | 32 | 80 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 8 | 15 | | | N/A | |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 10 | 20 | | | N/A | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | G | Q | | | 16 | 30 | | | 50 | 100 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 15 | 27 | | 15 | 27 | ns |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 19 | 30 | | 19 | 30 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 7 | 15 | | | 32 | 80 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 14 | 25 | | 17 | 25 | |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 20 | 30 | | 20 | 30 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | G | $\overline{Q}$ | | | 16 | 30 | | | 48 | 100 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 16 | 30 | | | N/A | ns |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 18 | 30 | | | N/A | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 7 | 15 | | | 38 | 80 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 7 | 15 | | | N/A | |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 10 | 20 | | | N/A | |
| $t_W$ | Width of Enabling Pulse | | | | 20 | | | | 100 | | | | 20 | | | 20 | | | ns |
| $t_{SETUP}$ | Setup Time | | | | 20 | | | | 100 | | | | 20 | | | 20 | | | ns |
| $t_{HOLD}$ | Hold Time | | | | 5 | | | | 25 | | | | 0 | | | 0 | | | ns |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for the DM54LS/74LS duration of short circuit should not exceed one second.

**Note 3:** $I_{CC}$ is tested with all inputs grounded and all outputs open.

# 4-Bit Binary Adders with Fast Carry

## General Description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

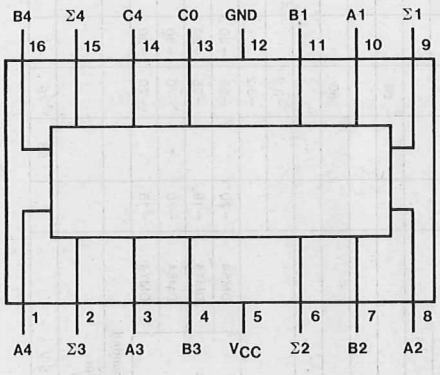
The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

## Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry

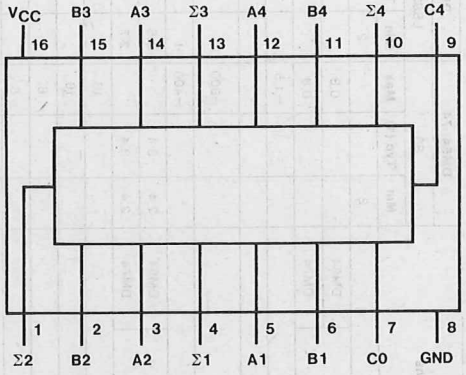
| Type | Typical Add Times: Two 8-Bit Words | Typical Add Times: Two 16-Bit Words | Typical Power Dissipation Per 4-Bit Adder |
|---|---|---|---|
| 83 | 23 ns | 43 ns | 290 mW |
| LS83A | 25 ns | 45 ns | 95 mW |
| LS283 | 25 ns | 45 ns | 95 mW |
| S283 | 15 ns | 30 ns | 510 mW |

## Connection Diagrams and Truth Table




5483 (J,W)
54LS83A (J,W)

7483 (N)
74LS83A (N)




54LS283 (J,W)
54S283 (J,W)

74LS283 (N)
74S283 (N)

| Input | | | | Output | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | When C0 = L | | | When C0 = H | | |
| | | | | | | When C2 = L | | | When C2 = H |
| A1 / A3 | B1 / B3 | A2 / A4 | B2 / B4 | Σ1 / Σ3 | Σ2 / Σ4 | C2 / C4 | Σ1 / Σ3 | Σ2 / Σ4 | C2 / C4 |
| L | L | L | L | L | L | L | H | L | L |
| H | L | L | L | H | L | L | L | H | L |
| L | H | L | L | H | L | L | L | H | L |
| H | H | L | L | L | H | L | H | H | L |
| L | L | H | L | L | H | L | H | H | L |
| H | L | H | L | H | H | L | L | L | H |
| L | H | H | L | H | H | L | L | L | H |
| H | H | H | L | L | L | H | H | L | H |
| L | L | L | H | L | H | L | H | H | L |
| H | L | L | H | H | H | L | L | L | H |
| L | H | L | H | H | H | L | L | L | H |
| H | H | L | H | L | L | H | H | L | H |
| L | L | H | H | L | L | H | H | L | H |
| H | L | H | H | H | L | H | L | H | H |
| L | H | H | H | H | L | H | L | H | H |
| H | H | H | H | L | H | H | H | H | H |

H = High Level, L = Low Level

**Note**

Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM54/74 83 | | | DM54/74 LS83A, LS283 | | | DM54/74 S283 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | DM54 | | | 0.8 | | | 0.8 | | | 0.8 | V |
| | | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | | | | | V |
| | | | | $I_I$ = −18 mA | | | | | | | −1.5 | | | −1.2 | |
| $I_{OH}$ | High Level Output Current | Any Output Except C4 | | | | | | −800 | | | −400 | | | −1000 | µA |
| | | Output C4 | | | | | | −400 | | | −400 | | | −500 | |
| $V_{OH}$ | High Level Output Voltge | | $V_{CC}$ = Min, $V_{IH}$ = 2 V $V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.4 | 3.4 | | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | | DM74 | 2.4 | 3.4 | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | Any Output Except C4 | | DM54 | | | | 16 | | | 4 | | | 20 | mA |
| | | | | DM74 | | | | 16 | | | 8 | | | 20 | |
| | | Output C4 | | DM54 | | | | 8 | | | 4 | | | 10 | |
| | | | | DM74 | | | | 8 | | | 8 | | | 10 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min $V_{IH}$ = 2 V $V_{IL}$ = Max | $I_{OL}$ = 4 mA | | | | | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | $I_{OL}$ = 8 mA | DM74 | | | | | 0.35 | 0.5 | | | 0.5 | |
| | | | | $I_{OL}$ = Max | | | 0.2 | 0.4 | | | | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | Any A or B | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | | | | 1 | mA |
| | | | | $V_I$ = 7 V | | | | | | | 0.2 | | | | |
| | | C0 | | $V_I$ = 5.5 V | | | | 1 | | | | | | 1 | |
| | | | | $V_I$ = 7 V | | | | | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | Any A or B | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 80 | | | | | | | µA |
| | | | | $V_I$ = 2.7 V | | | | | | | 40 | | | 50 | |
| | | C0 | | $V_I$ = 2.4 V | | | | 80 | | | | | | | |
| | | | | $V_I$ = 2.7 V | | | | | | | 20 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | Any A or B | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | | −3.2 | | | −0.8 | | | −2 | mA |
| | | C0 | | | | | | −3.2 | | | −0.4 | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | Any Output Except C4 | $V_{CC}$ = Max (2) | | DM54 | −20 | | −55 | −20 | | −100 | −40 | | −100 | mA |
| | | | | | DM74 | −18 | | −55 | −20 | | −100 | −40 | | −100 | |
| | | Output C4 | | | DM54 | −20 | | −70 | −20 | | −100 | −40 | | −100 | |
| | | | | | DM74 | −18 | | −70 | −20 | | −100 | −40 | | −100 | |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max Outputs Open | Any Inputs Grounded | | | | | | 22 | 39 | | | | mA |
| | | | | All B Low, Other Inputs at 4.5 V | | | | | | 19 | 34 | | 80 | 120 | |
| | | | | All Inputs at 4.5 V | | | 58 | 79 | | 19 | 34 | | 95 | 160 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Only one output should be shorted at a time, or for 54LS/74LS or 54S/74S duration of short circuit should not exceed one second.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

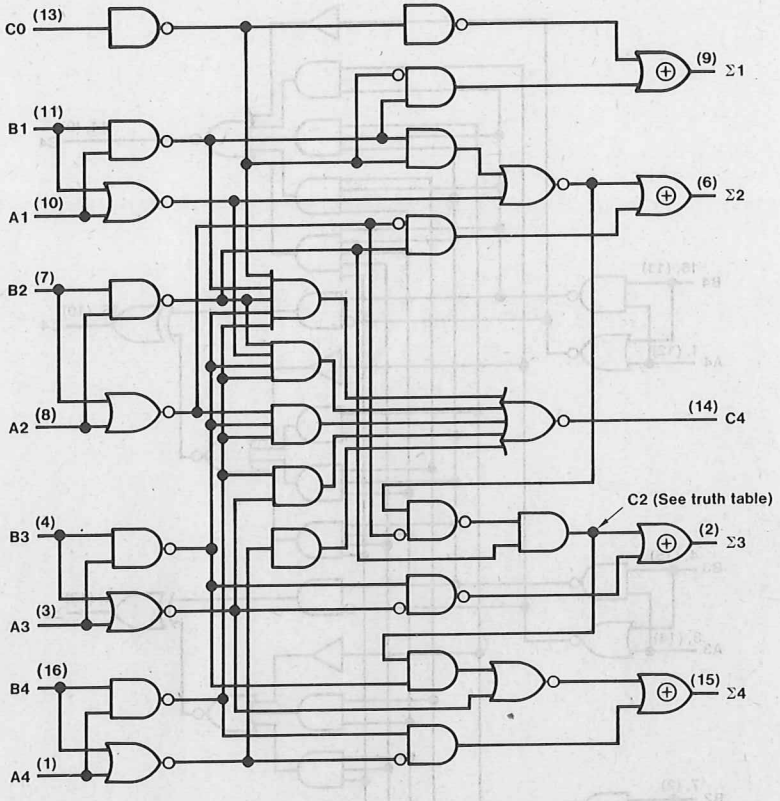
| Parameter | | From (Input) | To (Output) | DM54/74 83 | | | | DM54/74 LS83A, LS283 | | | | DM54/74 LS83A, LS283 | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | C0 | $\Sigma_1$ or $\Sigma_2$ | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 22 | 32 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 16 | 24 | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 19 | 28 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 20 | 32 | | | 15 | 24 | | | 21 | 30 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | C0 | $\Sigma_3$ | | | 28 | 47 | | | 16 | 24 | | | 19 | 28 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 22 | 38 | | | 15 | 24 | | | 21 | 30 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | C0 | $\Sigma_4$ | | | 28 | 47 | | | 16 | 24 | | | 19 | 28 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 28 | 47 | | | 15 | 24 | | | 21 | 30 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $A_i$ or $B_i$ | $\Sigma_i$ | | | | 38 | | | 15 | 24 | | | 19 | 28 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 33 | | | 15 | 24 | | | 21 | 30 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | C0 | $C_4$ | $C_L$ = 15 pF, $R_L$ = 780 Ω | | 12 | 19 | | | 11 | 17 | | | 15 | 24 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 12 | 19 | | | 11 | 17 | | | 17 | 25 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $A_i$ or $B_i$ | $C_4$ | | | 12 | 19 | | | 11 | 17 | | | 15 | 24 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 12 | 19 | | | 12 | 17 | | | 18 | 26 | ns |

## Switching Characteristics (Continued)

| Parameter | | From (Input) | To (Output) | DM54/74 | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | S283 | | | | S283 | | | | |
| | | | | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | C0 | $\Sigma_1$ or $\Sigma_2$ | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 11 | 18 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 13 | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 12 | 18 | | | 14 | 20 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | C0 | $\Sigma_3$ | | | 11 | 18 | | | 13 | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 12 | 18 | | | 14 | 20 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | C0 | $\Sigma_4$ | | | 11 | 18 | | | 13 | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 12 | 18 | | | 14 | 20 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $A_i$ or $B_i$ | $\Sigma_i$ | | | 12 | 18 | | | 14 | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 11.5 | 18 | | | 14 | 20 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | C0 | $C_4$ | $C_L$ = 15 pF, $R_L$ = 560 Ω | | 6 | 11 | $C_L$ = 50 pF, $R_L$ = 560 Ω | | 10 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 7.5 | 11 | | | 12 | 15 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $A_i$ or $B_i$ | $C_4$ | | | 7.5 | 12 | | | 12 | 16 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 8.5 | 12 | | | 13 | 16 | ns |

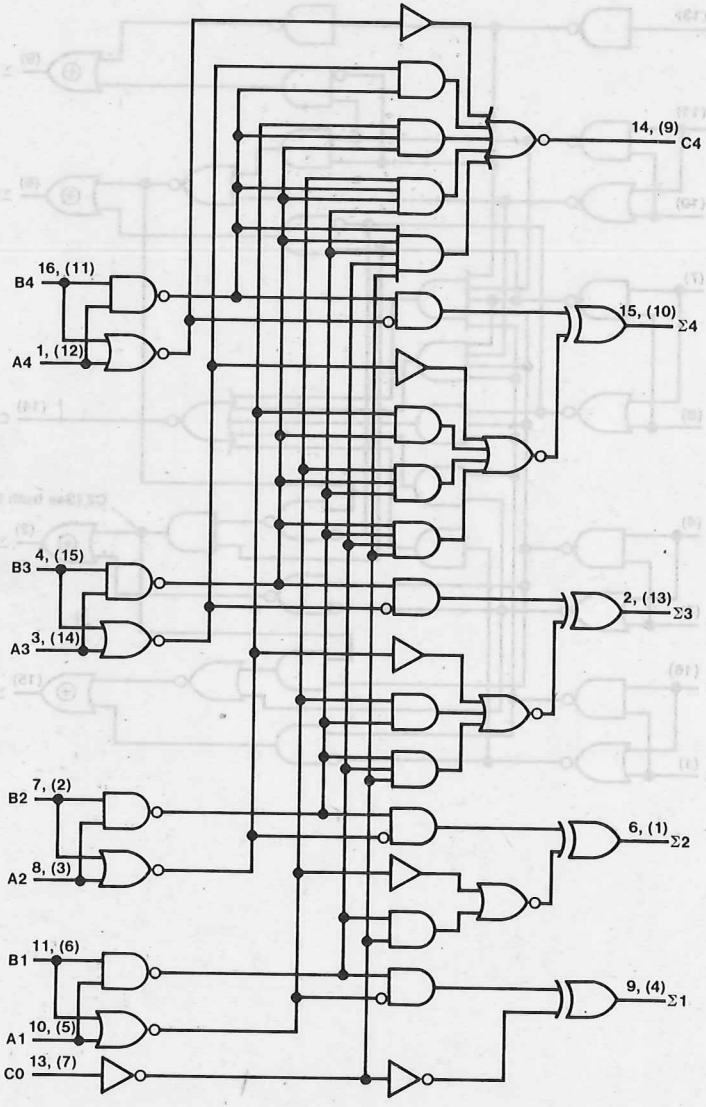
## Logic Diagrams

83



## Logic Diagrams (Continued)

LS83A, LS283, S283




**Note**
Pin numbers shown in parenthesis are for LS283, S283

# 4-Bit Magnitude Comparators

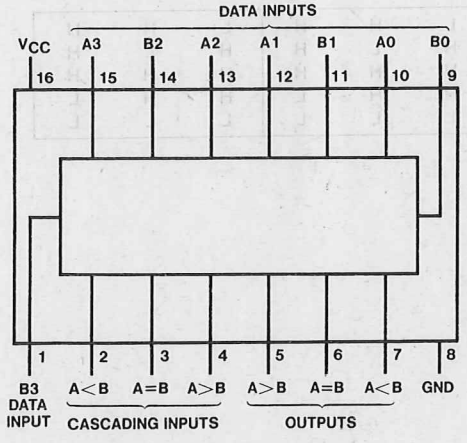
## General Description

These four-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two, 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input and in addition for the L85, low-level voltages applied to the A > B and A < B inputs. The cascading paths of the 85, and LS85 are implemented with only a two-gate-level delay to reduce overall comparison times for long words.

## Features

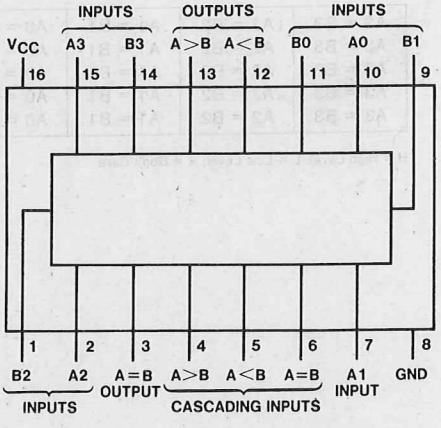
| Type | Typical Power Dissipation | Typical Delay (4-Bit Words) |
|---|---|---|
| 85 | 275 mW | 23 ns |
| L85 | 20 mW | 55 ns |
| LS85 | 52 mW | 24 ns |

## Connection Diagrams




5485 (J,W)
54LS85 (J,W)

7485 (N)
74LS85 (N)




54L85 (J,W); 74L85 (N)

## Truth Tables

| Comparing Inputs | | | | Cascading Inputs | | | Outputs | | |
|---|---|---|---|---|---|---|---|---|---|
| A3, B3 | A2, B2 | A1, B1 | A0, B0 | A > B | A < B | A = B | A > B | A < B | A = B |
| A3 > B3 | X | X | X | X | X | X | H | L | L |
| A3 < B3 | X | X | X | X | X | X | L | H | L |
| A3 = B3 | A2 > B2 | X | X | X | X | X | H | L | L |
| A3 = B3 | A2 < B2 | X | X | X | X | X | L | H | L |
| A3 = B3 | A2 = B2 | A1 > B1 | X | X | X | X | H | L | L |
| A3 = B3 | A2 = B2 | A1 < B1 | X | X | X | X | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 > B0 | X | X | X | H | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 < B0 | X | X | X | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | H | L | L | H | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | H | L | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | L | H | L | L | H |

**85, LS85**

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | X | X | H | L | L | H |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | H | H | L | L | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | L | L | H | H | L |

**L85**

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | H | H | L | H | H |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | H | L | H | H | L | H |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | H | H | H | H | H | H |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | H | H | L | H | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | L | L | L | L | L |

H = High Level, L = Low Level, X = Don't Care

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM54/74 85 | | | DM54/74 L85 | | | DM54/74 LS85 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | DM54 | | | 0.8 | | | 0.7 | | | 0.8 | V |
| | | | | | DM74 | | | 0.8 | | | 0.7 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | N/A | | | | V |
| | | | | $I_I$ = −18 mA | | | | | | | N/A | | | −1.5 | |
| $I_{OH}$ | High Level Output Current | | | | | | | −800 | | | −200 | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.4 | | | 2.4 | | | 2.5 | 3.4 | | V |
| | | | | | DM74 | 2.4 | | | 2.4 | | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 16 | | | 2 | | | 4 | mA |
| | | | | | DM74 | | | 16 | | | 3.6 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | | 0.4 | | 0.15 | 0.3 | | 0.25 | 0.4 | V |
| | | | | | DM74 | | | 0.4 | | 0.2 | 0.4 | | 0.35 | 0.5 | |
| | | | | $I_{OL}$ = 4 mA | DM74 | | | | | | | | 0.25 | 0.4 | |
| $I_I$ | Input Current at Maximum Input Voltage | A < B, A > B, or A = B (5) | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1.0 | | | 0.1 | | | | mA |
| | | | | $V_I$ = 7 V | | | | | | | | | | 0.1 | |
| | | All Other Inputs | | $V_I$ = 5.5 V | | | | 1.0 | | | 0.3 | | | | |
| | | | | $V_I$ = 7 V | | | | | | | | | | 0.3 | |
| $I_{IH}$ | High Level Input Current | A < B, A > B, or A = B (5) | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | 10 | | | | μA |
| | | | | $V_I$ = 2.7 V | | | | | | | | | | 20 | |
| | | All Other Inputs | | $V_I$ = 2.4 V | | | | 120 | | | 30 | | | | |
| | | | | $V_I$ = 2.7 V | | | | | | | | | | 60 | |
| $I_{IL}$ | Low Level Input Current | A < B, A > B, or A = B (5) | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | | | −0.18 | | | | μA |
| | | | | $V_I$ = 0.4 V | | | | −1.6 | | | | | | −0.4 | |
| | | All Other Inputs | | $V_I$ = 0.3 V | | | | | | | −0.54 | | | | |
| | | | | $V_I$ = 0.4 V | | | | −4.8 | | | | | | −1.2 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | DM54 | −20 | | −55 | −3 | | −15 | −20 | | −100 | mA |
| | | | | | DM74 | −18 | | −55 | −3 | | −15 | −20 | | −100 | |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max | Condition A | (3) | | | | | | 6.6 | | | | mA |
| | | | | Condition B | | | | | | | 7.0 | | | | |
| | | | | | (4) | | 55 | 88 | | | | | 10.4 | 20 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.
**Note 3:** With all outputs open, $I_{CC}$ is measured for Condition A with all inputs at 4.5 V, and for Condition B with all inputs grounded.
**Note 4:** $I_{CC}$ is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.
**Note 5:** The condition A = B applies to L85 values only. For DM5485/DM7485 and LS85 use the values for "All Other Inputs."

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

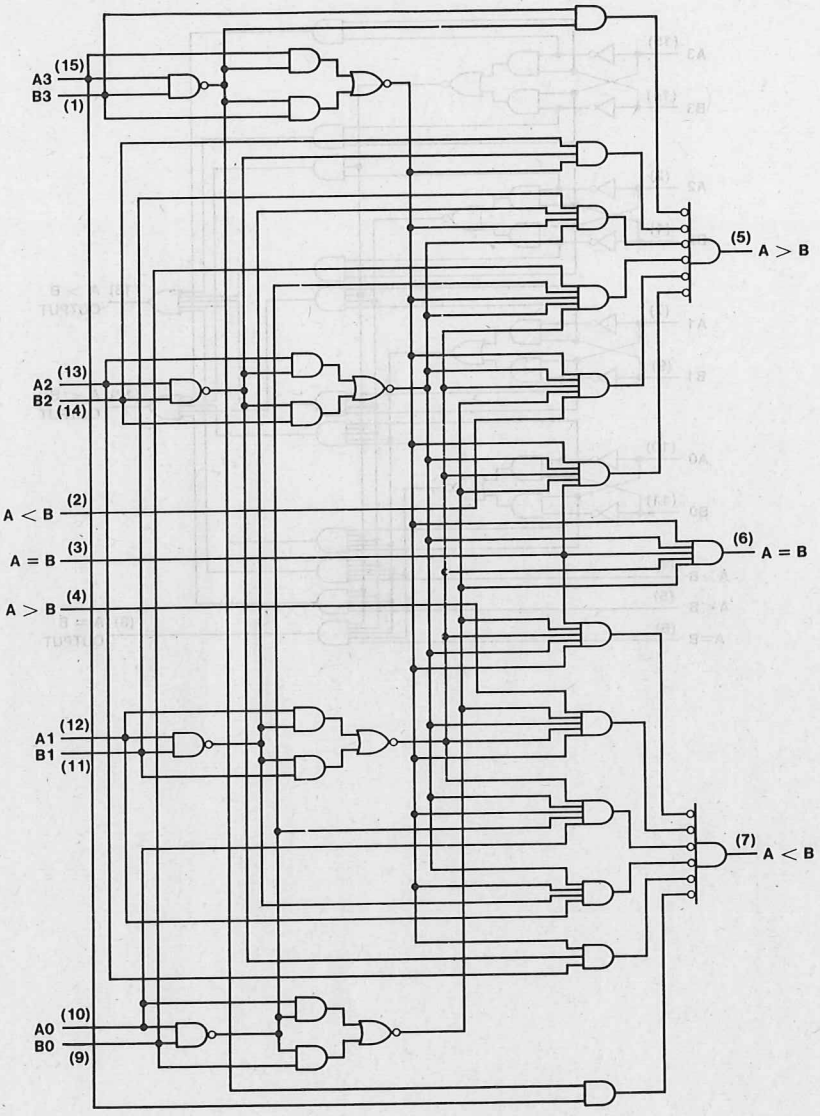
| Parameter | | From Input | To Output | Number of Gate Levels | DM54/74 85 | | | | DM54/74 L85 | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any A or B Data Input | A < B, A > B | 1 | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 7 | | $C_L$ = 50 pF, $R_L$ = 4 kΩ | | 70 | 115 | ns |
| | | | | 2 | | | 12 | | | | 70 | 115 | |
| | | | | 3 | | | 17 | 26 | | | 70 | 115 | |
| | | | A = B | 4 | | | 23 | 35 | | | 70 | 115 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Any A or B Data Input | A < B, A > B | 1 | | | 11 | | | | 55 | 90 | ns |
| | | | | 2 | | | 15 | | | | 55 | 90 | |
| | | | | 3 | | | 20 | 30 | | | 55 | 90 | |
| | | | A = B | 4 | | | 20 | 30 | | | 55 | 90 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A < B or A = B | A > B | 1 | | | 7 | 11 | | | 55 | 100 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | A < B or A = B | A > B | 1 | | | 11 | 17 | | | 40 | 65 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A = B | A = B | 2 | | | 13 | 20 | | | 55 | 100 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | A = B | A = B | 2 | | | 11 | 17 | | | 40 | 65 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A > B or A = B | A < B | 1 | | | 7 | 11 | | | 55 | 100 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | A > B or A = B | A < B | 1 | | | 11 | 17 | | | 40 | 65 | ns |

## Switching Characteristics (Continued)

| Parameter | | From Input | To Output | Number of Gate Levels | DM54/74 LS85 | | | | LS85 | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any A or B Data Input | A < B, A > B | 1 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 14 | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 17 | | ns |
| | | | | 2 | | | 19 | | | | 22 | | |
| | | | | 3 | | | 24 | 36 | | | 27 | 42 | |
| | | | A = B | 4 | | | 23 | 40 | | | 26 | 40 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Any A or B Data Input | A < B, A > B | 1 | | | 11 | | | | 17 | | ns |
| | | | | 2 | | | 15 | | | | 21 | | |
| | | | | 3 | | | 20 | 30 | | | 26 | 40 | |
| | | | A = B | 4 | | | 20 | 30 | | | 26 | 40 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A < B or A = B | A > B | 1 | | | 14 | 22 | | | 17 | 26 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | A < B or A = B | A > B | 1 | | | 11 | 17 | | | 17 | 26 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A = B | A = B | 2 | | | 13 | 20 | | | 16 | 25 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | A = B | A = B | 2 | | | 11 | 17 | | | 17 | 26 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A > B or A = B | A < B | 1 | | | 14 | 22 | | | 17 | 26 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | A > B or A = B | A < B | 1 | | | 11 | 17 | | | 17 | 26 | ns |

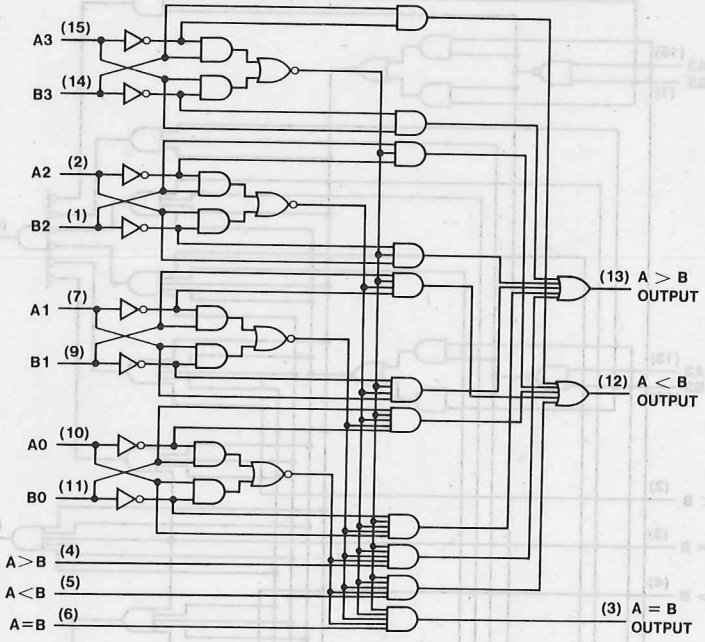
## Logic Diagrams

85, LS85



## Logic Diagrams (Continued)

**L85**



# 64-Bit Read/Write Memories

## General Description

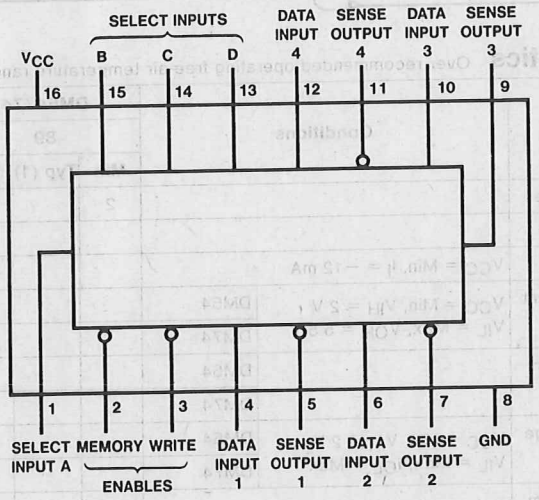
The DM5489B/DM7489B, DM54L89A/DM74L89A are fully decoded 64-bit RAMs organized as 16, 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the logical "1" state.

The "A" suffix on the low power versions is used to denote that full "tenth-power" technology has been employed in building this RAM.

## Features

- For application as a "scratch pad" memory with nondestructive read-out
- Fully decoded memory organized as 16 words of four bits each
- Fast access time — DM54/74—35 ns typical; DM54L/74L—110 ns
- Diode-clamped, buffered inputs
- Open-collector outputs provide wire-OR capability
- Typical power dissipation — DM54/74—400 mW; DM54L/74L—75 mW
- Pin compatible with 3101, MM5501

## Connection Diagram



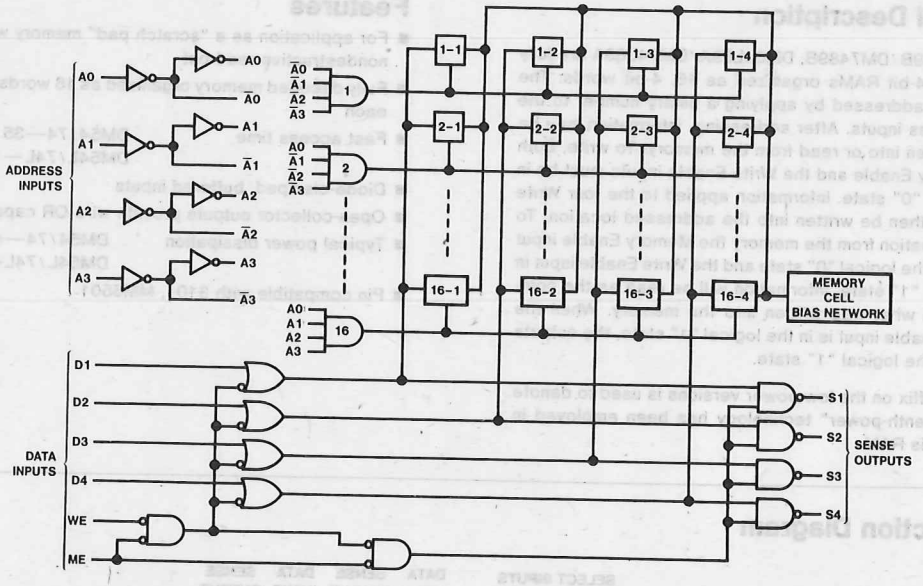

5489 (J)
54L89A (J,W)

7489 (N)
74L89A (N)

## Truth Table

| Memory Enable | Write Enable | Operation | Outputs |
|---|---|---|---|
| 0 | 0 | Write | Logical "1" State |
| 0 | 1 | Read | Complement of Data Stored in Memory |
| 1 | X | Hold | Logical "1" State |

## Logic Diagram




## Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM54/74 89 | | | DM54/74 L89A | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | | | 0.7 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $I_{CEX}$ | High Level Output Current | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $V_{OH}$ = 5.5 V | DM54 | | | 100 | | | 50 | μA |
| | | | DM74 | | | 20 | | | 50 | |
| $I_{OL}$ | Low Level Output Current | | DM54 | | | 12 | | | 2.0 | mA |
| | | | DM74 | | | 12 | | | 3.6 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OL}$ = Max | DM54 | | | 0.4 | | | 0.3 | V |
| | | | DM74 | | | 0.4 | | | 0.4 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | | | 0.1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | | | 10 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | | −0.18 | mA |
| | | | $V_I$ = 0.4 V | | | −1.6 | | | | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (2) | | | 80 | 120 | | 15 | 19 | mA |
| $C_O$ | Off-State Output Capacitance | $V_{CC}$ = 5 V, $V_O$ = 2.0 V, f = 1 MHz | | | 6 | | | N/A | | pF |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** $I_{CC}$ is measured with all inputs grounded.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Condition | DM54/74 89 | | | Conditions | DM54/74L L89A | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output From Memory Enable | $C_L$ = 30 pF, $R_{L1}$ = 300 Ω, $R_{L2}$ = 600 Ω | | 23 | 35 | $C_L$ = 50 pF, $R_L$ = 4 kΩ | | 64 | 90 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Memory Enable | | | 23 | 35 | | | 33 | 60 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output From Select | | | 34 | 50 | | | 90 | 150 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Select | | | 35 | 50 | | | 78 | 150 | ns |
| $t_{SR}$ | Sense Recovery Time After Writing | | | 35 | 50 | | | 110 | 165 | ns |
| $t_W$ | Width of Write-Enable Pulse | | 40 | | | | 50 | | | ns |
| $t_{SETUP}$ | Setup Time, Data Input With Respect to Write Enable | | 0 | | | | 0 | | | ns |
| $t_{SETUP}$ | Select Input Setup Time With Respect to Write Enable | | 0 | | | | 0 | | | ns |
| $t_{HOLD}$ | Hold Time, Data Input With Respect to Write Enable | | 0 | | | | 0 | | | ns |
| $t_{HOLD}$ | Select Input Hold Time After Writing | | 5 | | | | 0 | | | ns |

# Decade, Divide by 12, and Binary Counters

## General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 90A, L90, and LS90, divide-by-six for the 92A and LS92, and divide-by-eight for the 93A, L93, and LS93.

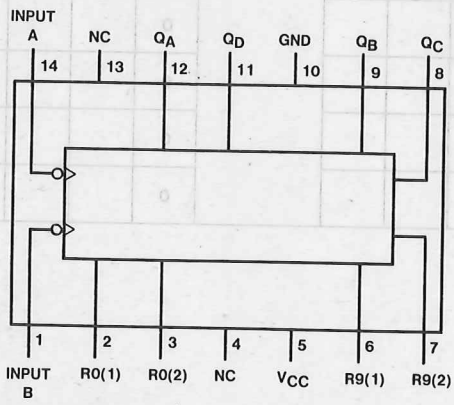
All of these counters have a gated zero reset and the 90A, L90, and LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary), the B input is connected to the $Q_A$ output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by ten count can be obtained from the 90A, L90, or LS90 counters by connecting the $Q_D$ output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output $Q_A$.

## Features

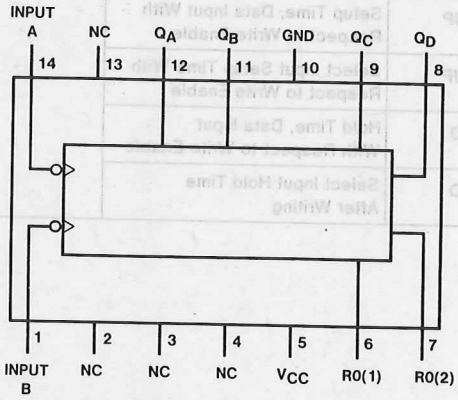
| Type | Typical Power Dissipation | Count Frequency |
|---|---|---|
| 90A | 145 mW | 42 MHz |
| L90 | 20 mW | 11 MHz |
| LS90 | 45 mW | 42 MHz |
| 92A, 93A | 130 mW | 42 MHz |
| LS92, LS93 | 45 mW | 42 MHz |
| L93 | 16 mW | 15 MHz |

## Connection Diagrams



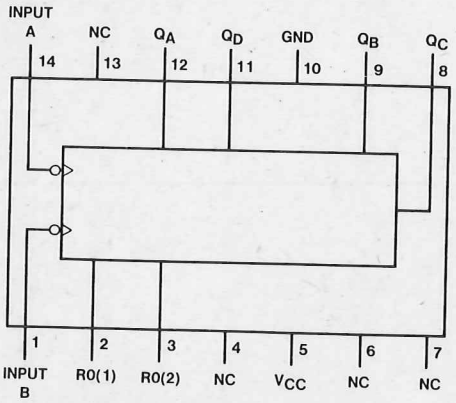

**5490A (J,W)**
**54L90 (J,W)**
**54LS90 (J,W)**

**7490A (N)**
**74L90 (N)**
**74LS90 (N)**



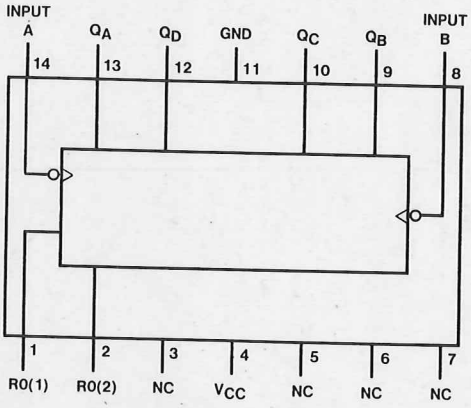

**5492A (J,W)**
**54LS92 (J,W)**

**7492A (N)**
**74LS92 (N)**




**5493A (J,W)**
**54LS93 (J,W)**

**7493A (N)**
**74LS93 (N)**




**54L93 (J,W); 74L93 (N)**

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM54/74 90A, 92A, 93A | | | DM54/74 L90, L93 | | | DM54/74 LS90, LS92, LS93 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | DM54 | | | 0.8 | | | 0.7 | | | 0.8 | V |
| | | | | | DM74 | | | 0.8 | | | 0.7 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | N/A | | | | V |
| | | | | $I_I$ = −18 mA | | | | | | | N/A | | | −1.5 | |
| $I_{OH}$ | High Level Output Current | | | | | | | −800 | | | −200 | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V | | DM54 | 2.4 | 3.4 | | 2.4 | | | 2.5 | 3.4 | | V |
| | | | $V_{IL}$ = Max, $I_{OH}$ = Max | | DM74 | 2.4 | 3.4 | | 2.4 | | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 16 | | | 2 | | | 4 | mA |
| | | | | | DM74 | | | 16 | | | 3.6 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = Max (3) | DM54 | | 0.2 | 0.4 | | 0.15 | 0.3 | | 0.25 | 0.4 | V |
| | | | | | DM74 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.35 | 0.5 | |
| | | | | $I_{OL}$ = 4 mA | DM74 | | | | | | | | 0.25 | 0.4 | |
| $I_I$ | Input Current at Maximum Input Voltage | Any Reset | $V_{CC}$ = Min | $V_I$ = 5.5 V | | | | 1 | | | 0.1 | | | | mA |
| | | | | $V_I$ = 7 V | | | | | | | | | | 0.1 | |
| | | A Input | | $V_I$ = 5.5 V | | | | 1 | | | 0.2 | | | 0.2 | |
| | | B Input | | $V_I$ = 5.5 V | L90, LS93 | | | | | | 0.4 | | | 0.2 | |
| | | | | | Others | | | 1 | | | 0.2 | | | 0.4 | |
| $I_{IH}$ | High Level Input Current | Any Reset | $V_{CC}$ = Max | $V_I$ = 2.7 V for LS, $V_I$ = 2.4 V for Others | | | | 40 | | | 10 | | | 20 | μA |
| | | A Input | | | | | | 80 | | | 20 | | | 40 | |
| | | B Input | | | 93 | | | 80 | | | 20 | | | 40 | |
| | | | | | Others | | | 120 | | | 40 | | | 80 | |
| $I_{IL}$ | Low Level Input Current | Any Reset | $V_{CC}$ = Max | $V_I$ = 0.3 V for L, $V_I$ = 0.4 V for Others | | | | −1.6 | | | −0.18 | | | −0.4 | mA |
| | | A Input | | | | | | −3.2 | | | −0.36 | | | −2.4 | |
| | | B Input | | | 93 | | | −3.2 | | | −0.36 | | | −1.6 | |
| | | | | | Others | | | −4.8 | | | −0.72 | | | −3.2 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | DM54 | −20 | | −57 | −3 | −9 | −15 | −20 | | −100 | mA |
| | | | | | DM74 | −18 | | −57 | −3 | −9 | −15 | −20 | | −100 | |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (4) | | 90A | | 29 | 42 | | | | | | | mA |
| | | | | | Others | | 26 | 39 | | | 5.5 | | 9 | 15 | |

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | To (Output) | Conditions | DM54/74 90A Min | 90A Typ | 90A Max | 92A Min | 92A Typ | 92A Max | 93A Min | 93A Typ | 93A Max | DM54/74 L90 Min | L90 Typ | L90 Max | L93 Min | L93 Typ | L93 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Count Frequency | | A | $Q_A$ | $C_L$ = 50 pF For L90 and L93 $C_L$ = 15 pF For All Others $R_L$ = 400 Ω For 90A, 92A and 93A $R_L$ = 4 kΩ For L90 and L93 | 32 | 42 | | 32 | 42 | | 32 | 42 | | 6 | 11 | | 6 | 15 | | MHz |
| | | | B | $Q_B$ | | 16 | | | 16 | | | 16 | | | | | | | | | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | A | $Q_A$ | | | 10 | 16 | | 10 | 16 | | 10 | 16 | | | | | | | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 12 | 18 | | 12 | 18 | | 12 | 18 | | | | | | | |
| $t_{PLH}$ | Propagaton Delay Time, Low-to-High Level Output | | A | $Q_D$ | | | 32 | 48 | | 32 | 48 | | 46 | 70 | | 175 | 300 | | 210 | 400 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 34 | 50 | | 34 | 50 | | 46 | 70 | | 190 | 300 | | 230 | 400 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | B | $Q_B$ | | | 10 | 16 | | 10 | 16 | | 10 | 16 | | | | | | | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 14 | 21 | | 14 | 21 | | 14 | 21 | | | | | | | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | B | $Q_C$ | | | 21 | 32 | | 10 | 16 | | 21 | 32 | | | | | | | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 23 | 35 | | 14 | 21 | | 23 | 35 | | | | | | | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | B | $Q_D$ | | | 21 | 32 | | 21 | 32 | | 34 | 51 | | | | | | | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 23 | 35 | | 23 | 35 | | 34 | 51 | | | | | | | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Set-to-0 | Any | | | 26 | 40 | | 26 | 40 | | 26 | 40 | | | | | | | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Set-to-9 | $Q_A$, $Q_D$ | | | 20 | 30 | | | | | | | | | | | | | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $Q_B$, $Q_C$ | | | 26 | 40 | | | | | | | | | | | | | |
| $t_W$ | Pulse Width | A Input | | | | 15 | | | 15 | | | 15 | | | 90 | | | 90 | | | ns |
| | | B Input | | | | 30 | | | 30 | | | 30 | | | 90 | | | 90 | | | |
| | | Reset Input | | | | 15 | | | 15 | | | 15 | | | 200 | | | 200 | | | |
| $t_{SETUP}$ | Reset Inactive State Setup Time | | | | | 25 | | | 25 | | | 25 | | | 200 | | | 200 | | | ns |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.
**Note 3:** $Q_A$ outputs are tested at $I_{OL}$ = MAX plus the limit value for $I_{IL}$ for the B input. This permits driving the B input while maintaining full fan-out capability.
**Note 4:** $I_{CC}$ is measured with all outputs open, both $R_0$ inputs grounded following a momentary connection to 4.5 V and all other inputs grounded.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | DM54/74 | | | | | | | | | | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | LS90 | | | | | | LS92 | | | | | | LS93 | | | | | | |
| | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | | $R_L$ = 2 kΩ, $C_L$ = 15 pF | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | | $R_L$ = 2 kΩ, $C_L$ = 15 pF | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | | $R_L$ = 2 kΩ, $C_L$ = 15 pF | | | |
| | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{max}$ | Maximum Count Frequency | A | $Q_A$ | 20 | 30 | | 32 | 42 | | 20 | 30 | | 32 | 42 | | 20 | 30 | | 32 | 42 | | MHz |
| | | B | $Q_B$ | 10 | | | 16 | | | 10 | | | 16 | | | 10 | | | 16 | | | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A | $Q_A$ | | 13 | 20 | | 10 | 16 | | 13 | 20 | | 10 | 16 | | 13 | 20 | | 10 | 16 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | 18 | 24 | | 12 | 18 | | 18 | 24 | | 12 | 18 | | 18 | 24 | | 12 | 18 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A | $Q_D$ | | 35 | 52 | | 32 | 48 | | 35 | 52 | | 32 | 48 | | 55 | 85 | | 46 | 70 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | 40 | 60 | | 34 | 50 | | 40 | 60 | | 34 | 50 | | 60 | 90 | | 46 | 70 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | B | $Q_B$ | | 15 | 23 | | 10 | 16 | | 15 | 23 | | 10 | 16 | | 15 | 23 | | 10 | 16 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | 20 | 30 | | 14 | 21 | | 20 | 30 | | 14 | 21 | | 20 | 30 | | 14 | 21 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | B | $Q_C$ | | 25 | 37 | | 21 | 32 | | 13 | 20 | | 10 | 16 | | 25 | 37 | | 21 | 32 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | 29 | 44 | | 23 | 35 | | 20 | 30 | | 14 | 21 | | 29 | 44 | | 23 | 35 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | B | $Q_D$ | | 24 | 36 | | 21 | 32 | | 24 | 36 | | 21 | 32 | | 40 | 60 | | 34 | 51 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | 29 | 44 | | 23 | 35 | | 29 | 44 | | 23 | 35 | | 46 | 70 | | 34 | 51 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Set-to-0 | Any | | 35 | 52 | | 26 | 40 | | 35 | 52 | | 26 | 40 | | 35 | 52 | | 26 | 40 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Set-to-9 | $Q_A$, $Q_D$ | | 23 | 35 | | 20 | 30 | | | | | | | | | | | | | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | $Q_B$, $Q_C$ | | 32 | 48 | | 26 | 40 | | | | | | | | | | | | | |
| $t_W$ | Pulse Width | A Input | | 25 | | | 15 | | | 25 | | | 15 | | | 25 | | | 15 | | | ns |
| | | B Input | | 50 | | | 30 | | | 50 | | | 30 | | | 50 | | | 30 | | | |
| | | Reset Input | | 25 | | | 15 | | | 25 | | | 15 | | | 25 | | | 15 | | | |
| $t_{SETUP}$ | Reset Inactive State Setup Time | | | 35 | | | 25 | | | 35 | | | 25 | | | 35 | | | 25 | | | ns |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

**Note 3:** $Q_A$ outputs are tested at $I_{OL}$ = max plus the limit value for $I_{IL}$ for the B input. This permits driving the B input while maintaining full fan-out capability.

**Note 4:** $I_{CC}$ is measured with all outputs open, both $R_0$ inputs grounded following momentary connection to 4.5 V and all other inputs grounded.

## Truth Tables

**90A, L90, LS90**
**BCD COUNT SEQUENCE**
**(See Note A)**

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

**90A, L90, LS90**
**BI-QUINARY (5-2)**
**(See Note B)**

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_A$ | $Q_D$ | $Q_C$ | $Q_B$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

**92A, LS92**
**COUNT SEQUENCE**
**(See Note C)**

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | H | L | L | L |
| 7 | H | L | L | H |
| 8 | H | L | H | L |
| 9 | H | L | H | H |
| 10 | H | H | L | L |
| 11 | H | H | L | H |

**93A, L93, LS93**
**COUNT SEQUENCE**
**(See Note C)**

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

**90A, L90, LS90**
**RESET/COUNT TRUTH TABLE**

| Reset Inputs | | | | Output | | | |
|---|---|---|---|---|---|---|---|
| R0(1) | R0(2) | R9(1) | R9(2) | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | X | L | L | L | L |
| H | H | X | L | L | L | L | L |
| X | X | H | H | H | L | L | H |
| X | L | X | L | COUNT | | | |
| L | X | L | X | COUNT | | | |
| L | X | X | L | COUNT | | | |
| X | L | L | X | COUNT | | | |

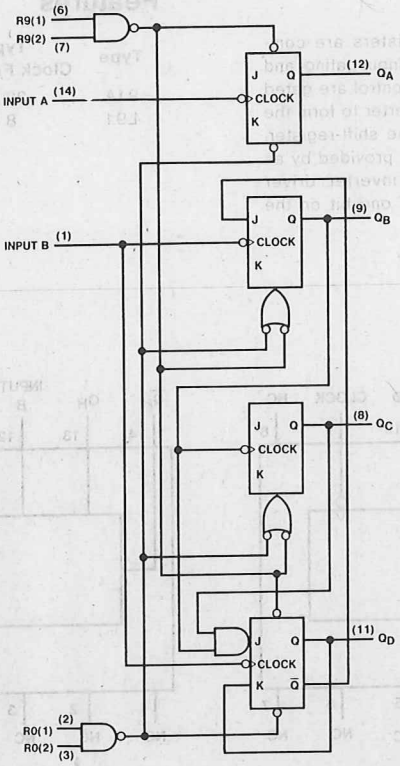
**92A, LS92, 93A, L93, LS93**
**RESET/COUNT TRUTH TABLE**

| Reset Inputs | | Output | | | |
|---|---|---|---|---|---|
| R0(1) | R0(2) | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | L | L | L |
| L | X | COUNT | | | |
| X | L | COUNT | | | |

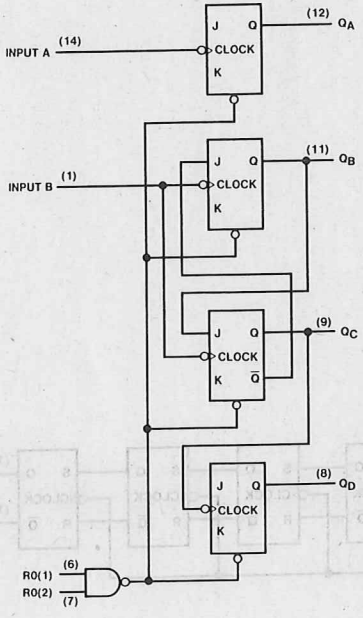
**Note A:** Output $Q_A$ is connected to input B for BCD count.
**Note B:** Output $Q_D$ is connected to input A for bi-quinary count.
**Note C:** Output $Q_A$ is connected to input B.
**Note D:** H = High Level, L = Low Level, X = Don't Care.

## Logic Diagrams

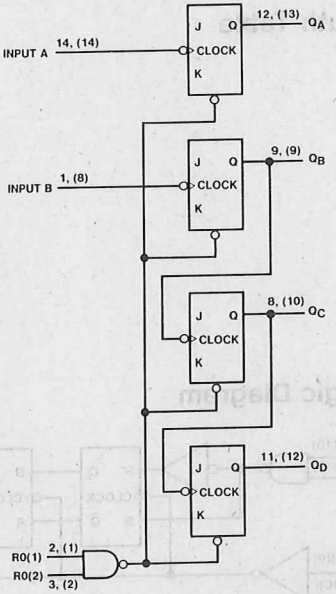
### 90A, L90, LS90




### 92A, LS92




### 93A, L93, LS93




**Note:** Numbers in parenthesis are for L93 only.

The J and K inputs shown without connection are for reference only and are functionally at a high level.

# 8-Bit Serial Shift Registers

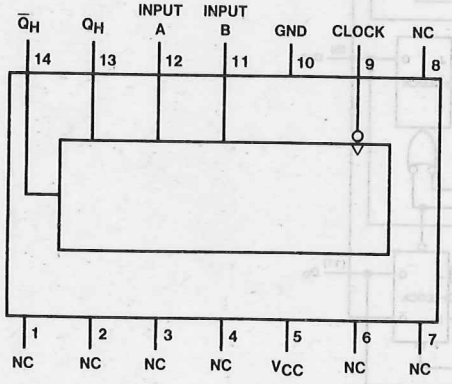
## General Description

These serial-in, serial-out 8-bit shift registers are composed of eight R-S master-slave flip-flops, input gating, and a clock driver. Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift-register. Drive for the internal common clock line is provided by an inverting clock driver. This clock pulse inverter/driver causes these circuits to shift information one bit on the positive edge of an input clock pulse.

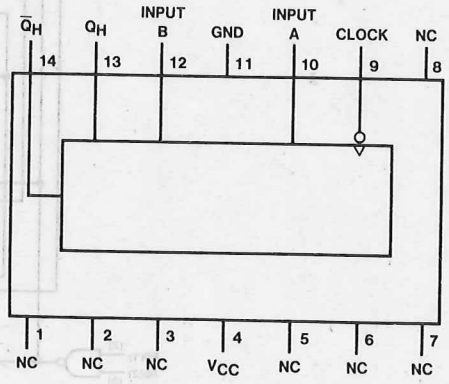
## Features

| Type | Typical Clock Frequency | Typical Power Dissipation |
|---|---|---|
| 91A | 22 MHz | 175 mW |
| L91 | 8 MHz | 17.5 mW |

## Connection Diagrams




54L91 (J); 74L91 (N)



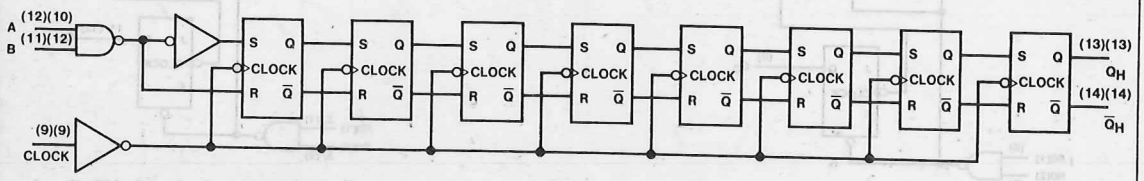

54L91/74L91 (W)

## Truth Table

| Inputs AT $t_n$ | | Outputs AT $t_{n+8}$ | |
|---|---|---|---|
| A | B | $Q_H$ | $\overline{Q}_H$ |
| H | H | H | L |
| L | X | L | H |
| X | L | L | H |

H = High, L = Low
X = Don't Care
$t_n$ = Reference bit time, clock low,
$t_{n+8}$ = Bit time after 8 low-to-high clock transitions.

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM54/74 L91 Min | DM54/74 L91 Typ(1) | DM54/74 L91 Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.7 | V |
| $I_{OH}$ | High Level Output Current | | | | | −200 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | 2.4 | 2.8 | | V |
| $I_{OL}$ | Low Level Output Current | | DM54 | | | 2 | mA |
| | | | DM74 | | | 3.6 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OL}$ = Max | DM54 | | 0.15 | 0.3 | V |
| | | | DM74 | | 0.2 | 0.4 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 0.1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 10 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | −0.18 | mA |
| | | | $V_I$ = 0.4 V | | | | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | DM54 | −3 | −8 | −15 | mA |
| | | | DM74 | −3 | −8 | −15 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ =Max (3) | DM54 | | 3.5 | 6.6 | mA |
| | | | DM74 | | 3.5 | 6.6 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.
**Note 3:** $I_{CC}$ is measured after the eighth clock pulse with the output open and A and B inputs grounded.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | DM54/74 L91 Min | DM54/74 L91 Typ | DM54/74 L91 Max | Units |
|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 50 pF, $R_L$ = 4 kΩ | 4 | 8 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | | 40 | 80 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | 65 | 130 | ns |
| $t_{W(CLOCK)}$ | Width of Clock Input Pulse | | 120 | | | ns |
| $t_{SETUP}$ | Setup Time | | 120 | | | ns |
| $t_{HOLD}$ | Hold Time | | 0 | | | ns |

# 4-Bit Parallel Access Shift Registers

## General Description

These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation.

Parallel (broadside) load
Shift right (the direction $Q_A$ toward $Q_D$)
Shift left (the direction $Q_D$ toward $Q_A$)

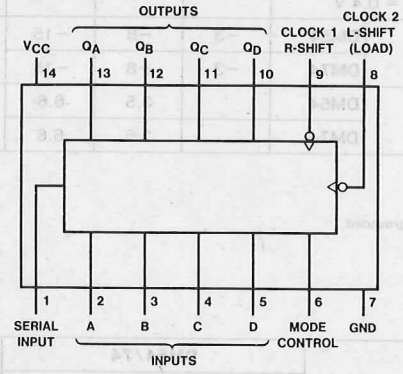
Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop ($Q_D$ to input C, etc.) and serial data is entered at input D. The clock input may be applied simultaneously to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the truth table will also ensure that register contents are protected.

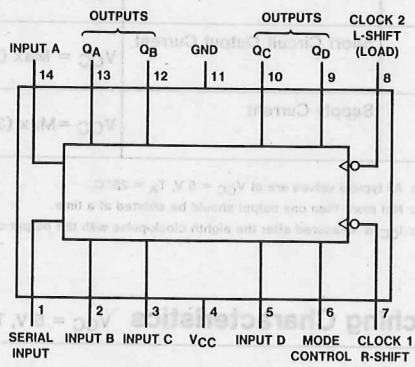
## Features

| Type | Typical Maximum Clock Frequency | Typical Power Dissipation |
|---|---|---|
| 95 | 36 MHz | 250 mW |
| L95 | 14 MHz | 24 mW |

## Connection Diagrams

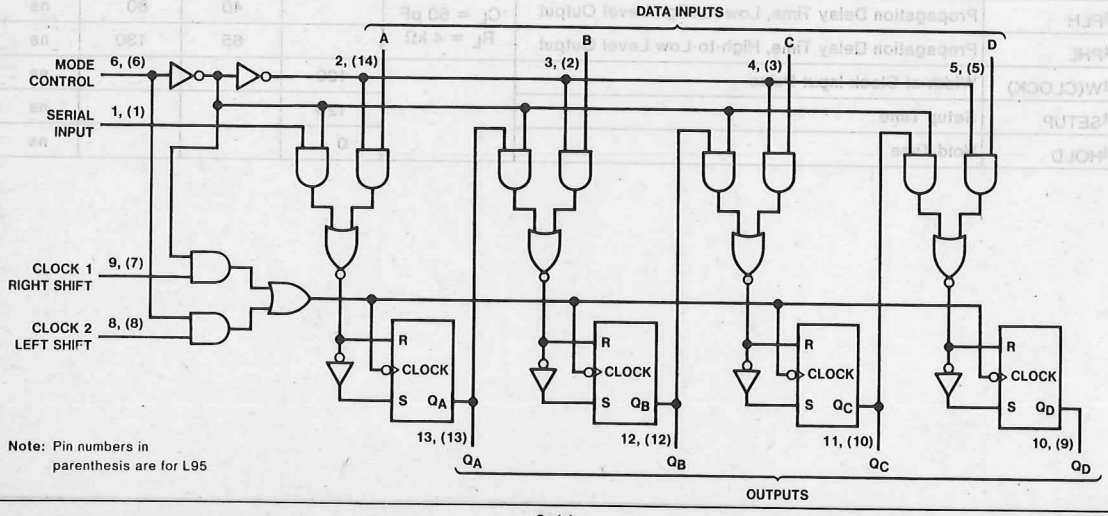



5495 (J,W); 7495 (N)




54L95 (J,W); 74L95 (N)

## Logic Diagram




Note: Pin numbers in parenthesis are for L95

## Electrical Characteristics Over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM54/74 95 | | | DM54/74 L95 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | | 0.8 | | | 0.7 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | | −1.5 | | | N/A | V |
| $I_{OH}$ | High Level Output Current | | | | | | | −800 | | | −200 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.4 | 3.4 | | 2.4 | 3.1 | | V |
| | | | | | DM74 | 2.4 | 3.4 | | 2.4 | 3.1 | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 16 | | | 2 | mA |
| | | | | | DM74 | | | 16 | | | 3.6 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | 0.13 | 0.3 | V |
| | | | | | DM74 | | 0.2 | 0.4 | | 0.2 | 0.4 | |
| | | | | $I_{OL}$ = 4 mA | DM74 | | | | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | Mode Control | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | | 1 | | | 0.2 | mA |
| | | Others | | | | | | 1 | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | Mode Control | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | | 80 | | | 20 | μA |
| | | Others | | | | | | 40 | | | 10 | |
| $I_{IL}$ | Low Level Input Current | Mode Control | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | | | −0.36 | mA |
| | | Others | | | | | | | | | −0.18 | |
| | | Mode Control | | $V_I$ = 0.4 V | | | | −3.2 | | | | |
| | | Others | | | | | | −1.6 | | | | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | | −18 | | −57 | −3 | −9 | −15 | mA |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (3) | | | | 50 | 75 | | 4.8 | 8 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time.

**Note 3:** $I_{CC}$ is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and a momentary 3 V, then ground, applied to both clock inputs.

6

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | DM54/74 95 Min | DM54/74 95 Typ | DM54/74 95 Max | Conditions | DM54/74 L95 Min | DM54/74 L95 Typ | DM54/74 L95 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF, $R_L$ = 400 Ω | 25 | 36 | | $C_L$ = 50 pF, $R_L$ = 4 kΩ | 6 | 14 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output From Clock | | | 25 | 35 | | | 42 | 90 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Clock | | | 25 | 35 | | | 48 | 90 | ns |
| $t_{W(CLOCK)}$ | Width of Clock Pulse | | 15 | | | | 90 | | | ns |
| $t_{SETUP}$ | Setup Time, High-Level Data | | 20 | 10 | | | 50 | | | ns |
| $t_{SETUP}$ | Setup Time, Low-Level Data | | 20 | 10 | | | 50 | | | ns |
| $t_{HOLD}$ | Hold Time, High-Level or Low-Level Data | | 0 | −10 | | | 0 | | | ns |
| $t_{ENABLE\ 1}$ | Time to Enable Clock 1 | | 20 | | | | 120 | | | ns |
| $t_{ENABLE\ 2}$ | Time to Enable Clock 2 | | 15 | | | | 100 | | | ns |
| $t_{INHIBIT\ 1}$ | Time to Inhibit Clock 1 | | 10 | | | | 0 | | | ns |
| $t_{INHIBIT\ 2}$ | Time to Inhibit Clock 2 | | 10 | | | | 0 | | | ns |

## Truth Table

| Inputs | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Mode Control | Clocks 2 (L) | Clocks 1 (R) | Serial | Parallel A | Parallel B | Parallel C | Parallel D | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| H | H | X | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| H | ↓ | X | X | a | b | c | d | a | b | c | d |
| H | ↓ | X | X | $Q_B$† | $Q_C$† | $Q_D$† | d | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | d |
| L | L | H | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| L | X | ↓ | H | X | X | X | X | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| L | X | ↓ | L | X | X | X | X | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| ↑ | L | L | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| ↓ | L | L | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| ↓ | L | H | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| ↑ | H | L | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| ↑ | H | H | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |

†Shifting left requires external connection of $Q_B$ to A, $Q_C$ to B, $Q_D$ to C. Serial data is entered at input D.

H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care (Any input, including transitions)

↓ = Transition from high to low level, ↑ = Transition from low to high level

a, b, c, d, = The level of steady state input at inputs A, B, C, or D, respectively.

$Q_{A0}$, $Q_{B0}$, $Q_{C0}$, $Q_{D0}$ = The level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the indicated steady state input conditions were established.

$Q_{An}$, $Q_{Bn}$, $Q_{Cn}$, $Q_{Dn}$ = The level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the most recent ↓ transition of the clock.

# 5-Bit Shift Registers

## General Description

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may also be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is low. Clearing is independent of the level of the clock input.

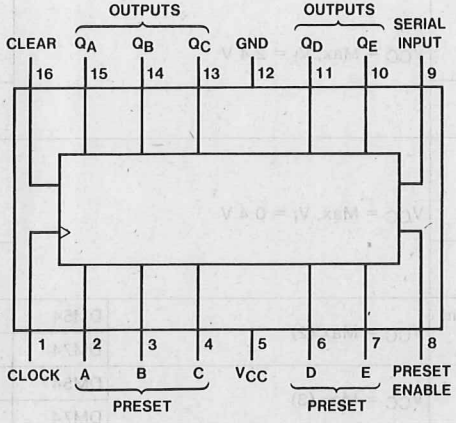
The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting is also independent of the level of the clock input.

Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

## Features

- N-bit serial-to-parallel converter
- N-bit parallel-to-serial converter
- N-bit storage register

## Connection Diagram




5496 (J,W); 7496 (J,N,W)

## Truth Table

| Inputs | | | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clear | Preset Enable | Preset A | B | C | D | E | Clock | Serial | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $Q_E$ |
| L | L | X | X | X | X | X | X | X | L | L | L | L | L |
| L | X | L | L | L | L | L | X | X | L | L | L | L | L |
| H | H | H | H | H | H | H | X | X | H | H | H | H | H |
| H | H | L | L | L | L | L | L | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $Q_{E0}$ |
| H | H | H | L | H | L | H | L | X | H | $Q_{B0}$ | H | $Q_{D0}$ | H |
| H | L | X | X | X | X | X | L | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $Q_{E0}$ |
| H | L | X | X | X | X | X | ↑ | H | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ |
| H | L | X | X | X | X | X | ↑ | L | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ |

H = high level (steady state), L = low level (steady state)
X = don't care (any input, including transitions)
↑ = transition from low to high level
$Q_{A0}$, $Q_{B0}$, etc. = the level of $Q_A$, $Q_B$, etc., respectively before the indicated steady state input conditions were established.
$Q_{An}$, $Q_{Bn}$, etc. = the level of $Q_A$, $Q_B$, etc., respectively before the most recent ↑ transition of the clock.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

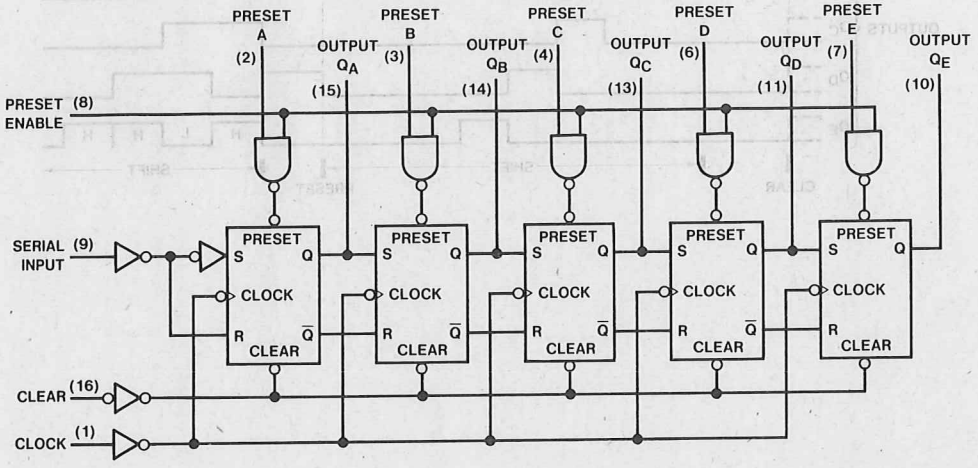
| Parameter | | | Conditions | | DM54/74 96 Min | DM54/74 96 Typ (1) | DM54/74 96 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = −400 μA | DM54 | 2.4 | 3.4 | | V |
| | | | | DM74 | 2.4 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | mA |
| | | | | DM74 | | | 16 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | V |
| | | | | DM74 | | 0.2 | 0.4 | |
| $I_I$ | Input Current at Maximum | | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | Any Input Except Preset Enable | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | μA |
| | | Preset Enable | | | | | 200 | |
| $I_{IL}$ | Low Level Input Current | Any Input Except Preset Enable | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −1.6 | mA |
| | | Preset Enable | | | | | −8 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | DM54 | −20 | | −57 | mA |
| | | | | DM74 | −18 | | −57 | |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (3) | DM54 | | 48 | 68 | mA |
| | | | | DM74 | | 48 | 79 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.
**Note 3:** $I_{CC}$ is measured with the clear input grounded and all other inputs and outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

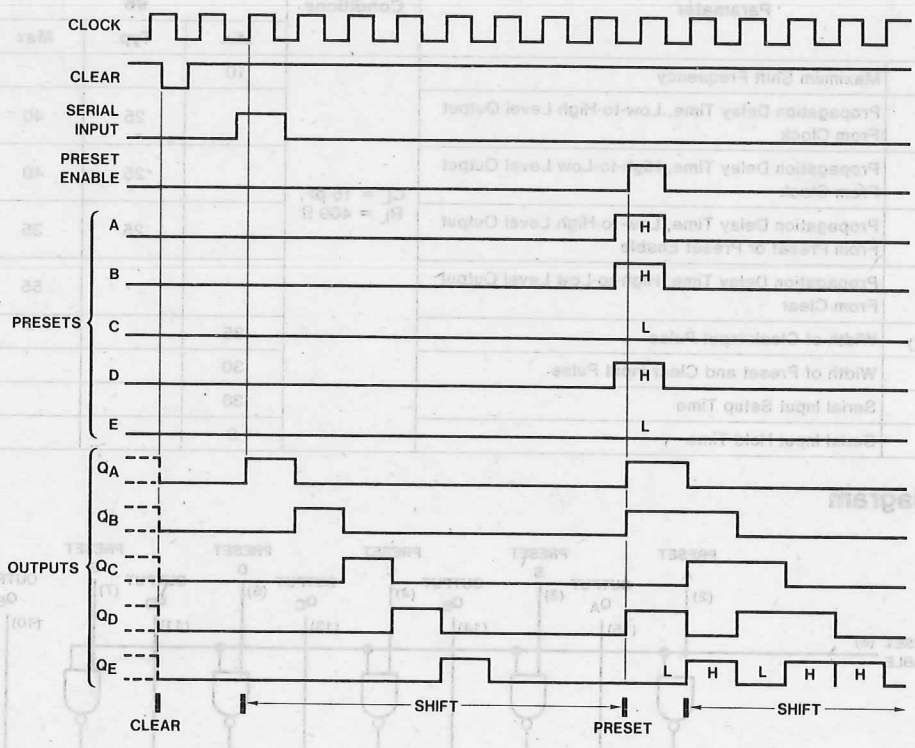
| Parameter | | Conditions | DM54/74 96 | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $f_{max}$ | Maximum Shift Frequency | $C_L$ = 15 pF, $R_L$ = 400 Ω | 10 | | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output From Clock | | | 25 | 40 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Clock | | | 25 | 40 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output From Preset or Preset Enable | | | 25 | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Clear | | | | 55 | ns |
| $t_{W(CLOCK)}$ | Width of Clock Input Pulse | | 35 | | | ns |
| $t_W$ | Width of Preset and Clear Input Pulse | | 30 | | | ns |
| $t_{SETUP}$ | Serial Input Setup Time | | 30 | | | ns |
| $t_{HOLD}$ | Serial Input Hold Time | | 0 | | | ns |

## Logic Diagram



## Timing Diagram

Typical Clear, Shift, Preset, and Shift Sequences



# 4-Bit Storage Registers

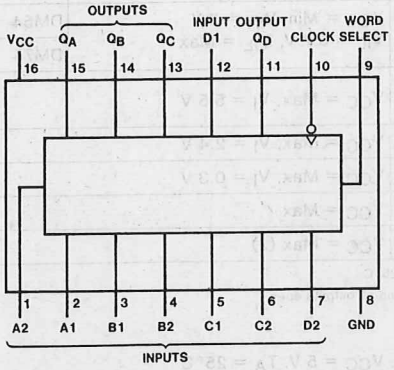
## General Description

These data selectors/storage registers are composed of four S-R master-slave flip-flops, four AND-OR INVERT gates, one buffer, and six inverter/drivers.

When the word select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high level input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is shifted to the output terminals on the negative-going edge of the clock pulse.

Typical clock frequency is 12 MHz.

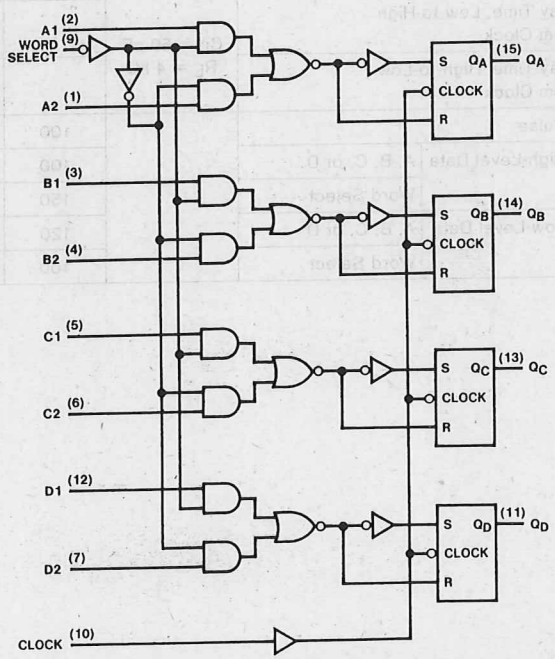
## Connection Diagram




Word select low for word 1, word select high for word 2, see description

**54L98 (J,W); 74L98 (N)**

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

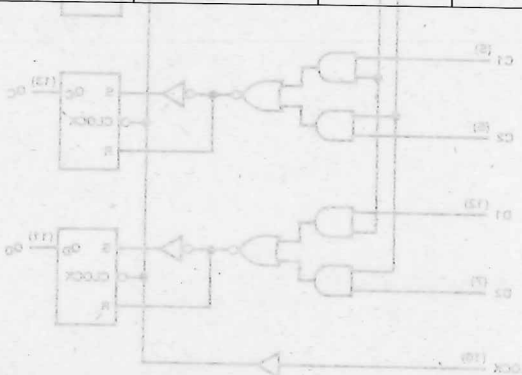
| Parameter | | Conditions | | DM54/74 L98 Min | DM54/74 L98 Typ (1) | DM54/74 L98 Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.7 | V |
| $I_{OH}$ | High Level Output Current | | | | | −200 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.7 V, $I_{OH}$ = −200 μA | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | DM54 | | | 2 | mA |
| | | | DM74 | | | 3.6 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.7 V, $I_{OL}$ = Max | DM54 | | 0.15 | 0.3 | V |
| | | | DM74 | | | 0.4 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 100 | μA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 10 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.3 V | | | | −0.18 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max | | −3 | −9 | −15 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (2) | | | 6 | 8 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** $I_{CC}$ is measured with all inputs grounded and all outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | Conditions | DM54/74 L98 Min | DM54/74 L98 Typ | DM54/74 L98 Max | Units |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Clock Frequency | | $C_L$ = 50 pF, $R_L$ = 4 kΩ | 6 | 12 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output From Clock | | | | 40 | 80 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Clock | | | | 65 | 100 | ns |
| $t_{W(CLOCK)}$ | Width of Clock Pulse | | | 100 | 65 | | ns |
| $t_{SETUP(H)}$ | Setup Time for High-Level Data | A, B, C, or D | | 100 | | | ns |
| | | Word Select | | 150 | | | |
| $t_{SETUP(L)}$ | Setup Time for Low-Level Data | A, B, C, or D | | 120 | | | |
| | | Word Select | | 100 | | | |



## General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The LS138 and S138 decode one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The LS139 and S139 comprise two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

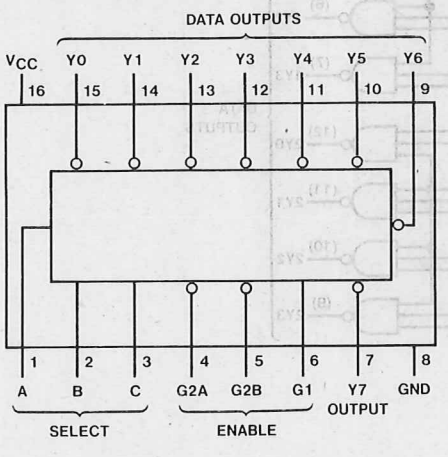
All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

## Features

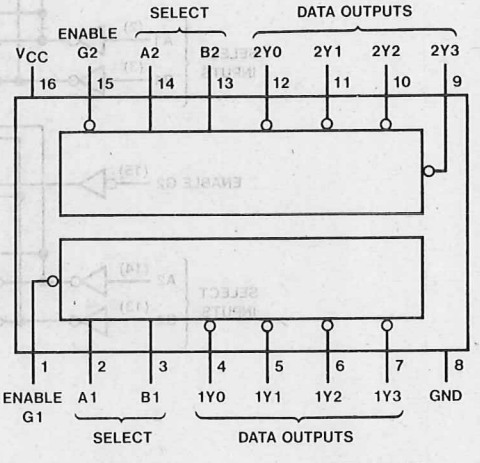
- Designed specifically for high-speed:
  - Memory decoders
  - Data transmission systems
- S138 and LS138 3-to-8-line decoders incorporate 3 enable inputs to simplify cascading and/or data reception
- S139 and LS139 contain two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance

| Type | Typical Propagation Delay (3 Levels of Logic) | Typical Power Dissipation |
|---|---|---|
| LS138 | 21 ns | 32 mW |
| S138 | 8 ns | 245 mW |
| LS139 | 21 ns | 34 mW |
| S139 | 7.5 ns | 300 mW |

## Connection Diagrams



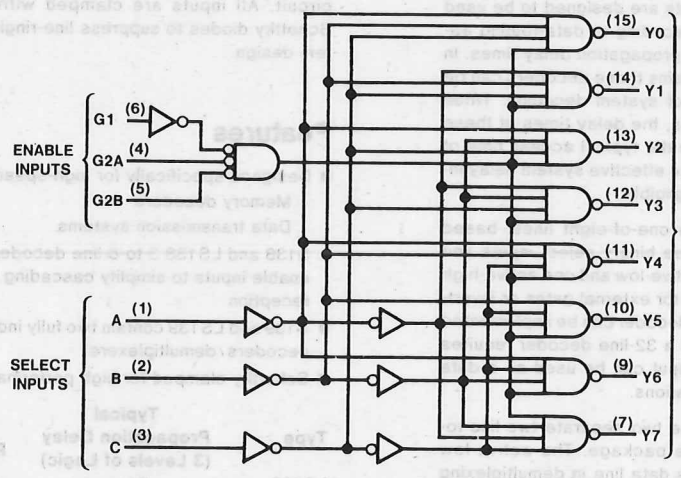

**54LS138 (J,W)** **74LS138 (N)**
**54S138 (J,W)** **74S138 (N)**



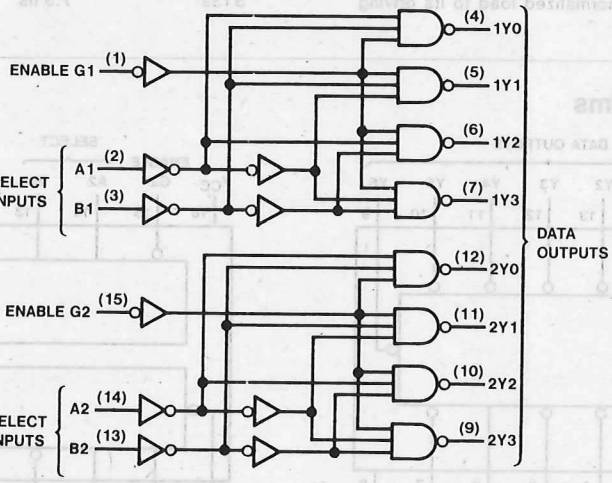

**54LS139 (J,W)** **74LS139 (N)**
**54S139 (J,W)** **74S139 (N)**

## Logic Diagrams

138, S138, LS138




139, S139, LS139



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 LS138, LS139 | | | DM54/74 S138, S139 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | | −1.5 | | | −1.2 | V |
| $I_{OH}$ | High Level Output Current | | | | | | −400 | | | −1000 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 4 | | | 20 | mA |
| | | | | DM74 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | DM74 | | 0.35 | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 4 mA | DM74 | | 0.25 | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | | | | 1 | mA |
| | | | $V_I$ = 7 V | | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.7 V | | | | 20 | | | 50 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.4 V | | | | −0.36 | | | | mA |
| | | | $V_I$ = 0.5 V | | | | | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −20 | | −100 | −40 | | −100 | mA |
| | | | | DM74 | −20 | | −100 | −40 | | −100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max, Outputs Enabled and Open | | LS138, S138 | | 6.3 | 10 | | 49 | 74 | mA |
| | | | | LS139, S139 | | 6.8 | 11 | | 60 | 90 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Levels of Delay | Conditions | DM54/74 LS138 | | | DM54/74 LS139 | | | Conditions | DM54/74 S138 | | | DM54/74 S139 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | Min | Typ | Max | | Min | Typ | Max | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Binary Select | Any | 2 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 13 | 18 | | 13 | 18 | $C_L$ = 15 pF, $R_L$ = 280 kΩ | | 4.5 | 7 | | 5 | 7.5 | ns |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 16 | 27 | | 16 | 27 | $C_L$ = 50 pF, $R_L$ = 280 kΩ | | 6 | 9 | | 6.5 | 10 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 17 | 27 | | 17 | 27 | $C_L$ = 15 pF, $R_L$ = 280 kΩ | | 7 | 10.5 | | 6.5 | 10 | ns |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 23 | 40 | | 23 | 40 | $C_L$ = 50 pF, $R_L$ = 280 kΩ | | 9 | 14 | | 8.5 | 13 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | | 3 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 13 | 18 | | 13 | 18 | $C_L$ = 15 pF, $R_L$ = 280 kΩ | | 7.5 | 12 | | 7 | 12 | ns |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 16 | 27 | | 16 | 27 | $C_L$ = 50 pF, $R_L$ = 280 kΩ | | 9 | 14 | | 8.5 | 13 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 17 | 27 | | 17 | 27 | $C_L$ = 15 pF, $R_L$ = 280 kΩ | | 8 | 12 | | 8 | 12 | ns |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 23 | 40 | | 23 | 40 | $C_L$ = 50 pF, $R_L$ = 280 kΩ | | 10 | 15 | | 10 | 15 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Enable | Any | 2 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 13 | 18 | | 13 | 18 | $C_L$ = 15 pF, $R_L$ = 280 kΩ | | 5 | 8 | | 5 | 8 | ns |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 16 | 27 | | 16 | 27 | $C_L$ = 50 pF, $R_L$ = 280 kΩ | | 6.5 | 10 | | 6.5 | 10 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 16 | 24 | | 16 | 24 | $C_L$ = 15 pF, $R_L$ = 280 kΩ | | 7 | 11 | | 6.5 | 10 | ns |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 22 | 40 | | 22 | 40 | $C_L$ = 50 pF, $R_L$ = 280 kΩ | | 9 | 14 | | 8.5 | 13 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | | 3 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 13 | 18 | | | N/A | $C_L$ = 15 pF, $R_L$ = 280 kΩ | | 7 | 11 | | | N/A | ns |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 16 | 27 | | | N/A | $C_L$ = 50 pF, $R_L$ = 280 kΩ | | 8.5 | 13 | | | N/A | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 19 | 28 | | | N/A | $C_L$ = 15 pF, $R_L$ = 280 kΩ | | 7 | 11 | | | N/A | ns |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 25 | 40 | | | N/A | $C_L$ = 50 pF, $R_L$ = 280 kΩ | | 9 | 14 | | | N/A | |

## Truth Tables

LS138, S138

| Inputs | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Enable | | Select | | | | | | | | | | |
| G1 | G2* | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |

*G2 = G2A + G2B

H = High level, L = low level, X = don't care

LS139, S139

| Inputs | | | Outputs | | | |
|---|---|---|---|---|---|---|
| Enable | Select | | | | | |
| G | B | A | Y0 | Y1 | Y2 | Y3 |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

H = high level, L = low level, X = don't care

# Priority Encoders

## General Description

These TTL encoders feature priority decoding of the input data to ensure that only the highest-order data line is encoded. The DM54147 and DM74147 encode nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. All inputs are buffered to represent one normalized Series 54/74 load. The DM54148 and DM74148 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input E1 and enable output E0) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level.

## Features

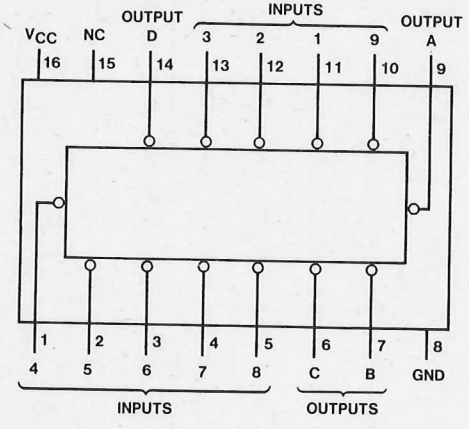
**DM54147, DM74147**

- Encodes 10-line decimal to 4-line BCD
- Applications include:
  - Keyboard encoding
  - Range selection
- Typical data delay 10 ns
- Typical power dissipation 225 mW

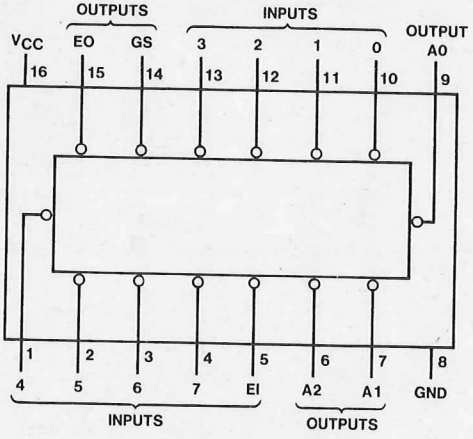
**DM54148, DM74148**

- Encodes 8 data lines to 3-line binary (octal)
- Applications include:
  - N-bit encoding
  - Code converters and generators
- Typical data delay 10 ns
- Typical power dissipation 190 mW

## Connection Diagrams




54147 (J,W); 74147 (J,N,W)




54148 (J,W); 74148 (J,N,W)

## Truth Tables

**54147/74147**

| Inputs | | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | D | C | B | A |
| H | H | H | H | H | H | H | H | H | H | H | H | H |
| X | X | X | X | X | X | X | X | L | L | H | H | L |
| X | X | X | X | X | X | X | L | H | L | H | H | H |
| X | X | X | X | X | X | L | H | H | H | L | L | L |
| X | X | X | X | X | L | H | H | H | H | L | L | H |
| X | X | X | X | L | H | H | H | H | H | L | H | L |
| X | X | X | L | H | H | H | H | H | H | L | H | H |
| X | X | L | H | H | H | H | H | H | H | H | L | L |
| X | L | H | H | H | H | H | H | H | H | H | L | H |
| L | H | H | H | H | H | H | H | H | H | H | H | L |

**54148/74148**

| Inputs | | | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E1 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | A2 | A1 | A0 | GS | E0 |
| H | X | X | X | X | X | X | X | X | H | H | H | H | H |
| L | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | X | X | X | X | X | X | X | L | L | L | L | L | H |
| L | X | X | X | X | X | X | L | H | L | L | H | L | H |
| L | X | X | X | X | X | L | H | H | L | H | L | L | H |
| L | X | X | X | X | L | H | H | H | L | H | H | L | H |
| L | X | X | X | L | H | H | H | H | H | L | L | L | H |
| L | X | X | L | H | H | H | H | H | H | L | H | L | H |
| L | X | L | H | H | H | H | H | H | H | H | L | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | L | H |

H = High Logic Level, L = Low Logic Level, X = Don't care

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | DM54/74 | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 147 | | | 148 | | | |
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | | −800 | | | −800 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OH}$ = −800 μA | | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | | 0.4 | | | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max, $V_I$ 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | 0 Input | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | N/A | | | 40 | μA |
| | | Others | | | | | 40 | | | 80 | |
| $I_{IL}$ | Low Level Input Current | 0 Input | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | N/A | | | −1.6 | mA |
| | | Others | | | | | −1.6 | | | −3.2 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | −35 | | −85 | −35 | | −85 | mA |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (3) | Condition 1 | | 50 | 70 | | 40 | 60 | mA |
| | | | | Condition 2 | | 42 | 62 | | 35 | 55 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time.

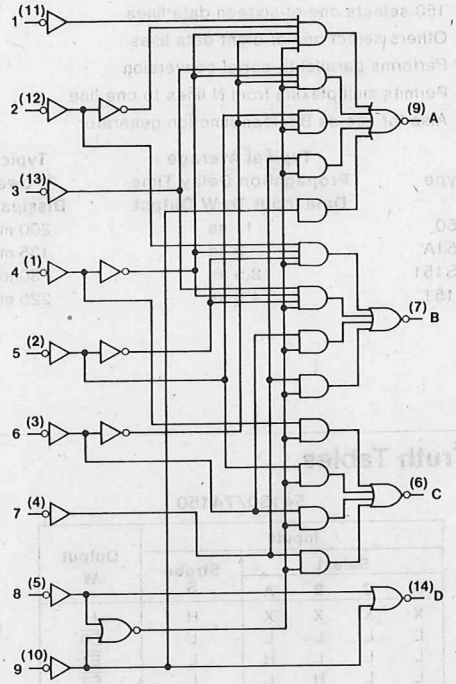
**Note 3:** For DM54147/DM74147, $I_{CC}$ (condition 1) is measured with input 7 grounded, other inputs and outputs open; $I_{CC}$ (condition 2) is measured with all inputs and outputs open. For DM54148/DM74148, $I_{CC}$ (condition 1) is measured with inputs 7 and E1 grounded, other inputs and outputs open; $I_{CC}$ (condition 2) is measured with all inputs and outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

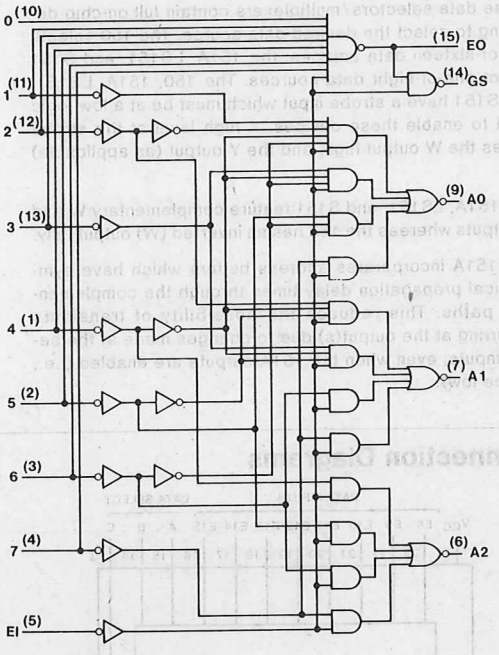
| Parameter | | From (Input) | To (Output) | Waveform | Conditions | DM54/74 147 Min | DM54/74 147 Typ | DM54/74 147 Max | DM54/74 148 Min | DM54/74 148 Typ | DM54/74 148 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | 0 thru 9 | A, B, C, D | In-Phase Output | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 9 | 14 | | 10 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 7 | 11 | | 9 | 14 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | 0 thru 9 | A, B, C, D | Out-of-Phase Output | | | 13 | 19 | | 13 | 19 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 12 | 19 | | 12 | 19 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | 0 thru 7 | E0 | Out-of-Phase Output | | | N/A | | | 6 | 10 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | N/A | | | 14 | 25 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | 0 thru 7 | GS | In-Phase Output | | | N/A | | | 18 | 30 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | N/A | | | 14 | 25 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | E1 | A0, A1, or A2 | In-Phase Output | | | N/A | | | 10 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | N/A | | | 10 | 15 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | E1 | GS | In-Phase Output | | | N/A | | | 8 | 12 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | N/A | | | 10 | 15 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | E1 | E0 | In-Phase Output | | | N/A | | | 10 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | N/A | | | 17 | 30 | ns |

## Logic Diagrams

147




148




6

## Data Selectors/Multiplexers

## General Description

These data selectors/multiplexers contain full on-chip decoding to select the desired data source. The 150 selects one-of-sixteen data sources; the 151A, LS151, and S151 select one-of-eight data sources. The 150, 151A, LS151, and S151 have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output (as applicable) low.

The 151A, LS151, and S151 feature complementary W and Y outputs whereas the 150 has an inverted (W) output only.

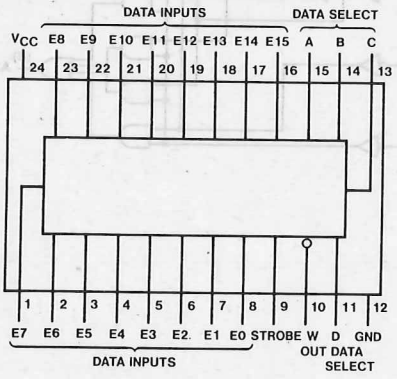
The 151A incorporates address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the 151A outputs are enabled (i.e., strobe low).

## Features

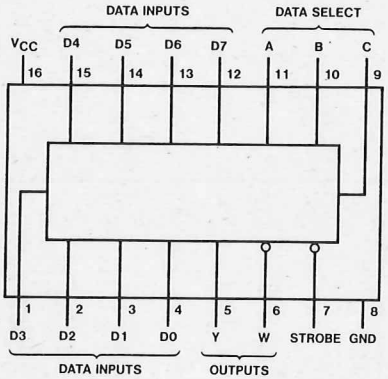
- 150 selects one-of-sixteen data lines
- Others select one-of-eight data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use as Boolean function generator

| Type | Typical Average Propagation Delay Time Data Input To W Output | Typical Power Dissipation |
|---|---|---|
| 150 | 11 ns | 200 mW |
| 151A | 9 ns | 135 mW |
| LS151 | 12.5 ns | 30 mW |
| S151 | 4.5 ns | 225 mW |

## Connection Diagrams




**54150 (J,F); 74150 (N)**




**54151A (J,W)**
**54LS151 (J,W)**
**54S151 (J,W)**

**74151A (N)**
**74LS151 (N)**
**74S151 (N)**

## Truth Tables

**54150/74150**

| Inputs | | | | | Output |
|---|---|---|---|---|---|
| Select | | | | Strobe | |
| D | C | B | A | S | W |
| X | X | X | X | H | H |
| L | L | L | L | L | $\overline{E0}$ |
| L | L | L | H | L | $\overline{E1}$ |
| L | L | H | L | L | $\overline{E2}$ |
| L | L | H | H | L | $\overline{E3}$ |
| L | H | L | L | L | $\overline{E4}$ |
| L | H | L | H | L | $\overline{E5}$ |
| L | H | H | L | L | $\overline{E6}$ |
| L | H | H | H | L | $\overline{E7}$ |
| H | L | L | L | L | $\overline{E8}$ |
| H | L | L | H | L | $\overline{E9}$ |
| H | L | H | L | L | $\overline{E10}$ |
| H | L | H | H | L | $\overline{E11}$ |
| H | H | L | L | L | $\overline{E12}$ |
| H | H | L | H | L | $\overline{E13}$ |
| H | H | H | L | L | $\overline{E14}$ |
| H | H | H | H | L | $\overline{E15}$ |

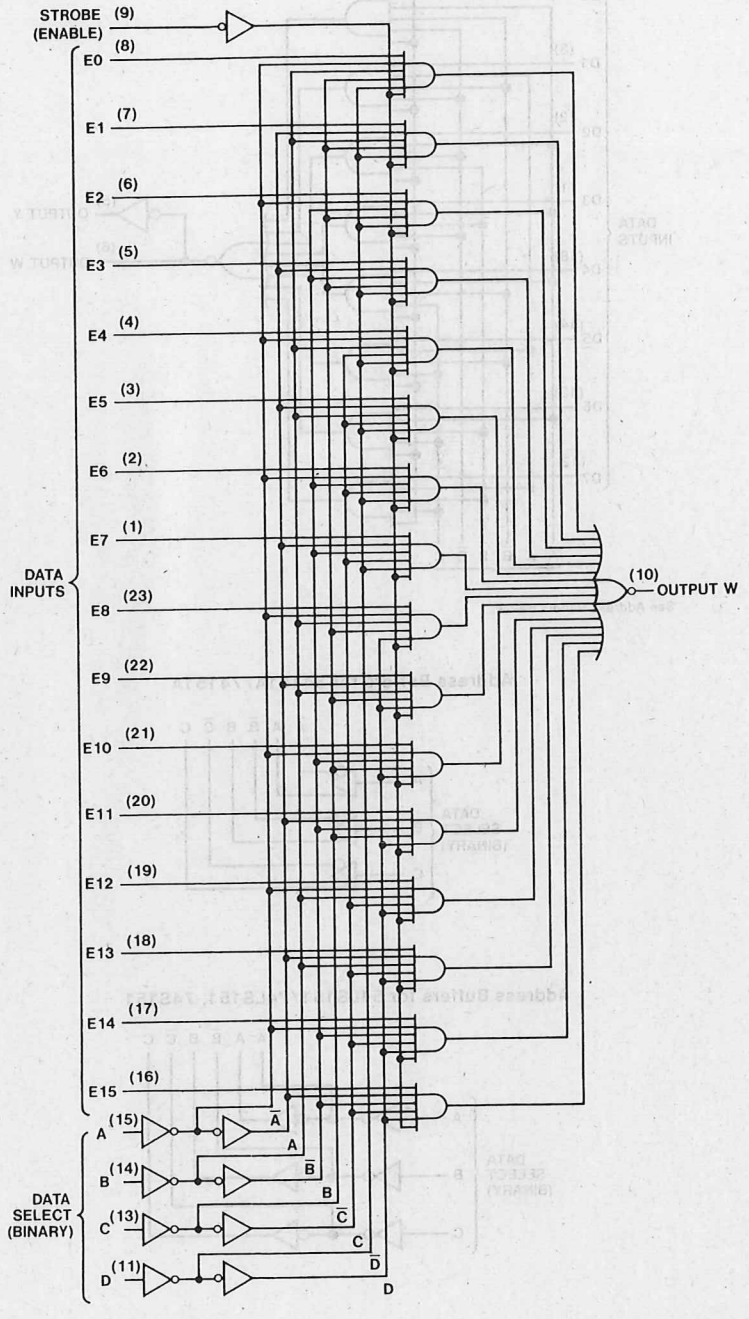
**54151A/74151A, 54LS151/74LS151, 74S151**

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| Select | | | Strobe | | |
| C | B | A | S | Y | W |
| X | X | X | H | L | H |
| L | L | L | L | D0 | $\overline{D0}$ |
| L | L | H | L | D1 | $\overline{D1}$ |
| L | H | L | L | D2 | $\overline{D2}$ |
| L | H | H | L | D3 | $\overline{D3}$ |
| H | L | L | L | D4 | $\overline{D4}$ |
| H | L | H | L | D5 | $\overline{D5}$ |
| H | H | L | L | D6 | $\overline{D6}$ |
| H | H | H | L | D7 | $\overline{D7}$ |

H = High Level, L = Low Level, X = Don't Care
$\overline{E0}$, $\overline{E1}$...$\overline{E15}$ = the complement of the level of the respective E input
D0, D1...D7 = the level of the respective D input

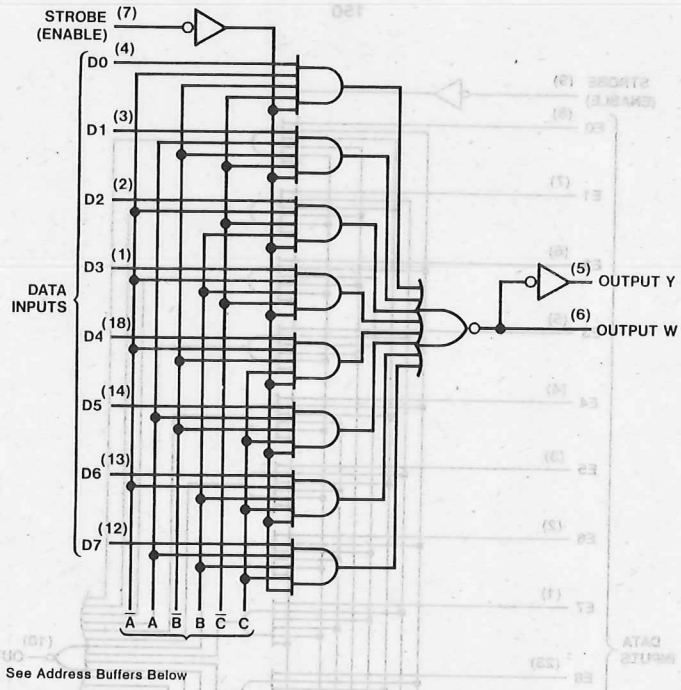
## Logic Diagrams

150

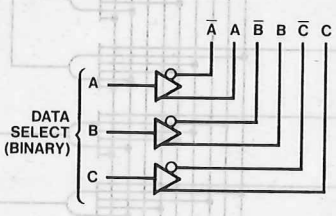


## Logic Diagrams (Continued)

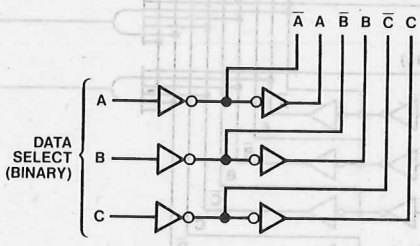
151A, LS151, S151




Address Buffers for 54151A/74151A




Address Buffers for 54LS151/74LS151, 74S151



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 150, 151A | | | DM54/74 LS151 | | | DM54/74 S151 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | | | | | V |
| | | | $I_I$ = −18 mA | | | | | | | −1.5 | | | −1.2 | |
| $I_{OH}$ | High Level Output Current | | | | | | −800 | | | −400 | | | −1000 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.4 | | | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.4 | | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Voltage | | | DM54 | | | 16 | | | 4 | | | 20 | mA |
| | | | | DM74 | | | 16 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | | 0.4 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | DM74 | | | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 4 mA | DM74 | | | | | 0.25 | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | | | | 1 | mA |
| | | | $V_I$ = 7 V | | | | | | | 0.1 | | | | |
| $I_{IH}$ | High Level input current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | | | | | μA |
| | | | $V_I$ = 2.7 V | | | | | | | 20 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.4 V | | | | −1.6 | | | −0.4 | | | | mA |
| | | | $V_I$ = 0.5 V | | | | | | | | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −20 | | −55 | −20 | | −100 | −40 | | −100 | mA |
| | | | | DM74 | −18 | | −55 | −20 | | −100 | −40 | | −100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | 150 | | 40 | 68 | | | | | | | mA |
| | | | | 151A | | 27 | 48 | | | | | | | |
| | | | | Others | | | | | 6 | 10 | | 45 | 70 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS or DM54S/74S duration of short circuit should not exceed one second.

**Note 3:** $I_{CC}$ is measured with the strobe and data select inputs at 4.5 V, all other inputs and outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | DM54/74 Conditions | DM54/74 150 Min | 150 Typ | 150 Max | 151A Min | 151A Typ | 151A Max | DM54/74 LS151 Conditions | LS151 Min | LS151 Typ | LS151 Max | DM54/74 S151 Conditions | S151 Min | S151 Typ | S151 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Select (4 levels) | Y | $C_L$ = 15 pF, $R_L$ = 400 Ω | | | N/A | | 23 | 38 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 27 | 43 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 12 | 18 | ns |
| | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 30 | 40 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 13.5 | 21 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | N/A | | 23 | 30 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 18 | 30 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 12 | 18 | ns |
| | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 24 | 36 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 14 | 21 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Select (3 levels) | W | | | 21 | 35 | | 16 | 26 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 14 | 23 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 10 | 15 | ns |
| | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 17 | 25 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 11.5 | 18 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 22 | 33 | | 16 | 30 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 20 | 32 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 9 | 13.5 | ns |
| | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 26 | 40 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 11 | 17 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Strobe | Y | | | | N/A | | 25 | 33 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 26 | 42 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 11 | 16.5 | ns |
| | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 29 | 44 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 12.5 | 19 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | N/A | | 19 | 30 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 20 | 32 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 12 | 18 | ns |
| | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 26 | 40 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 14 | 21 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Strobe | W | | | 15.5 | 24 | | 11 | 21 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 15 | 24 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 9 | 13 | ns |
| | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 18 | 27 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 10.5 | 16 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 21 | 30 | | 17 | 25 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 18 | 30 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 8.5 | 12 | ns |
| | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 24 | 36 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 10.5 | 16 | |

## Switching Characteristics (Continued)

| Parameter | | From (Input) | To (Output) | DM54/74 Conditions | DM54/74 150 Min | DM54/74 150 Typ | DM54/74 150 Max | DM54/74 151A Min | DM54/74 151A Typ | DM54/74 151A Max | DM54/74 LS151 Conditions | DM54/74 LS151 Min | DM54/74 LS151 Typ | DM54/74 LS151 Max | DM54/74 S151 Conditions | DM54/74 S151 Min | DM54/74 S151 Typ | DM54/74 S151 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | D0 thru D7 | Y | $C_L$ = 15 pF, $R_L$ = 400 Ω | | | N/A | | 17 | 24 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 20 | 32 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 8 | 12 | ns |
| | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 23 | 35 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 9.5 | 15 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | N/A | | 18 | 24 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 16 | 26 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 8 | 12 | ns |
| | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 22 | 33 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 10 | 15 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | E0 thru E15 or D0 thru D7 | W | | | 13 | 20 | | 10 | 14 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 13 | 21 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 4.5 | 7 | ns |
| | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 16 | 25 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 6 | 9 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 8.5 | 14 | | 8 | 14 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 12 | 20 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 4.5 | 7 | ns |
| | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 18 | 27 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 6.5 | 10 | |

# Dual 4-Line to 1-Line Data Selectors/Multiplexers

## General Description

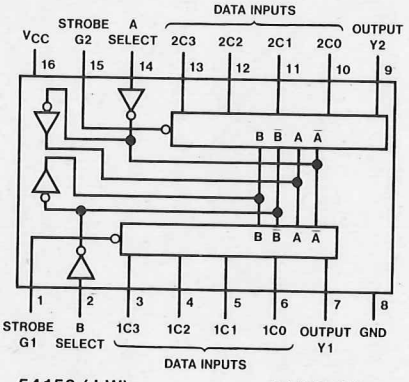
Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

## Features

- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low-impedance, totem-pole outputs

| Type | Typical Average Propagation Delay Times From Data | From Strobe | From Select | Typical Power Dissipation |
|---|---|---|---|---|
| 153 | 11 ns | 18 ns | 20 ns | 170 mW |
| LS153 | 14 ns | 19 ns | 22 ns | 31 mW |
| S153 | 6 ns | 9.5 ns | 12 ns | 225 mW |

## Connection Diagram




54153 (J,W)
54LS153 (J,W)
54S153 (J,W)

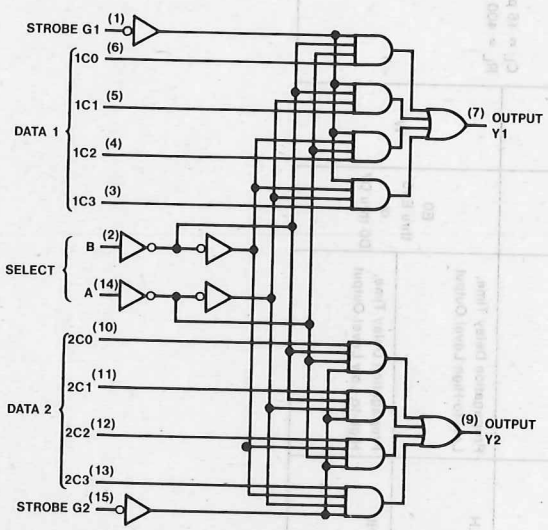
74153 (N)
74LS153 (N)
74S153 (N)

## Truth Table

| Select Inputs | | Data Inputs | | | | Strobe | Output |
|---|---|---|---|---|---|---|---|
| B | A | C0 | C1 | C2 | C3 | G | Y |
| X | X | X | X | X | X | H | L |
| L | L | L | X | X | X | L | L |
| L | L | H | X | X | X | L | H |
| L | H | X | L | X | X | L | L |
| L | H | X | H | X | X | L | H |
| H | L | X | X | L | X | L | L |
| H | L | X | X | H | X | L | H |
| H | H | X | X | X | L | L | L |
| H | H | X | X | X | H | L | H |

Select inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 153 | | | DM54/74 LS153 | | | DM54/74 S153 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | | | | | V |
| | | | $I_I$ = −18 mA | | | | | | | −1.5 | | | −1.2 | |
| $I_{OH}$ | High Level Output Current | | | | | | −800 | | | −400 | | | −1000 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.4 | 3.2 | | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.4 | 3.2 | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | | | 4 | | | 20 | mA |
| | | | | DM74 | | | 16 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | DM74 | | 0.2 | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 4 mA | DM74LS | | | | | 0.25 | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | | | | 1 | mA |
| | | | $V_I$ = 7 V | | | | | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | | | | | uA |
| | | | $V_I$ = 2.7 V | | | | | | | 20 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.4 V | | | | −1.6 | | | −0.36 | | | | mA |
| | | | $V_I$ = 0.5 V | | | | | | | | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −20 | | −55 | −20 | | −100 | −40 | | −100 | mA |
| | | | | DM74 | −18 | | −57 | −20 | | −100 | −40 | | −100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | DM54 | | 34 | 52 | | 6.2 | 10 | | 45 | 70 | mA |
| | | | | DM74 | | 34 | 60 | | 6.2 | 10 | | 45 | 70 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS or DM54S/74S duration of short circuit should not exceed one second.

**Note 3:** $I_{CCL}$ is measured with the outputs open and all inputs grounded.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | DM54/74 153 | | | | DM54/74 LS153 | | | | DM54/74 S153 | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Y | $C_L$ = 30 pF, $R_L$ = 400 Ω | | 11 | 18 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 10 | 15 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 6 | 9 | ns |
| | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 13 | 20 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 7.5 | 12 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Data | Y | | | 10 | 23 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 17 | 26 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 6 | 9 | ns |
| | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 23 | 35 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 8 | 12 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Select | Y | | | 20 | 34 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 19 | 29 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 11.5 | 18 | ns |
| | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 22 | 35 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 13 | 20 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Select | Y | | | 20 | 34 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 25 | 38 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 12 | 18 | ns |
| | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 31 | 45 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 14 | 21 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Strobe | Y | | | 19 | 30 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 16 | 24 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 10 | 15 | ns |
| | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 19 | 30 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 15 | 18 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Strobe | Y | | | 17 | 23 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 21 | 32 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 9 | 13.5 | ns |
| | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 27 | 40 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 11 | 17 | |

# 4-Line to 16-Line Decoders/Demultiplexers

## General Description

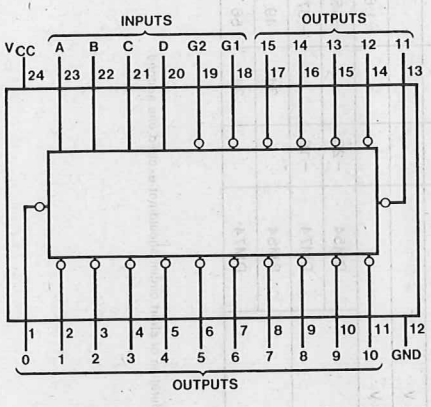
Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

## Features

- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs

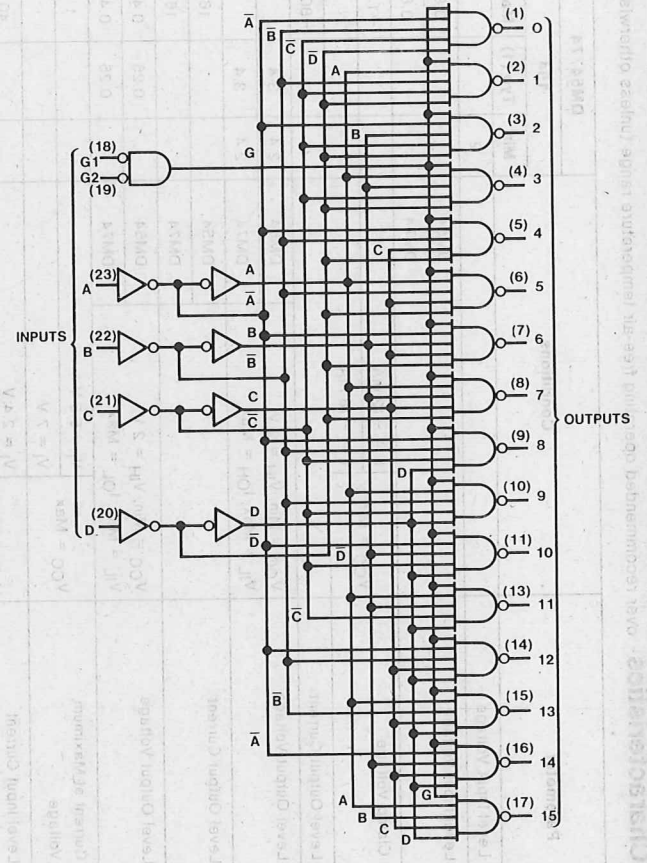
| Type | Typical Propagation Delay | | Typical Power Dissipation |
|---|---|---|---|
| | 3 Levels of Logic | Strobe | |
| 154 | 19 ns | 18 ns | 170 mW |
| L154A | 55 ns | 45 ns | 24 mW |
| LS154 | 23 ns | 19 ns | 45 mW |

## Connection and Logic Diagrams




**54154 (J,F)**
**54L154A (J,F)**
**54LS154 (J,F)**

**74154 (N)**
**74L154A (N)**
**74LS154 (N)**



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 154 | | | DM54/74 L154A | | | DM54/74 LS154 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.7 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.7 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | N/A | | | | V |
| | | | $I_I$ = −18 mA | | | | | | | | | | −1.5 | |
| $I_{OH}$ | High Level Output Current | | | | | | −800 | | | −200 | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.4 | 3.4 | | 2.4 | 2.8 | | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.4 | 3.4 | | 2.4 | 2.8 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | | | 2 | | | 4 | mA |
| | | | | DM74 | | | 16 | | | 3.6 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = Max, $I_{OL}$ = Max | | DM54 | | 0.25 | 0.4 | | 0.15 | 0.3 | | 0.25 | 0.4 | V |
| | | | | DM74 | | 0.25 | 0.4 | | 0.20 | 0.4 | | 0.35 | 0.5 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | 0.1 | | | | mA |
| | | | $V_I$ = 7 V | | | | | | | | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | 10 | | | | μA |
| | | | $V_I$ = 2.7 V | | | | | | | | | | 20 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | | | −0.18 | | | | mA |
| | | | $V_I$ = 0.4 V | | | | −1.6 | | | | | | −0.4 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −20 | | −55 | −3 | −9 | −15 | −20 | | −100 | mA |
| | | | | DM74 | −18 | | −57 | −3 | −9 | −15 | −20 | | −100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | DM54 | | 34 | 49 | | 4.8 | 6.0 | | 9 | 14 | mA |
| | | | | DM74 | | 34 | 56 | | 4.8 | 6.0 | | 9 | 14 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

**Note 3:** $I_{CC}$ is measured with all inputs grounded and all outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| | Parameter | Conditions | DM54/74 154 Min | DM54/74 154 Typ | DM54/74 154 Max | Conditions | DM54/74 L154A Min | DM54/74 L154A Typ | DM54/74 L154A Max | Conditions | DM54/74 LS154 Min | DM54/74 LS154 Typ | DM54/74 LS154 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output, From A, B, C, or D Inputs Through 3 Levels of Logic | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 18 | 36 | $C_L$ = 50 pF, $R_L$ = 4 kΩ | | 35 | 70 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 18 | 30 | ns |
| | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 22 | 35 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output, From A, B, C, or D Inputs Through 3 Levels of Logic | | | 21 | 33 | | | 75 | 150 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 18 | 30 | ns |
| | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 24 | 35 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output, From Either Strobe Input | | | 17 | 30 | | | 35 | 70 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 12 | 20 | ns |
| | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 15 | 25 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output, From Either Strobe Input | | | 18 | 27 | | | 55 | 110 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 16 | 25 | ns |
| | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 23 | 35 | |

## Truth Table

| Inputs | | | | | | Outputs | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| G1 | G2 | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | L | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H |
| L | L | H | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H |
| L | L | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H |
| L | L | H | H | L | L | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H |
| L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H |
| L | L | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | L | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

H = High Level, L = Low Level, X = Don't Care

# Dual 2-Line to 4-Line Decoders/Demultiplexers

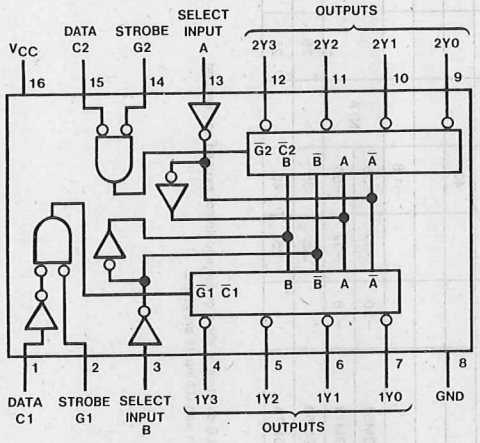
## General Description

These TTL circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied at C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8-line decoder, or 1-to-8-line demuliplexer, without external gating. Input clamping diodes are provided on these circuits to minimize transmission-line effects and simplify system design.

## Features

- Applications:
  - Dual 2-to-4-line decoder
  - Dual 1-to-4-line demultiplexer
  - 3-to-8-line decoder
  - 1-to-8-line demultiplexer
- Individual strobes simplify cascading for decoding or demultiplexing larger words
- Input clamping diodes simplify system design
- Choice of outputs:
  - Totem-pole (155, LS155)
  - Open-collector (156, LS156)

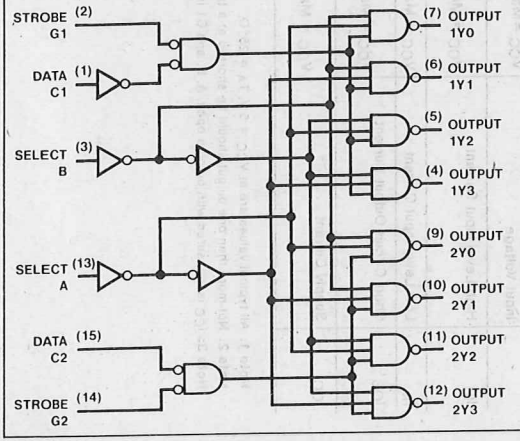
## Connection Diagram




54155 (J,W)
54LS155 (J,W)
54156 (J,W)
54LS156 (J,W)

74155 (N)
74LS155 (N)
74156 (N)
74LS156 (N)

## Logic Diagram




## Truth Tables

**2-Line-to-4-Line Decoder or 1-Line-to-4-Line Demultiplexer**

| Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| Select | | Strobe | Data | | | | |
| B | A | G1 | C1 | 1Y0 | 1Y1 | 1Y2 | 1Y3 |
| X | X | H | X | H | H | H | H |
| L | L | L | H | L | H | H | H |
| L | H | L | H | H | L | H | H |
| H | L | L | H | H | H | L | H |
| H | H | L | H | H | H | H | L |
| X | X | X | L | H | H | H | H |

| Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| Select | | Strobe | Data | | | | |
| B | A | G2 | C2 | 2Y0 | 2Y1 | 2Y2 | 2Y3 |
| X | X | H | X | H | H | H | H |
| L | L | L | L | L | H | H | H |
| L | H | L | L | H | L | H | H |
| H | L | L | L | H | H | L | H |
| H | H | L | L | H | H | H | L |
| X | X | X | H | H | H | H | H |

**3-Line-to-8-Line Decoder or 1-Line-to-8-Line Demultiplexer**

| Inputs | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Select | | | Strobe Or Data | (0) | (1) | (2) | (3) | (4) | (5) | (6) | (7) |
| C† | B | A | G‡ | 2Y0 | 2Y1 | 2Y2 | 2Y3 | 1Y0 | 1Y1 | 1Y2 | 1Y3 |
| X | X | X | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | H | H | H | H |
| L | H | L | L | H | H | L | H | H | H | H | H |
| L | H | H | L | H | H | H | L | H | H | H | H |
| H | L | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | L | H | H |
| H | H | L | L | H | H | H | H | H | H | L | H |
| H | H | H | L | H | H | H | H | H | H | H | L |

†C = inputs C1 and C2 connected together
‡G = inputs G1 and G2 connected together
H = high level, L = low level, X = don't care

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM54/74 155 Min | DM54/74 155 Typ (1) | DM54/74 155 Max | DM54/74 156 Min | DM54/74 156 Typ (1) | DM54/74 156 Max | DM54/74 LS155 Min | DM54/74 LS155 Typ (1) | DM54/74 LS155 Max | DM54/74 LS156 Min | DM54/74 LS156 Typ (1) | DM54/74 LS156 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | DM54 | | | 0.8 | | | 0.8 | | | 0.8 | | | 0.8 | V |
| | | | DM74 | | | 0.8 | | | 0.8 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | | | | | | | V |
| | | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | | | | | | | −1.5 | | | −1.5 | |
| $I_{CEX}$ | High Level Output Current | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $V_{OH}$ = 5.5 V | | | | | | | 250 | | | | | | 100 | μA |
| $I_{OH}$ | High Level Output Current | | | | | −800 | | | | | | −400 | | | | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | DM54 | 2.4 | | | | | | 2.5 | 3.4 | | | | | V |
| | | | DM74 | 2.4 | | | | | | 2.7 | 3.4 | | | | | |
| $I_{OL}$ | Low Level Output Current | | DM54 | | | 16 | | | 16 | | | 4 | | | 4 | mA |
| | | | DM74 | | | 16 | | | 16 | | | 8 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $I_{OL}$ = 4 mA | | | | | | | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 8 mA DM74 | | | | | | | | 0.35 | 0.5 | | 0.35 | 0.5 | |
| | | | $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | | | | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | 1 | | | 1 | | | | | | | mA |
| | | | $V_I$ = 7 V | | | | | | | | | 0.1 | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | 40 | | | 40 | | | | | | | μA |
| | | | $V_I$ = 2.7 V | | | | | | | | | 20 | | | 20 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −1.6 | | | −1.6 | | | −0.36 | | | −0.36 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | DM54 | −20 | −32 | −55 | N/A | | N/A | −20 | | −100 | N/A | | N/A | mA |
| | | | DM74 | −18 | −32 | −55 | | | | −20 | | −100 | | | | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | DM54 | | 25 | 35 | | 25 | 35 | | 6.1 | 10 | | 6.1 | 10 | mA |
| | | | DM74 | | 25 | 40 | | 25 | 40 | | 6.1 | 10 | | 6.1 | 10 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

**Note 3:** $I_{CC}$ is measured with outputs open, A, B, and C1 inputs at 4.5 V, and C2, G1 and G2 inputs grounded.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Levels of Logic | DM54/74 Conditions | DM54/74 155 Min | DM54/74 155 Typ | DM54/74 155 Max | DM54/74 156 Min | DM54/74 156 Typ | DM54/74 156 Max | DM54/74 Conditions | DM54/74 LS155 Min | DM54/74 LS155 Typ | DM54/74 LS155 Max | DM54/74 LS156 Min | DM54/74 LS156 Typ | DM54/74 LS156 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A, B, C2 G1 or G2 | Y | 2 | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 13 | 20 | | 15 | 23 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 12 | 18 | | 17 | 28 | ns |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 15 | 22 | | 20 | 32 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | A, B, C2 G1 or G2 | Y | 2 | | | 18 | 27 | | 19 | 30 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 17 | 27 | | 18 | 33 | ns |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 23 | 35 | | 24 | 39 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A or B | Y | 3 | | | 18 | 27 | | 21 | 32 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 12 | 18 | | 17 | 28 | ns |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 15 | 24 | | 20 | 32 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | A or B | Y | 3 | | | 17 | 26 | | 18 | 27 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 17 | 27 | | 19 | 33 | ns |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 23 | 35 | | 25 | 40 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | C1 | Y | 3 | | | 17 | 24 | | 19 | 27 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 13 | 20 | | 18 | 28 | ns |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 16 | 24 | | 21 | 32 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | C1 | Y | 3 | | | 17 | 26 | | 18 | 27 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 17 | 27 | | 19 | 34 | ns |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 23 | 35 | | 25 | 40 | |

# Quad 2-Line to 1-Line Data Selectors/Multiplexers

## General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The 157, L157A, LS157, and S157 present true data whereas the LS158 and S158 present inverted data to minimize propagation delay time.

## Applications

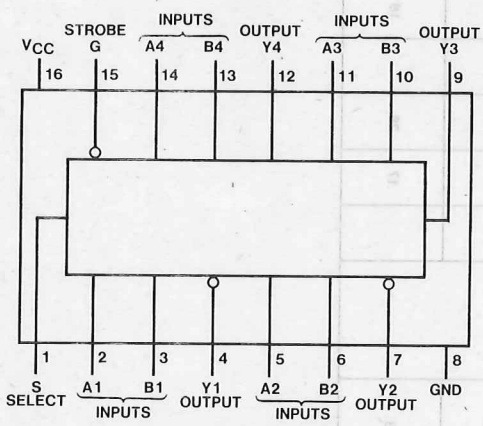
- Expand any data input point
- Multiplex dual data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

## Features

- Buffered inputs and outputs
- Three speed/power ranges available

| Type | Typical Propagation Time | Typical Power Dissipation |
|---|---|---|
| 157 | 9 ns | 150 mW |
| L157A | 40 ns | 15 mW |
| LS157 | 9 ns | 49 mW |
| S157 | 5 ns | 250 mW |
| LS158 | 7 ns | 24 mW |
| S158 | 4 ns | 195 mW |

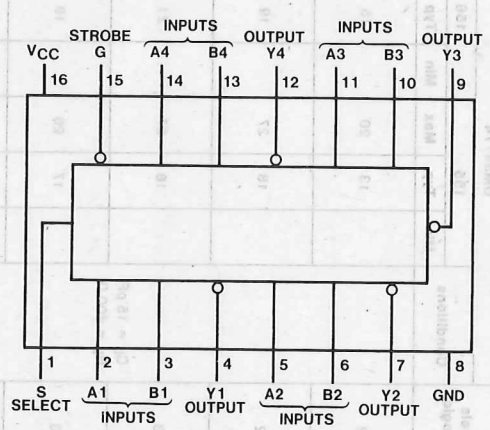
## Connection Diagrams




Low level at S selects A inputs
High level at S selects B inputs

**54157 (J,W)**
**54L157A (J,W)**
**54LS157 (J)**
**54S157 (J,W)**

**74157 (N)**
**74L157A (N)**
**74LS157 (N)**
**74S157 (N)**




Low level at S selects A inputs
High level at S selects B inputs

**54LS158 (J,W)**
**54S158 (J,W)**

**74LS158 (N)**
**74S158 (N)**

## Truth Table

| Inputs | | | | Output Y | |
|---|---|---|---|---|---|
| Strobe | Select | A | B | 157, L157A LS157, S157 | LS158 S158 |
| H | X | X | X | L | H |
| L | L | L | X | L | H |
| L | L | H | X | H | L |
| L | H | X | L | L | H |
| L | H | X | H | H | L |

H = High Level, L = Low Level, X = Don't Care

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM54/74 157 | | | DM54/74 L157A | | | DM54/74 LS157, LS158 | | | DM54/74 S157, S158 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | DM54 | | | 0.8 | | | 0.7 | | | 0.8 | | | 0.8 | V |
| | | | | | DM74 | | | 0.8 | | | 0.7 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | N/A | | | | | | | V |
| | | | | $I_I$ = −18 mA | | | | | | | N/A | | | −1.5 | | | −1.2 | |
| $I_{OH}$ | High Level Output Current | | | | | | | −800 | | | −200 | | | −400 | | | −1000 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.4 | 3.4 | | 2.4 | | | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | | DM74 | 2.4 | 3.4 | | 2.4 | | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 16 | | | 2 | | | 4 | | | 20 | mA |
| | | | | | DM74 | | | 16 | | | 3.6 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min<br>$V_{IH}$ = 2 V<br>$V_{IL}$ = Max | $I_{OL}$ = 4 mA | DM74 | | | | | | | | 0.25 | 0.4 | | | | V |
| | | | | $I_{OL}$ = Max | DM54 | | | 0.4 | | | 0.3 | | 0.25 | 0.4 | | | 0.5 | |
| | | | | | DM74 | | | 0.4 | | | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| $I_I$ | Input Current at Maximum Input Voltage | Any Input | $V_{CC}$ = Max | | $V_I$ = 5.5 V | | | 1 | | | 0.1 | | | | | | 1 | mA |
| | | S or G Input | | | $V_I$ = 7 V | | | | | | | | | 0.2 | | | | |
| | | A or B Input | | | | | | | | | | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | Any Input | $V_{CC}$ = Max | | $V_I$ = 2.4 V | | | 40 | | | 10 | | | | | | | μA |
| | | S or G Input | | | $V_I$ = 2.7 V | | | | | | | | | 40 | | | 50 | |
| | | A or B Input | | | | | | | | | | | | 20 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | Any Input | $V_{CC}$ = Max | | $V_I$ = 0.3 V | | | | | | −0.18 | | | | | | | mA |
| | | S or G Input | | | $V_I$ = 0.4 V | | | −1.6 | | | | | | −0.8 | | | | |
| | | A or B Input | | | | | | −1.6 | | | | | | −0.4 | | | | |
| | | Any Input | | | $V_I$ = 0.5 V | | | | | | | | | | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | DM54 | −20 | | −55 | −3 | −9 | −15 | −20 | | −100 | −40 | | −100 | mA |
| | | | | | DM74 | −18 | | −55 | −3 | −9 | −15 | −20 | | −100 | −40 | | −100 | |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (3) | | 157 | | 30 | 48 | | 3 | 4 | | 9.7 | 16 | | 50 | 78 | mA |
| | | | | | 158 | | | N/A | | | N/A | | 4.8 | 8 | | 39 | 61 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for the DM54LS/74LS or DM54S/74S duration of the short circuit should not exceed one second.

**Note 3:** $I_{CC}$ is measured with 4.5 V applied to all inputs and all outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

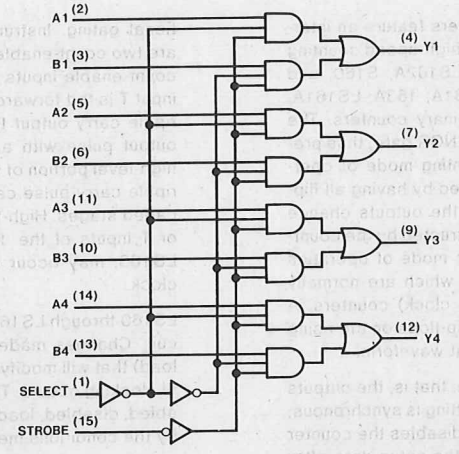
| Parameter | | | From (Input) | To (Output) | DM54/74 157 | | | | DM54/74 L157A | | | | DM54/74 LS157, LS158 | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | 157 | Data | Y | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 8 | 14 | $C_L$ = 50 pF, $R_L$ = 4 kΩ | | 40 | 80 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 9 | 14 | ns |
| | | 158 | | | | | | N/A | | | | N/A | | | 9 | 12 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | 157 | | | | | 10 | 14 | | | 40 | 80 | | | 9 | 14 | ns |
| | | 158 | | | | | | N/A | | | | N/A | | | 8 | 12 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | 157 | Strobe | Y | | | 13 | 20 | | | 60 | 120 | | | 13 | 20 | ns |
| | | 158 | | | | | | N/A | | | | N/A | | | 12 | 17 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | 157 | | | | | 14 | 21 | | | 60 | 120 | | | 14 | 21 | ns |
| | | 158 | | | | | | N/A | | | | N/A | | | 13 | 18 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | 157 | Select | Y | | | 15 | 23 | | | 70 | 140 | | | 16 | 23 | ns |
| | | 158 | | | | | | N/A | | | | N/A | | | 13 | 20 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | 157 | | | | | 17 | 27 | | | 50 | 100 | | | 15 | 27 | ns |
| | | 158 | | | | | | N/A | | | | N/A | | | 18 | 24 | |

## Switching Characteristics (Continued)

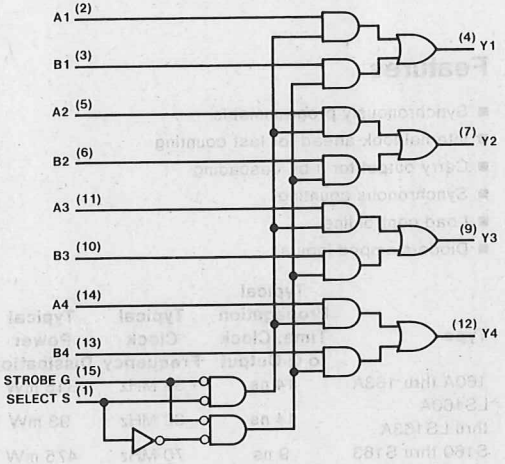
| Parameter | | | From (Input) | To (Output) | DM54/74 LS157, LS158 | | | | DM54/74 S157, S158 | | | | DM54/74 S157, S158 | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | 157 | Data | Y | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 12 | 18 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 6.5 | 10 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 5 | 7.5 | ns |
| | | 158 | | | | | 12 | 18 | | | 5.5 | 9 | | | 4 | 6 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | 157 | | | | | 15 | 23 | | | 6.5 | 10 | | | 4.5 | 6.5 | ns |
| | | 158 | | | | | 14 | 21 | | | 6 | 9 | | | 4 | 6 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | 157 | Strobe | Y | | | 16 | 24 | | | 10 | 15 | | | 8.5 | 12.5 | ns |
| | | 158 | | | | | 15 | 23 | | | 8 | 12 | | | 6.5 | 11.5 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | 157 | | | | | 20 | 30 | | | 9.5 | 15 | | | 7.5 | 12 | ns |
| | | 158 | | | | | 19 | 28 | | | 9 | 14 | | | 7 | 12 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | 157 | Select | Y | | | 19 | 28 | | | 11 | 17 | | | 9.5 | 15 | ns |
| | | 158 | | | | | 16 | 24 | | | 9.5 | 15 | | | 8 | 12 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | 157 | | | | | 21 | 32 | | | 11.5 | 17 | | | 9.5 | 15 | ns |
| | | 158 | | | | | 24 | 36 | | | 10 | 15 | | | 8 | 12 | |

## Logic Diagrams

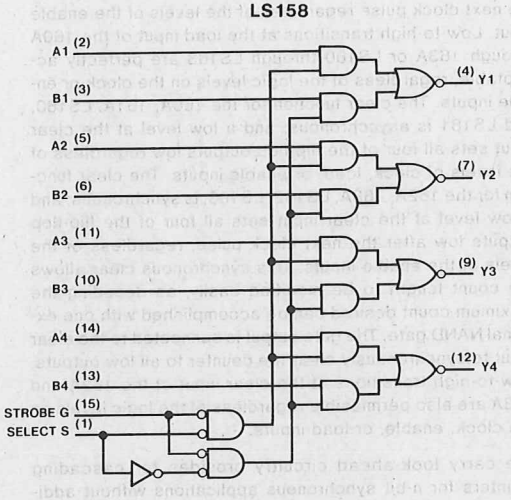
157, L157A



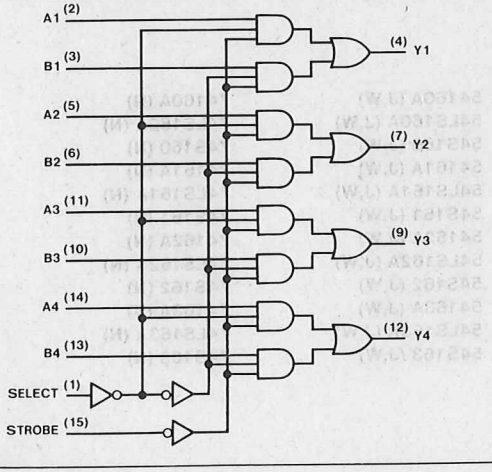

LS157



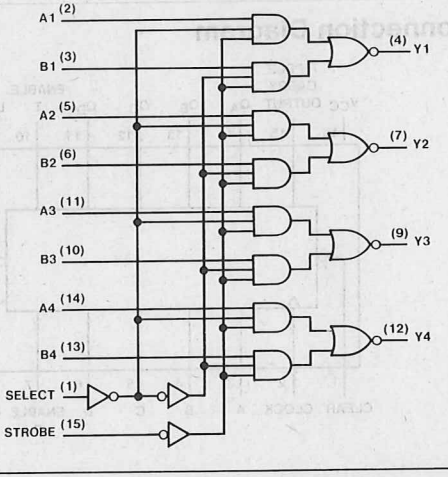

LS158




S157




S158




6

## Synchronous 4-Bit Counters

## General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 160A, 162A, LS160A, LS162A, S160, and S162 are decade counters and the 161A, 163A, LS161A, LS163A, S161, and S163 are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input. Low-to-high transitions at the load input of the 160A through 163A or LS160 through LS163 are perfectly acceptable, regardless of the logic levels on the clock or enable inputs. The clear function for the 160A, 161A, LS160, and LS161 is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the 162A, 163A, LS162, LS163, is synchronous; and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs. Low-to-high transitions at the clear input of the 162A and 163A are also permissible regardless of the logic levels on the clock, enable, or load inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the $Q_A$ output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the 160A through 163A or LS160 through LS163, may occur regardless of the logic level on the clock.

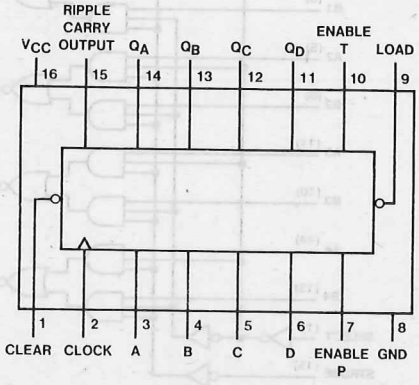
LS160 through LS163 feature a fully independent clock circuit. Changes made to control inputs (enable P or T, or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

## Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs

| Type | Typical Propagation Time, Clock to Q Output | Typical Clock Frequency | Typical Power Dissipation |
|---|---|---|---|
| 160A thru 163A | 14 ns | 35 MHz | 315 mW |
| LS160A thru LS163A | 14 ns | 32 MHz | 93 mW |
| S160 thru S163 | 9 ns | 70 MHz | 475 mW |

## Connection Diagram




| | |
|---|---|
| 54160A (J,W) | 74160A (N) |
| 54LS160A (J,W) | 74LS160A (N) |
| 54S160 (J,W) | 74S160 (N) |
| 54161A (J,W) | 74161A (N) |
| 54LS161A (J,W) | 74LS161A (N) |
| 54S161 (J,W) | 74S161 (N) |
| 54162A (J,W) | 74162A (N) |
| 54LS162A (J,W) | 74LS162A (N) |
| 54S162 (J,W) | 74S162 (N) |
| 54163A (J,W) | 74163A (N) |
| 54LS163A (J,W) | 74LS163A (N) |
| 54S163 (J,W) | 74S163 (N) |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM54/74 160A, 161A 162A, 163A | | | DM54/74 LS160A, LS161A LS162A, LS163A | | | DM54/74 S160, S161 S162, S163 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | DM54 | | | 0.8 | | | 0.8 | | | 0.8 | V |
| | | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | | | | | V |
| | | | | $I_I$ = −18 mA | | | | | | | −1.5 | | | −1.2 | |
| $I_{OH}$ | High Level Output Current | | | | | | | −800 | | | −400 | | | −1000 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.4 | 3.4 | | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | | DM74 | 2.4 | 3.4 | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 16 | | | 4 | | | 20 | mA |
| | | | | | DM74 | | | 16 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min<br>$V_{IH}$ = 2 V<br>$V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | | DM74 | | 0.2 | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| | | | | $I_{OL}$ = 4 mA | DM74 | | | | | 0.25 | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | All | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | | | | 1 | mA |
| | | Data or Enable P | | $V_I$ = 7 V | | | | | | | 0.1 | | | | |
| | | Load, Clock, or Enable T | | | | | | | | | 0.2 | | | | |
| | | Clear (LS160A, LS161A) | | | | | | | | | 0.1 | | | | |
| | | Clear (LS162A, LS163A) | | | | | | | | | 0.2 | | | | |

## Electrical Characteristics (Continued)

| Parameter | | | Conditions | | DM54/74 160A, 161A 162A, 163A | | | DM54/74 LS160A, LS161A LS162A, LS163A | | | DM54/74 S160, S161 S162, S163 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $I_{IH}$ | High Level Input Current | Load | $V_{CC}$ = Max<br>$V_I$ = 2.4 V (160A-163A)<br>$V_I$ = 2.7 V (LS160A-LS163A)<br>$V_I$ = 2.7 V (S160-S163) | | | | 40 | | | 40 | | | 50 | μA |
| | | Clock | | | | | 80 | | | 40 | | | 50 | |
| | | Enable T | | | | | 80 | | | 40 | | | 100 | |
| | | Data | | | | | 40 | | | 20 | | | 50 | |
| | | Enable P | | | | | 40 | | | 20 | | | 50 | |
| | | Clear (160, 161) | | | | | 40 | | | 20 | | | 50 | |
| | | Clear (162, 163) | | | | | 40 | | | 40 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | Data, Enable P | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −1.6 | | | −0.4 | | | −2 | mA |
| | | Clock | | | | | −3.2 | | | −0.8 | | | −2 | |
| | | Load | | | | | −1.6 | | | −0.8 | | | −2 | |
| | | Enable T | | | | | −3.2 | | | −0.8 | | | −4 | |
| | | Clear (160, 161) | | | | | −1.6 | | | −0.4 | | | −2 | |
| | | Clear (162, 163) | | | | | −1.6 | | | −0.8 | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | DM54 | −20 | | −57 | −20 | | −100 | −40 | | −100 | mA |
| | | | | DM74 | −18 | | −57 | −20 | | −100 | −40 | | −100 | |
| $I_{CCH}$ | Supply Current, All Outputs High | | $V_{CC}$ = Max (3) | DM54 | | 59 | 85 | | 18 | 31 | | | | mA |
| | | | | DM74 | | 59 | 94 | | 18 | 31 | | | | |
| $I_{CCL}$ | Supply Current, All Outputs Low | | $V_{CC}$ = Max (4) | DM54 | | 63 | 91 | | 19 | 32 | | | | mA |
| | | | | DM74 | | 63 | 101 | | 19 | 32 | | | | |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max | | | | | | | | | 95 | 160 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS and DM54S/74S, duration of short circuit should not exceed one second.

**Note 3:** $I_{CCH}$ is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

**Note 4:** $I_{CCL}$ is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | To (Output) | DM54/74 160A, 161A, 162A, 163A | | | | DM54/74 LS160A, LS161A, LS162A, LS163A | | | | DM54/74 LS160A, LS161A, LS162A, LS163A | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | | | $C_L$ = 15 pF, $R_L$ = 400 Ω | 25 | 35 | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 25 | 32 | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 20 | 25 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock | Ripple carry | | | 18 | 27 | | | 16 | 24 | | | 20 | 30 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clock | Ripple carry | | | 16 | 24 | | | 19 | 30 | | | 25 | 38 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock (Load Input High) | Any Q | | | 14 | 20 | | | 15 | 22 | | | 18 | 27 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clock (Load Input High) | Any Q | | | 16 | 23 | | | 19 | 27 | | | 25 | 38 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock (Load Input Low) | Any Q | | | 14 | 21 | | | 16 | 24 | | | 19 | 30 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clock (Load Input Low) | Any Q | | | 18 | 25 | | | 21 | 29 | | | 26 | 38 | ns |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | | Enable T | Ripple carry | | | 10 | 15 | | | 13 | 18 | | | 16 | 27 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Enable T | Ripple carry | | | 12 | 16 | | | 10 | 15 | | | 16 | 27 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clear (5) | Any Q | | | 24 | 36 | | | 25 | 35 | | | 31 | 45 | ns |
| $t_{W(CLOCK)}$ | Width of Clock Pulse | | | | | 25 | | | | 20 | 6 | | | 25 | | | ns |
| $t_{W(CLEAR)}$ | Width of Clear Pulse | | | | | 20 | | | | 20 | 9 | | | 25 | | | ns |
| $t_{SETUP}$ | Setup Time | Data Inputs A, B, C, D | | | | 20 | | | | 20 | 8 | | | 20 | | | ns |
| | | Enable P | | | | 20 | | | | 25 | 17 | | | 30 | | | |
| | | Load | | | | 25 | | | | 25 | 15 | | | 30 | | | |
| | | Clear (6) | | | | 20 | | | | 25 | | | | 30 | | | |
| $t_{HOLD}$ | Hold Time at Any Input | Data A, B, C, D | | | | 0 | | | | 0 | −3 | | | 5 | | | ns |
| | | Others | | | | 0 | | | | 0 | −3 | | | 25 | | | |
| $t_{RECOVERY}$ | Clear | | | | | | | | | 20 | | | | | | | ns |

**Note 5:** Propagation delay for clearing is measured from the clear input for the 160A, LS160A, 161A, LS161A, S160, and S161 or from the clock input transition for the 162A, LS162A, 163A, LS163A, S162, and S163.

**Note 6:** This applies only for 162, 163, LS162A, LS163A, S162, and S163 which have synchronous clear inputs.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

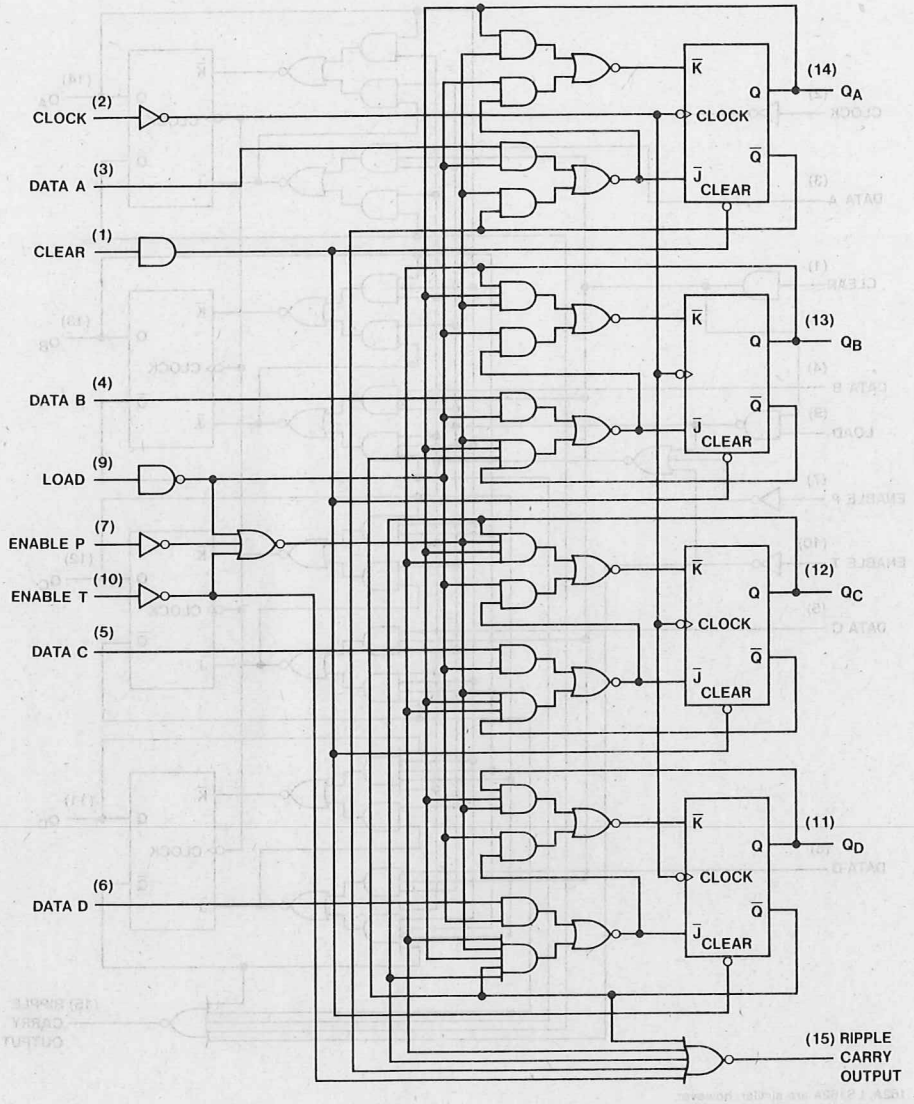
| Parameter | | | From (Input) | To (Output) | DM54/74 | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | S160, S161, S162, S163 | | | | S160–S163 | | | | |
| | | | | | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | | | $C_L$ = 15 pF, $R_L$ = 280 kΩ | 40 | 70 | | $C_L$ = 50 pF, $R_L$ = 280 Ω | 35 | 60 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock | Ripple carry | | | 14 | 25 | | | 16 | 25 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clock | Ripple carry | | | 17 | 25 | | | 19 | 28 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock (Load Input High) | Any Q | | | 8 | 15 | | | 10 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clock (Load Input High) | Any Q | | | 10 | 15 | | | 12 | 18 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock (Load Input Low) | Any Q | | | 8 | 15 | | | 10 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clock (Load Input Low) | Any Q | | | 10 | 15 | | | 12 | 18 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Enable T | Ripple carry | | | 10 | 15 | | | 12 | 18 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Enable T | Ripple carry | | | 10 | 15 | | | 12 | 18 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clear (5) | Any Q | | | 14 | 20 | | | 16 | 24 | ns |
| $t_{W(CLOCK)}$ | Width of Clock Pulse | | | | | 10 | | | | 12 | | | ns |
| $t_{W(CLEAR)}$ | Width of Clear Pulse | | | | | 10 | | | | 12 | | | ns |
| $t_{SETUP}$ | Setup Time | Data Inputs A, B, C, D | | | | 4 | | | | 5 | | | ns |
| | | Enable P | | | | 12 | | | | 14 | | | |
| | | Load | | | | 14 | | | | 16 | | | |
| | | Clear (6) | | | | 14 | | | | 16 | | | |
| $t_{HOLD}$ | Hold Time at Any Input | Data A, B, C, D | | | | 3 | | | | 5 | | | ns |
| | | Others | | | | 0 | | | | 2 | | | |
| $t_{RECOVERY}$ | Clear | | | | | 12 | | | | | | | ns |

**Note 5:** Propagation delay for clearing is measured from the clear input for the 160A, LS160A, 161A, LS161A, S160, and S161 or from the clock input transition for the 162A, LS162A, 163A, LS163A, S162, and S163.

**Note 6:** This applies only for 162, 163, LS162A, LS163A, S162, and S163 which have synchronous clear inputs.

## Logic Diagrams

160A, LS160A

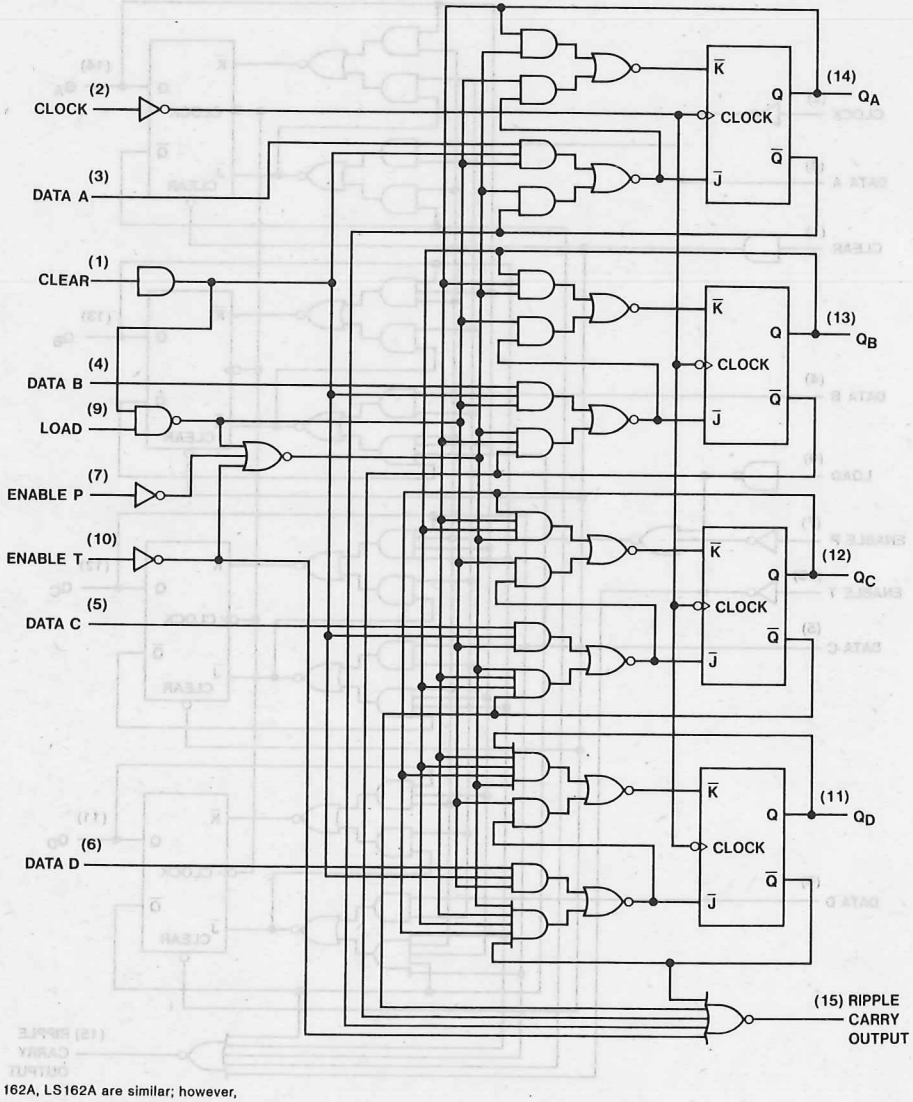



161A, LS161A are similiar; however, the clear is asynchronous as shown for 160A, LS160A decade counters.

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## Logic Diagrams (Continued)

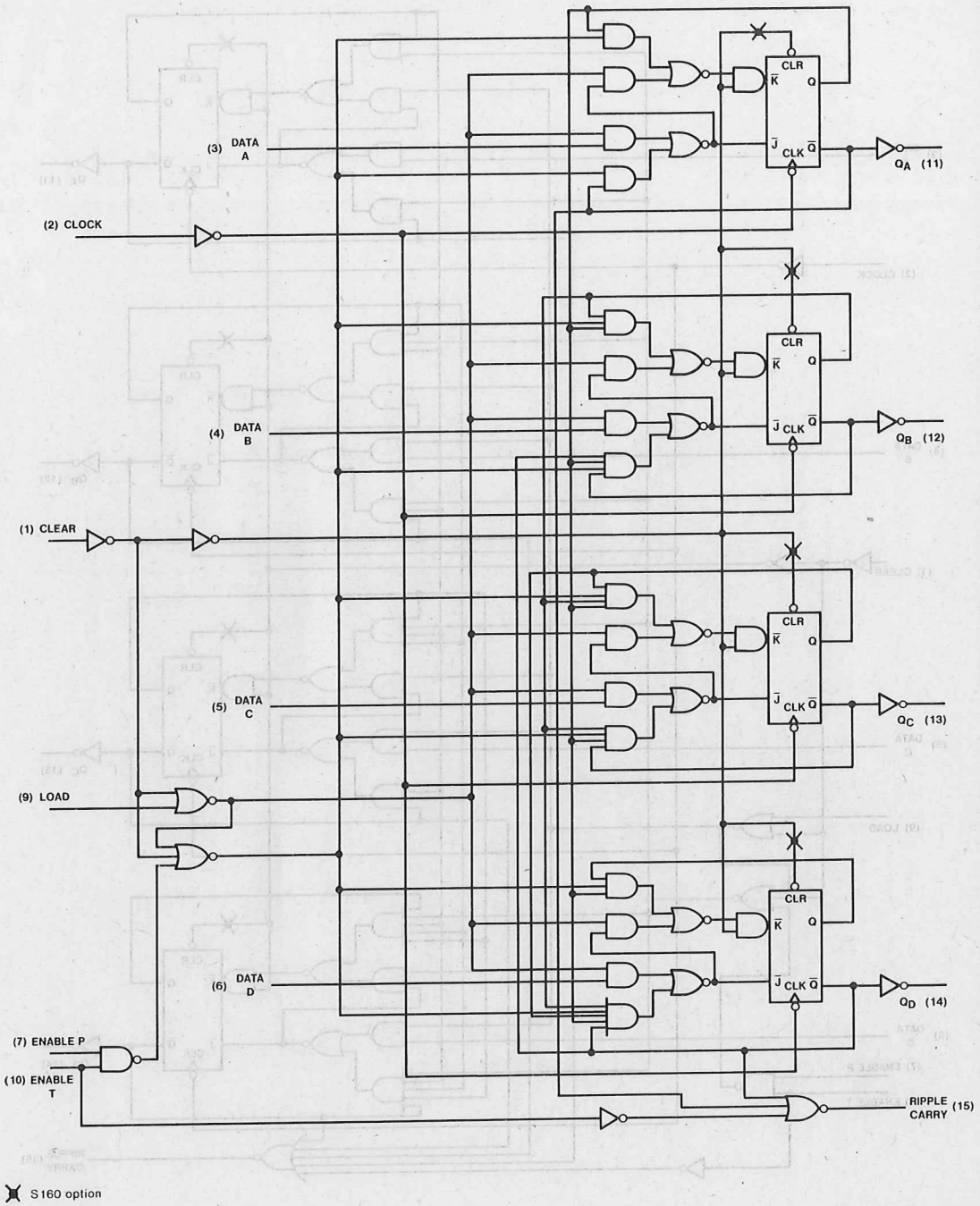
**163A, LS163A**




162A, LS162A are similar; however, the clear is synchronous as shown for the 163A, LS163A binary counters.

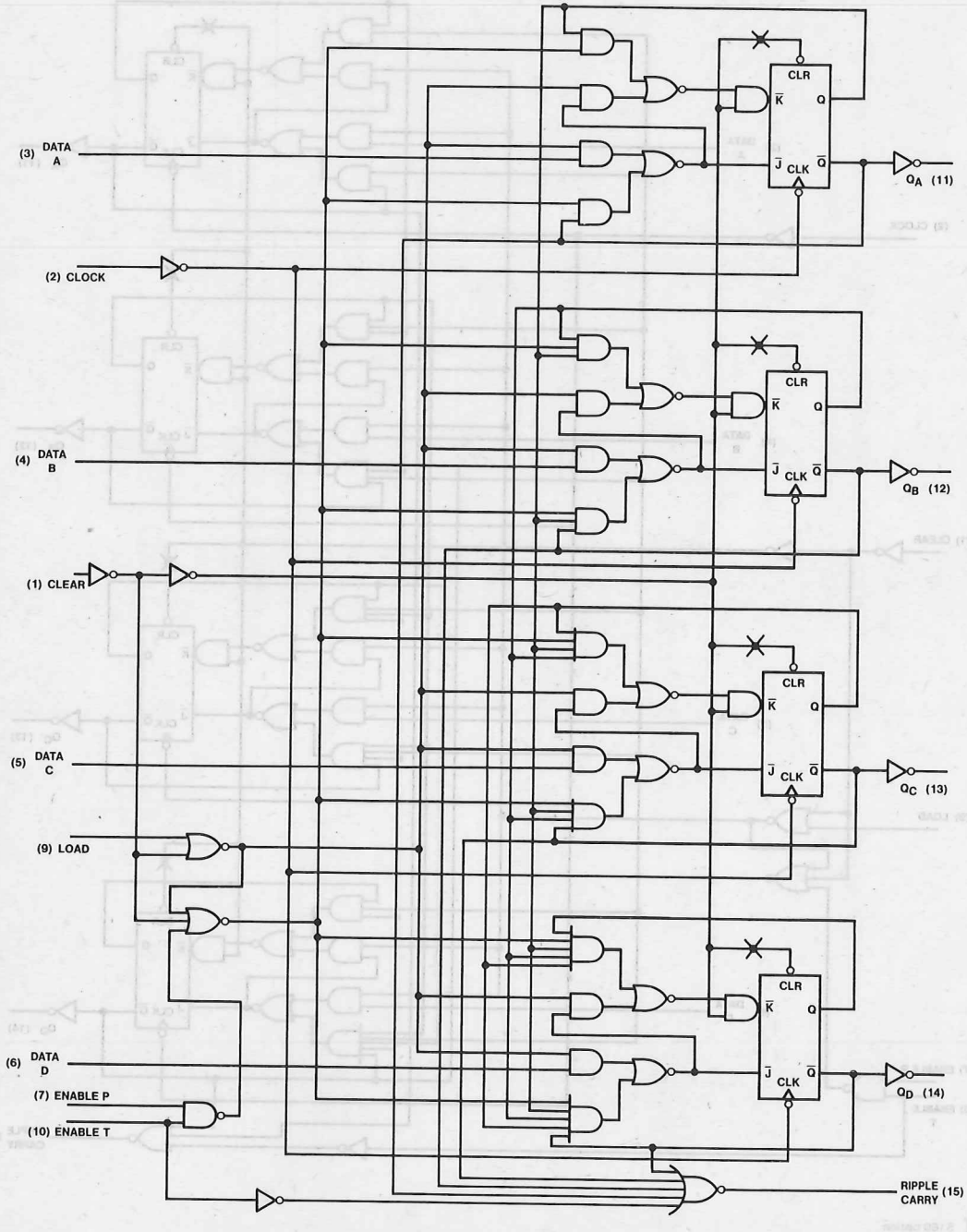
## Logic Diagrams (Continued)

S160, S162



## Logic Diagrams (Continued)

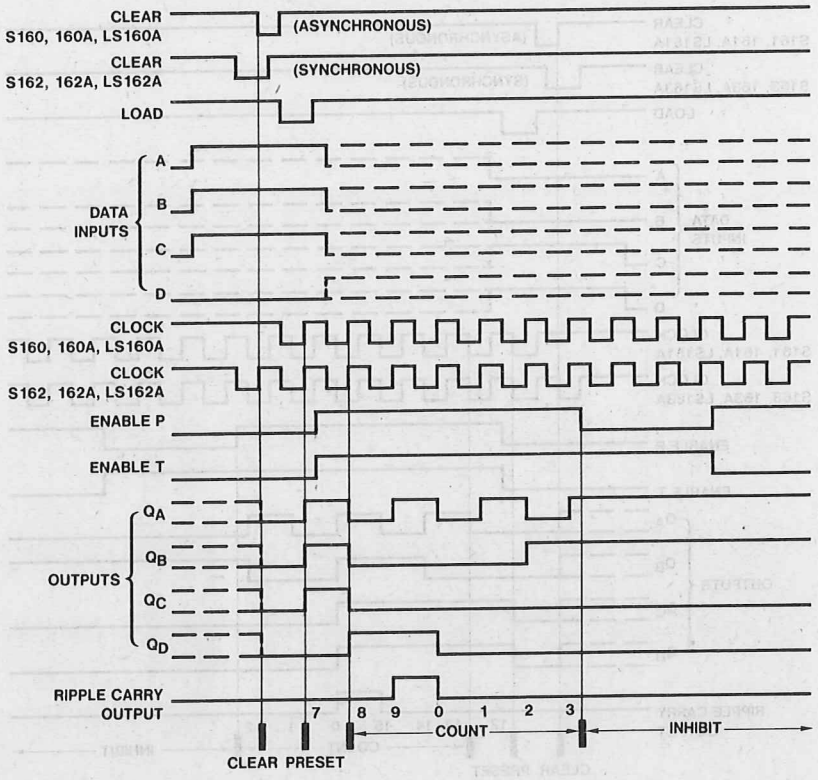
S161, S163




S161 option

## Timing Diagrams

160A, 162A, LS160A, LS162A, S160, S162 Synchronous Decade Counters
Typical Clear, Preset, Count and Inhibit Sequences

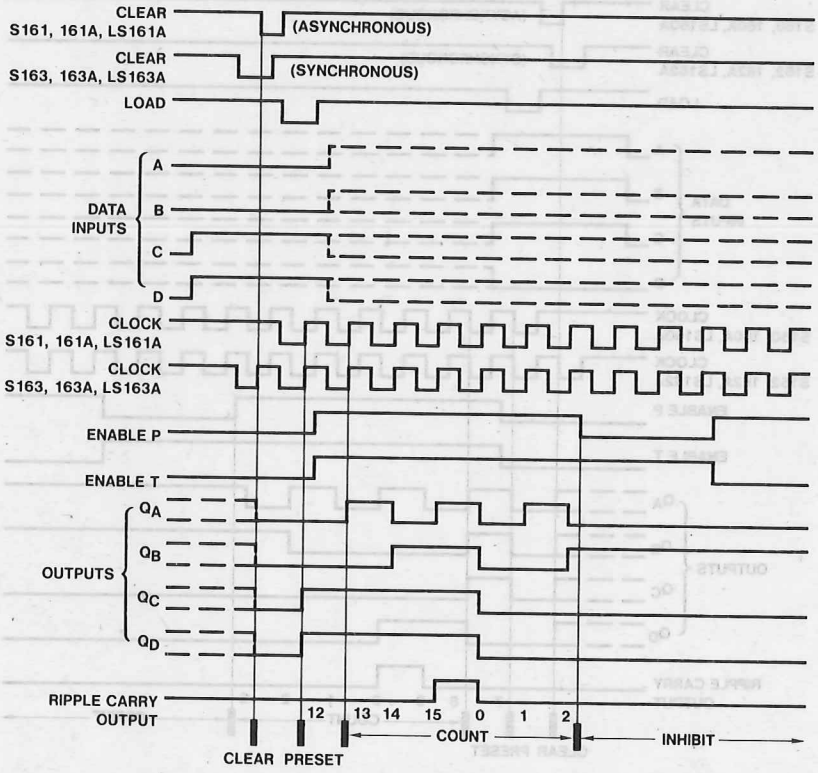



**Sequence:**

(1) Clear outputs to zero
(2) Preset to BCD seven
(3) Count to eight, nine, zero, one, two, and three
(4) Inhibit

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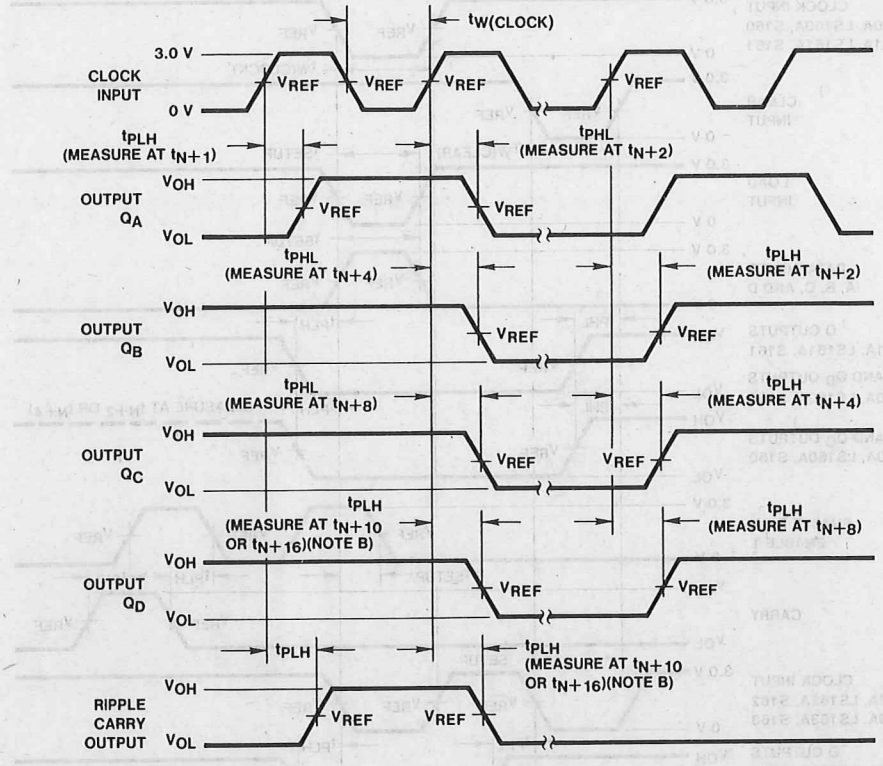
## 161A, 163A, LS161A, LS163A, S161, S163 Synchronous Binary Counters
### Typical Clear, Preset, Count and Inhibit Sequences




**Sequence:**
(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one and two
(4) Inhibit

## Parameter Measurement Information

### Switching Time Waveforms




**Note A:** The input pulses are supplied by a generator having the following characteristics: PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\,\Omega$. For 160A through 163A, $t_r \leq 10$ ns, $t_f \leq 10$ ns; for LS160A through LS163A, $t_r \leq 6$ ns, $t_f \leq 6$ ns; for S160 through S163, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure $f_{MAX}$.

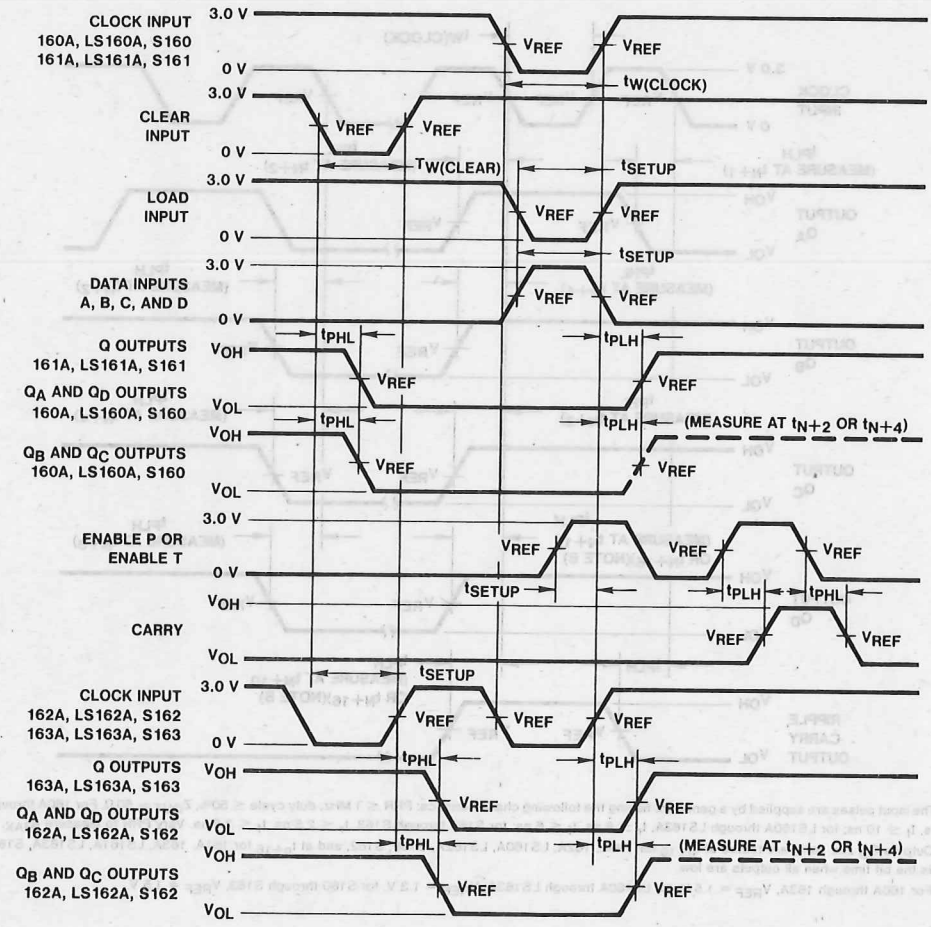
**Note B:** Outputs $Q_D$ and carry are tested at $t_{n+10}$ for 160A, 162A, LS160A, LS162A, S160, S162, and at $t_{n+16}$ for 161A, 163A, LS161A, LS163A, S161, S163, where $t_n$ is the bit time when all outputs are low.

**Note C:** For 160A through 163A, $V_{REF} = 1.5$ V; for LS160A through LS163A, $V_{REF} = 1.3$ V; for S160 through S163, $V_{REF} = 1.5$ V.

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## Parameter Measurement Information (Continued)

### Switching Time Waveforms




**Note A:** The input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\ \Omega$. For 160A through 163A, $t_r \leq 10$ ns, $t_f \leq 10$ ns; for LS160A through LS163A, $t_r \leq 6$ ns, $t_f \leq 6$ ns; for S160 through S163, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure $f_{MAX}$.

**Note B:** Enable P and enable T setup times are measured at $t_{n+0}$.

**Note C:** For 160A through 163A, $V_{REF} = 1.5$ V; for LS160A through LS163A, $V_{REF} = 1.3$ V; for S160 through S163, $V_{REF} = 1.5$ V.

# 8-Bit Serial In/Parallel Out Shift Registers

## General Description

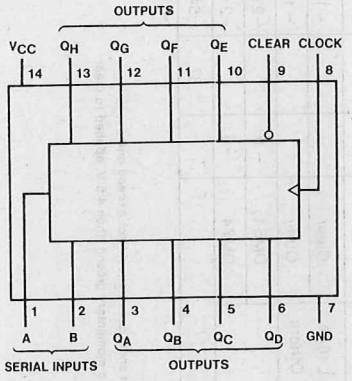
These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

## Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear

| Type | Typical Clock Frequency | Typical Power Dissipation |
|---|---|---|
| 164 | 36 MHz | 185 mW |
| L164A | 14 MHz | 30 mW |
| LS164 | 36 MHz | 80 mW |

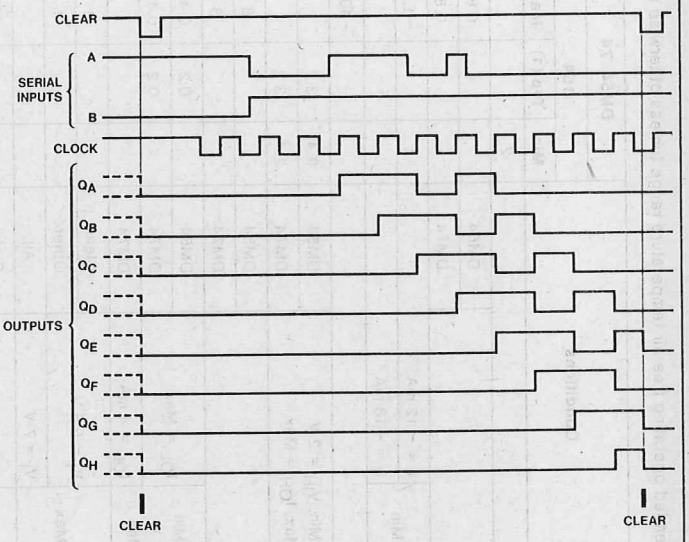
## Connection Diagram



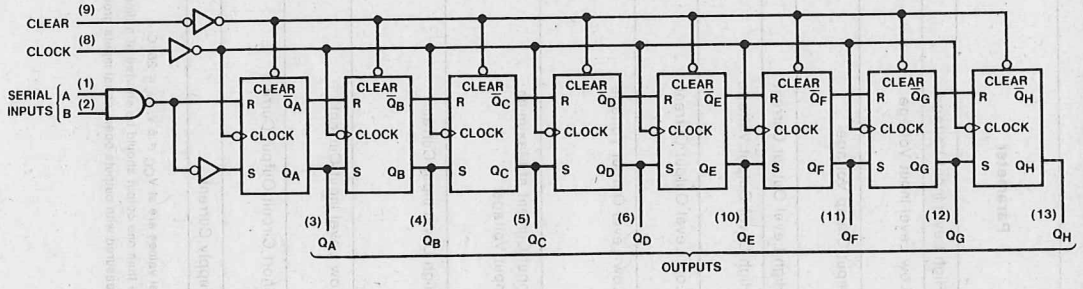

**54164 (J,W)**
**54L164A (J,W)**
**54LS164 (J,W)**

**74164 (N)**
**74L164A (N)**
**74LS164 (N)**

## Timing Diagram




## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 164 | | | DM54/74 L164A | | | DM54/74 LS164 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.7 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.7 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | N/A | | | | V |
| | | | $I_I$ = −18 mA | | | | | | | | | | −1.5 | |
| $I_{OH}$ | High Level Output Current | | | | | | −400 | | | −200 | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.4 | 3.2 | | 2.4 | | | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.4 | 3.2 | | 2.4 | | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 8 | | | 2 | | | 4 | mA |
| | | | | DM74 | | | 8 | | | 3.6 | | | 8 | |
| $V_{OH}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | | 0.3 | | 0.25 | 0.4 | V |
| | | | | DM74 | | 0.2 | 0.4 | | | 0.4 | | 0.35 | 0.5 | |
| | | | $I_{OL}$ = 4 mA | DM74 | | | | | | | | 0.25 | 0.4 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | Clear | | | 1 | | | 0.2 | | | | mA |
| | | | | Other | | | 1 | | | 0.1 | | | | |
| | | | $V_I$ = 7 V | All | | | | | | | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | Clear | | | 40 | | | 20 | | | | μA |
| | | | | Other | | | 40 | | | 10 | | | | |
| | | | $V_I$ = 2.7 V | All | | | | | | | | | 20 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.3 V, L164A; $V_I$ = 0.4 V, Others | Clear | | | −1.6 | | | −0.36 | | | −0.4 | mA |
| | | | | Other | | | −1.6 | | | −0.18 | | | −0.4 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −10 | | −27.5 | −3 | −9 | −15 | −20 | | −100 | mA |
| | | | | DM74 | −9 | | −27.5 | −3 | −9 | −15 | −20 | | −100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | | | 37 | 54 | | 6 | 9 | | 16 | 27 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

**Note 3:** $I_{CC}$ is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V, applied to clear.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | | DM54/74 164 | | | DM54/74 L164A | | | DM54/74 LS164 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | $R_L$ = 800 Ω for the 164<br>$R_L$ = 4 kΩ for the L164A<br>$R_L$ = 2 kΩ for the LS164 | $C_L$ = 15 pF | 25 | 36 | | 6 | 14 | | 25 | 36 | | MHz |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Outputs From Clear Input | | $C_L$ = 15 pF | | 24 | 36 | | | | | 24 | 36 | ns |
| | | | $C_L$ = 50 pF | | 28 | 42 | | 75 | 120 | | 30 | 45 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Outputs From Clock Input | | $C_L$ = 15 pF | 8 | 17 | 27 | | | | | 17 | 27 | ns |
| | | | $C_L$ = 50 pF | 10 | 20 | 30 | | 50 | 85 | | 20 | 30 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Outputs From Clock Input | | $C_L$ = 15 pF | 10 | 21 | 32 | | | | | 21 | 32 | ns |
| | | | $C_L$ = 50 pF | 10 | 25 | 37 | | 90 | 135 | | 28 | 40 | |
| $t_W$ | Width of Clock or Clear Input Pulse | | | 20 | | | 60 | 40 | | 20 | | | ns |
| $t_{SETUP}$ | Data Setup Time | | | 15 | | | 40 | 20 | | 15 | | | ns |
| $t_{HOLD}$ | Data Hold Time | | | 5 | | | 20 | −5 | | 5 | | | ns |
| $t_{RECOVERY}$ | Clear | | | | | | | | | 30 | | | ns |

## Truth Table

| Inputs | | | | Outputs | | |
|---|---|---|---|---|---|---|
| Clear | Clock | A | B | $Q_A$ | $Q_B$ | $Q_H$ |
| L | X | X | X | L | L | L |
| H | L | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |
| H | ↑ | H | H | H | $Q_{An}$ | $Q_{Gn}$ |
| H | ↑ | L | X | L | $Q_{An}$ | $Q_{Gn}$ |
| H | ↑ | X | L | L | $Q_{An}$ | $Q_{Gn}$ |

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

$Q_{A0}$, $Q_{B0}$, $Q_{H0}$ = The level of $Q_A$, $Q_B$, or $Q_H$, respectively, before the indicated steady-state input conditions were established.

$Q_{An}$, $Q_{Gn}$ = The level of $Q_A$ or $Q_G$ before the most recent ↑ transition of the clock; indicates a one-bit shift.

# 8-Bit Parallel In/Serial Out Shift Registers

## General Description

These are 8-bit serial shift registers which shift the data in the direction of $Q_A$ toward $Q_H$ when clocked. Parallel-in access is made available by eight individual direct data inputs, which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

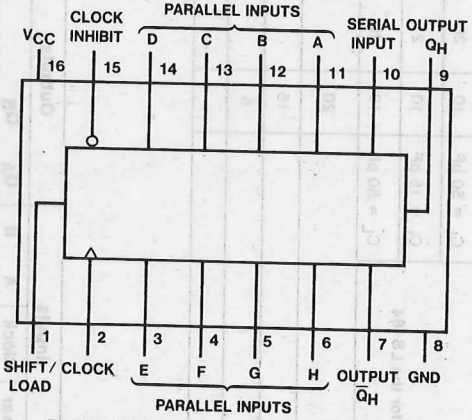
Clocking is accomplished through a 2-input NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input, regardless of the logic levels on the clock, clock inhibit, or serial inputs.

## Features

- Complementary outputs
- Direct overriding (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion

| Type | Typical Frequency | Typical Power Dissipation |
|---|---|---|
| 165 | 20 MHz | 200 mW |
| L165A | 14 MHz | 30 mW |
| LS165 | 35 MHz | 105 mW |

## Connection Diagram




**54165 (J,W)**
**54L165A (J,W)**
**54LS165 (J,W)**

**74165 (N)**
**74L165A (N)**
**74LS165 (N)**

## Truth Table

| Inputs | | | | | Internal Outputs | | Output $Q_H$ |
|---|---|---|---|---|---|---|---|
| Shift/ Load | Clock Inhibit | Clock | Serial | Parallel A...H | $Q_A$ | $Q_B$ | |
| L | X | X | X | a...h | a | b | h |
| H | L | L | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |
| H | L | ↑ | H | X | H | $Q_{An}$ | $Q_{Gn}$ |
| H | L | ↑ | L | X | L | $Q_{An}$ | $Q_{Gn}$ |
| H | H | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |

H = High Level (steady state), L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from low-to-high level
a...h = The level of steady-state input at inputs A through H, respectively.
$Q_{A0}$, $Q_{B0}$, $Q_{H0}$ = The level of $Q_A$, $Q_B$, or $Q_H$, respectively, before the indicated steady-state input conditions were established.
$Q_{An}$, $Q_{Gn}$ = The level of $Q_A$ or $Q_G$, respectively, before the most recent ↑ transition of the clock.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM54/74 165 | | | DM54/74 L165A | | | DM54/74 LS165 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | | 0.8 | | | 0.7 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | N/A | | | | V |
| | | | | $I_I$ = −18 mA | | | | | | | N/A | | | −1.5 | |
| $I_{OH}$ | High Level Output Current | | | | | | | −800 | | | −200 | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.4 | | | 2.4 | | | 2.5 | 3.4 | | V |
| | | | | | DM74 | 2.4 | | | 2.4 | | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 16 | | | 2 | | | 4 | mA |
| | | | | | DM74 | | | 16 | | | 3.6 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OL}$ = Max | | DM54 | | 0.2 | 0.4 | | | 0.3 | | 0.25 | 0.4 | V |
| | | | | | DM74 | | 0.2 | 0.4 | | | 0.4 | | 0.35 | 0.5 | |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max, $V_I$ = 5.5 V | | All Inputs | | | 1 | | | 0.1 | | | | mA |
| | | | $V_{CC}$ = Max, $V_I$ = 7 V | | Shift/Load | | | | | | | | | 0.3 | |
| | | | | | Other Inputs | | | | | | | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | Load Input | $V_{CC}$ = Max, $V_I$ = 2.4 V, $V_I$ = 2.7 V (LS165) | | | | | 80 | | | 30 | | | 60 | μA |
| | | Other Inputs | | | | | | 40 | | | 10 | | | 20 | |
| $I_{IL}$ | Low Level Input Current | Load Input | $V_{CC}$ = Max | $V_I$ = 0.3 V for L165A | | | | −3.2 | | | −0.54 | | | −1.2 | mA |
| | | Other Inputs | | $V_I$ = 0.4 V for 165 | | | | −1.6 | | | −0.18 | | | −0.4 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | DM54 | −20 | | −55 | −3 | | −15 | −20 | | −100 | mA |
| | | | | | DM74 | −18 | | −55 | −3 | | −15 | −20 | | −100 | |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (3) | | | | 40 | 63 | | | 9.5 | | 21 | 36 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

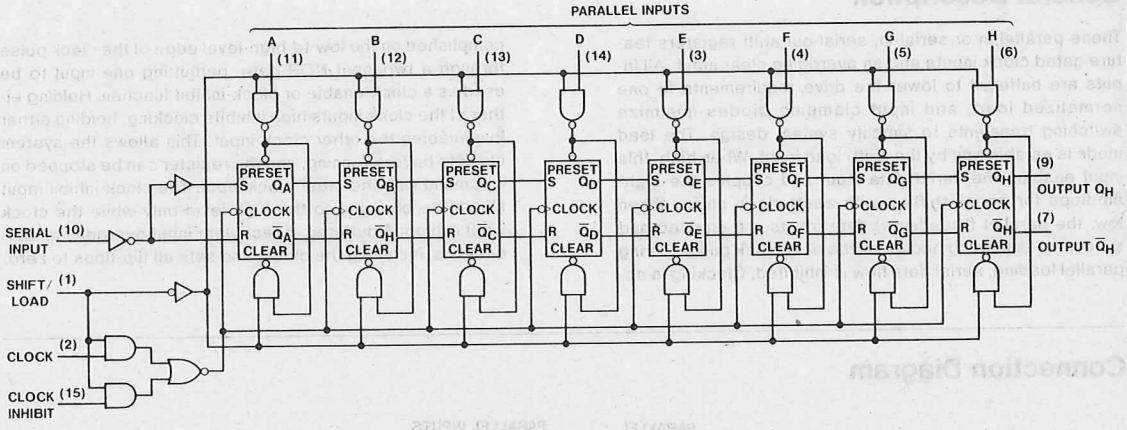
**Note 2:** Not more that one output should be shorted at a time and for DM54LS/74LS duration should not exceed one second.

**Note 3:** With the outputs open, clock inhibit and shift/load at 4.5 V, and a clock pulse applied to the clock input, $I_{CC}$ is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

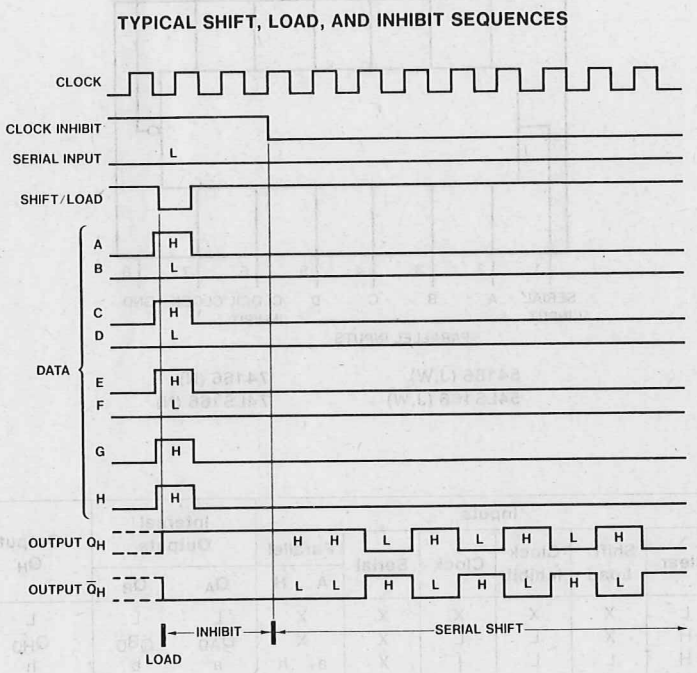
## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | DM54/74 165 Conditions | DM54/74 165 Min | DM54/74 165 Typ | DM54/74 165 Max | DM54/74 L165A Conditions | DM54/74 L165A Min | DM54/74 L165A Typ | DM54/74 L165A Max | DM54/74 LS165 Conditions | DM54/74 LS165 Min | DM54/74 LS165 Typ | DM54/74 LS165 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | | | $C_L$ = 15 pF, $R_L$ = 400 Ω | 14 | 20 | | $C_L$ = 50 pF, $R_L$ = 4 kΩ | 6 | 14 | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 25 | 35 | | MHz |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 20 | 30 | | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Load | Any | | | 34 | 50 | | | 44 | 88 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 22 | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 42 | 60 | | | 62 | 124 | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 25 | 38 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Clock | Any | | | 26 | 40 | | | 35 | 70 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 22 | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 35 | 50 | | | 50 | 100 | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 28 | 42 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | H | $Q_H$ | | | 25 | 40 | | | 33 | 66 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 27 | 40 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 36 | 50 | | | 56 | 112 | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 30 | 45 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | H | $\overline{Q}_H$ | | | 25 | 40 | | | 33 | 66 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 28 | 40 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 36 | 50 | | | 56 | 112 | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 35 | 52 | |
| | | | | | | | | | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 14 | 25 | ns |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 17 | 26 | |
| | | | | | | | | | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 21 | 30 | ns |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 28 | 42 | |
| | | | | | | | | | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 21 | 30 | ns |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 25 | 38 | |
| | | | | | | | | | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 16 | 25 | ns |
| | | | | | | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 22 | 33 | |
| $t_{W(CLOCK)}$ | Width of Clock Input Pulse | | | | 35 | | | | 100 | | | | 25 | | | ns |
| $t_{W(LOAD)}$ | Width of Load Input Pulse | | | | 35 | | | | 100 | | | | 15 | | | ns |
| $t_{SETUP}$ | Parallel Input Setup Time | | | | 25 | | | | 44 | | | | 10 | | | ns |
| $t_{SETUP}$ | Serial Input Setup Time | | | | 40 | | | | 44 | | | | 20 | | | ns |
| $t_{HOLD}$ | Hold Time at Any Input | | | | 5 | | | | 10 | | | | 0 | | | ns |
| $t_{SETUP}$ | Clock Enable Setup Time | | | | | | | | | | | | 30 | | | ns |
| $t_{SETUP}$ | Shift Setup Time | | | | | | | | | | | | 45 | | | ns |

## Logic Diagram




## Timing Diagram

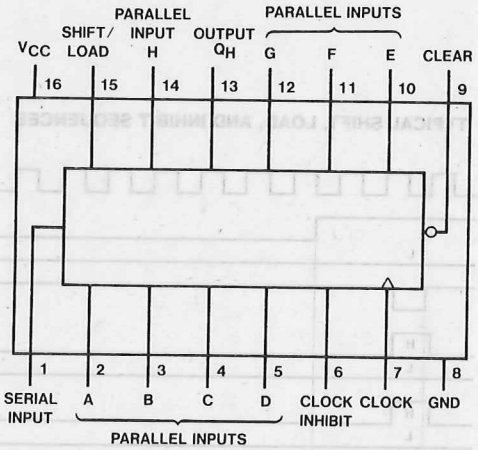


# 8-Bit Parallel In/Serial Out Shift Registers

## General Description

These parallel-in or serial-in, serial-out shift registers feature gated clock inputs and an overriding clear input. All inputs are buffered to lower the drive requirements to one normalized load, and input clamping diodes minimize switching transients to simplify system design. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

## Connection Diagram




54166 (J,W)
54LS166 (J,W)

74166 (N)
74LS166 (N)

## Truth Table

| Inputs | | | | | | Internal Outputs | | Output $Q_H$ |
|---|---|---|---|---|---|---|---|---|
| Clear | Shift/ Load | Clock Inhibit | Clock | Serial | Parallel A...H | $Q_A$ | $Q_B$ | |
| L | X | X | X | X | X | L | L | L |
| H | X | L | L | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |
| H | L | L | ↑ | X | a...h | a | b | h |
| H | H | L | ↑ | H | X | H | $Q_{An}$ | $Q_{Gn}$ |
| H | H | L | ↑ | L | X | L | $Q_{An}$ | $Q_{Gn}$ |
| H | X | H | ↑ | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

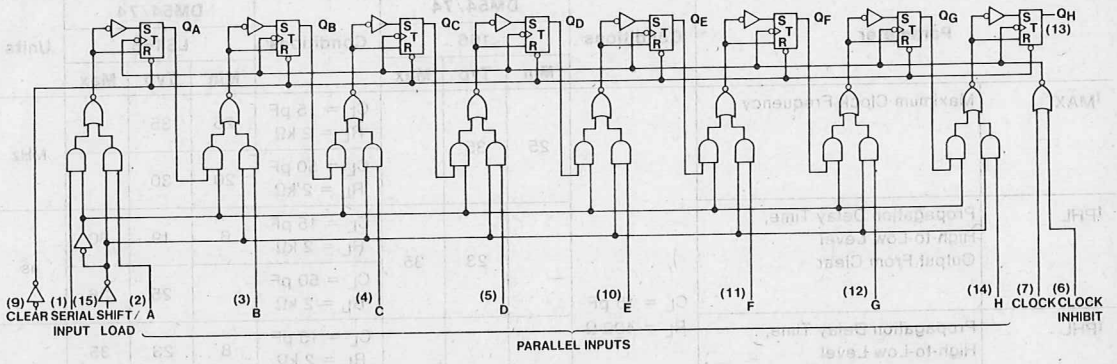
↑ = Transition from low to high level

a...h = The level of steady-state input at inputs A through H, respectively

$Q_{A0}$, $Q_{B0}$, $Q_{H0}$ = The level of $Q_A$, $Q_B$, $Q_H$, respectively, before the indicated steady-state input conditions were established

$Q_{An}$, $Q_{Gn}$ = The level of $Q_A$, $Q_G$, respectively, before the most recent ↑ transition of the clock

## Logic Diagram




## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 166 | | | DM54/74 LS166 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | | V |
| | | | $I_I$ = −18 mA | | | | | | | −1.5 | |
| $I_{OH}$ | High Level Output Current | | | | | | −800 | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | DM54 | 2.4 | | | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.4 | | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | | | 4 | mA |
| | | | | DM74 | | | 16 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = Max | | DM54 | | | 0.4 | | 0.25 | 0.4 | V |
| | | | | DM74 | | | 0.4 | | 0.35 | 0.5 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | | mA |
| | | | $V_I$ = 7 V | | | | | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | | μA |
| | | | $V_I$ = 2.7 V | | | | | | | 20 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | | −1.6 | | | −0.4 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −20 | | −57 | −20 | | −100 | mA |
| | | | | DM74 | −18 | | −57 | −20 | | −100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | DM54 | | 72 | 104 | | 22 | 38 | mA |
| | | | | DM74 | | 72 | 116 | | 22 | 38 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, for LS the duration should not exceed one second.

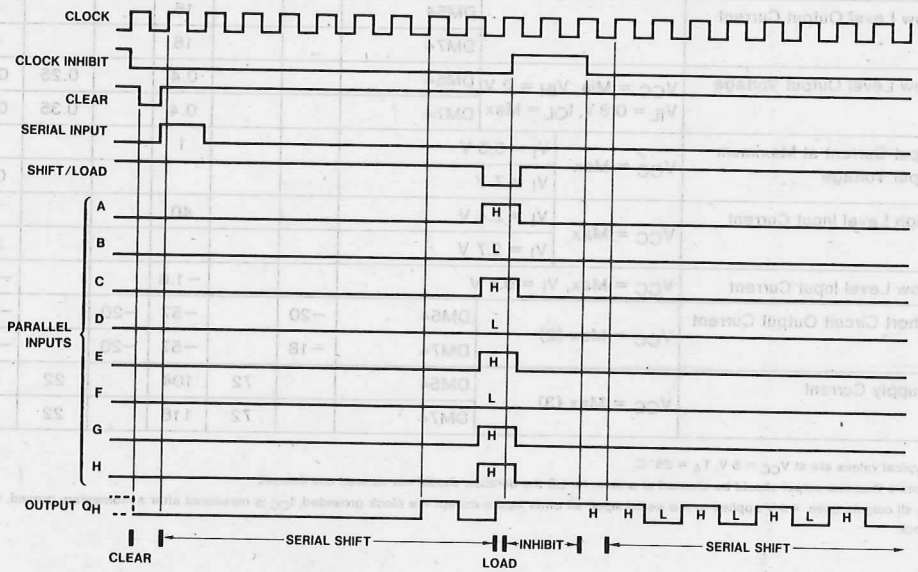
**Note 3:** With all outputs open, 4.5 V applied to the serial input, all other inputs except the clock grounded, $I_{CC}$ is measured after a momentary ground, then 4.5 V, is applied to clock.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | DM54/74 166 | | | Conditions | DM54/74 LS166 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | $C_L$ = 15 pF, $R_L$ = 400 Ω | 25 | 35 | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 25 | 35 | | MHz |
| | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 20 | 30 | | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Clear | | | 23 | 35 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 6 | 19 | 30 | ns |
| | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 25 | 36 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Clock | | 8 | 20 | 30 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 8 | 23 | 35 | ns |
| | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 29 | 41 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output From Clock | | 8 | 17 | 26 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 8 | 24 | 35 | ns |
| | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 27 | 38 | |
| $t_W$ | Width of Clock or Clear Pulse | | 20 | | | | 20 | | | ns |
| $t_{SETUP}$ | Mode Control Setup Time | | 30 | | | | 30 | | | ns |
| $t_{SETUP}$ | Data Setup Time | | 20 | | | | 20 | | | ns |
| $t_{HOLD}$ | Hold Time at Any Input | | 0 | | | | 0 | | | ns |

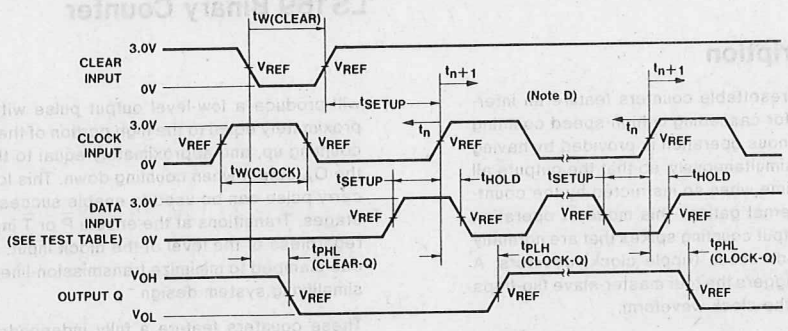
## Timing Diagram

**Typical Clear, Shift, Load, Inhibit, and Shift Sequences**



## Parameter Measurement Information

### Voltage Waveforms




### Test Table For Synchronous Inputs

| Data Input For Test | Shift/Load | Output Tested (See Note C) |
|---|---|---|
| H | 0 V | $Q_H$ at $T_{N+1}$ |
| Serial Input | 4.5 V | $Q_H$ at $T_{N+8}$ |

**Note A:** The clock pulse has the following characteristics: $t_{W(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{W(clear)} \geq 20$ ns and $t_{HOLD} = 0$ ns. When testing $f_{MAX}$, vary the clock PRR.

**Note B:** A clear pulse is applied prior to each test.

**Note C:** Propagation delay times ($t_{PLH}$ and $t_{PHL}$) are measured at $t_{n+1}$. Proper shifting of data is verified at $t_{n+8}$ with a functional test.

**Note D:** $t_n$ = bit time before clocking transition
$t_{n+1}$ = bit time after one clocking transition
$t_{n+8}$ = bit time after eight clocking transitions

**Note E:** $V_{REF}$ = 1.5 V for 166 and 1.3 V for LS166

# Synchronous 4-Bit Up/Down Counters
## 'LS168 Decade Counter
## 'LS169 Binary Counter

## General Description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs all change at the same time when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset either high or low. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

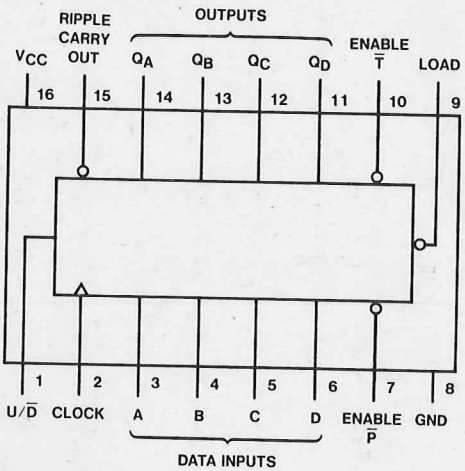
The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count-enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry outputs. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the $Q_A$ output when counting up, and approximately equal to the low portion of the $Q_A$ output when counting down. This low-level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down), which modify the operating mode, have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

## Features

- Fully synchronous operation for counting and programming.
- Internal look-ahead for fast counting.
- Carry output for n-bit cascading.
- Fully independent clock circuit

## Connection Diagram




**54LS168 (J,W)**
**54LS169 (J,W)**

**74LS168 (N)**
**74LS169 (N)**

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | DM54/74 LS168, LS169 Min | Typ (1) | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −400 μA | DM54 | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 4 | mA |
| | | | | DM74 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $I_{OL}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | DM54 | | 0.25 | 0.4 | V |
| | | | | DM74 | | 0.35 | 0.5 | |
| $I_I$ | Input Current at Maximum Input Voltage | A, B, C, D, P, U/D | $V_{CC}$ = Max, $V_I$ = 7 V | | | | 0.1 | mA |
| | | Clock, T | | | | | 0.1 | |
| | | Load | | | | | 0.2 | |
| $I_{IH}$ | High Level Input Current | A, B, C, D, P, U/D | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | 20 | μA |
| | | Clock, T | | | | | 20 | |
| | | Load | | | | | 40 | |
| $I_{IL}$ | Low Level Input Current | A, B, C, D, P, U/D | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −0.4 | mA |
| | | T | | | | | −0.4 | |
| | | Load, Clock | | | | | −0.4 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (3) | | | 20 | 34 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

**Note 3:** $I_{CC}$ is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

6

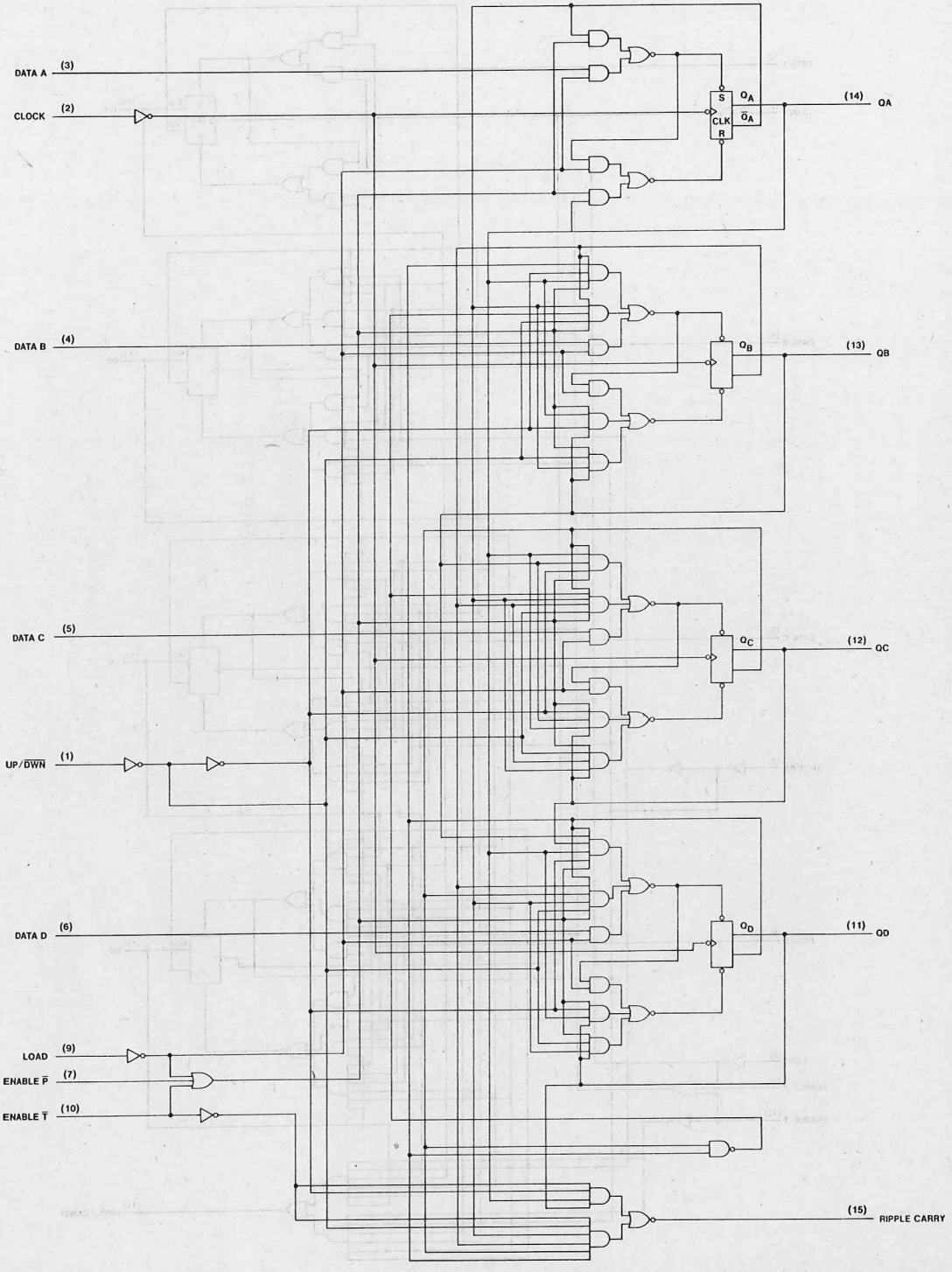
## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | To (Output) | Conditions | DM54/DM74 LS168, LS169 Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 25 | 32 | | MHz |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 20 | 28 | | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock | Ripple Carry | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 23 | 35 | ns |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 26 | 39 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 23 | 35 | |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 29 | 44 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock | Any Q | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 13 | 20 | ns |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 16 | 24 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 15 | 23 | |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 21 | 32 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Enable $\overline{T}$ | Ripple Carry | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 12 | 18 | ns |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 15 | 24 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 12 | 18 | |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 18 | 28 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Up/Down (4) | Ripple Carry | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 17 | 25 | ns |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 20 | 30 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 19 | 29 | |
| | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 25 | 38 | |
| $t_{W(CLOCK)}$ | Width of Clock Pulse (High or Low) | | | | | 25 | | | ns |
| $t_{SETUP}$ | Setup Time | Data Inputs A, B, C, D | | | | 20 | | | ns |
| | | Enable $\overline{P}$ or $\overline{T}$ | | | | 20 | | | |
| | | Load | | | | 25 | | | |
| | | Up/Down | | | | 30 | | | |
| $t_{HOLD}$ | Hold Time | Data Inputs A, B, C, D | | | | 0 | | | ns |
| | | Enable $\overline{P}$ or $\overline{T}$ | | | | 0 | | | |
| | | Load, Up/Down | | | | 0 | | | |

**Note 4:** Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for LS168 or 15 for LS169), the ripple carry output will be out of phase.

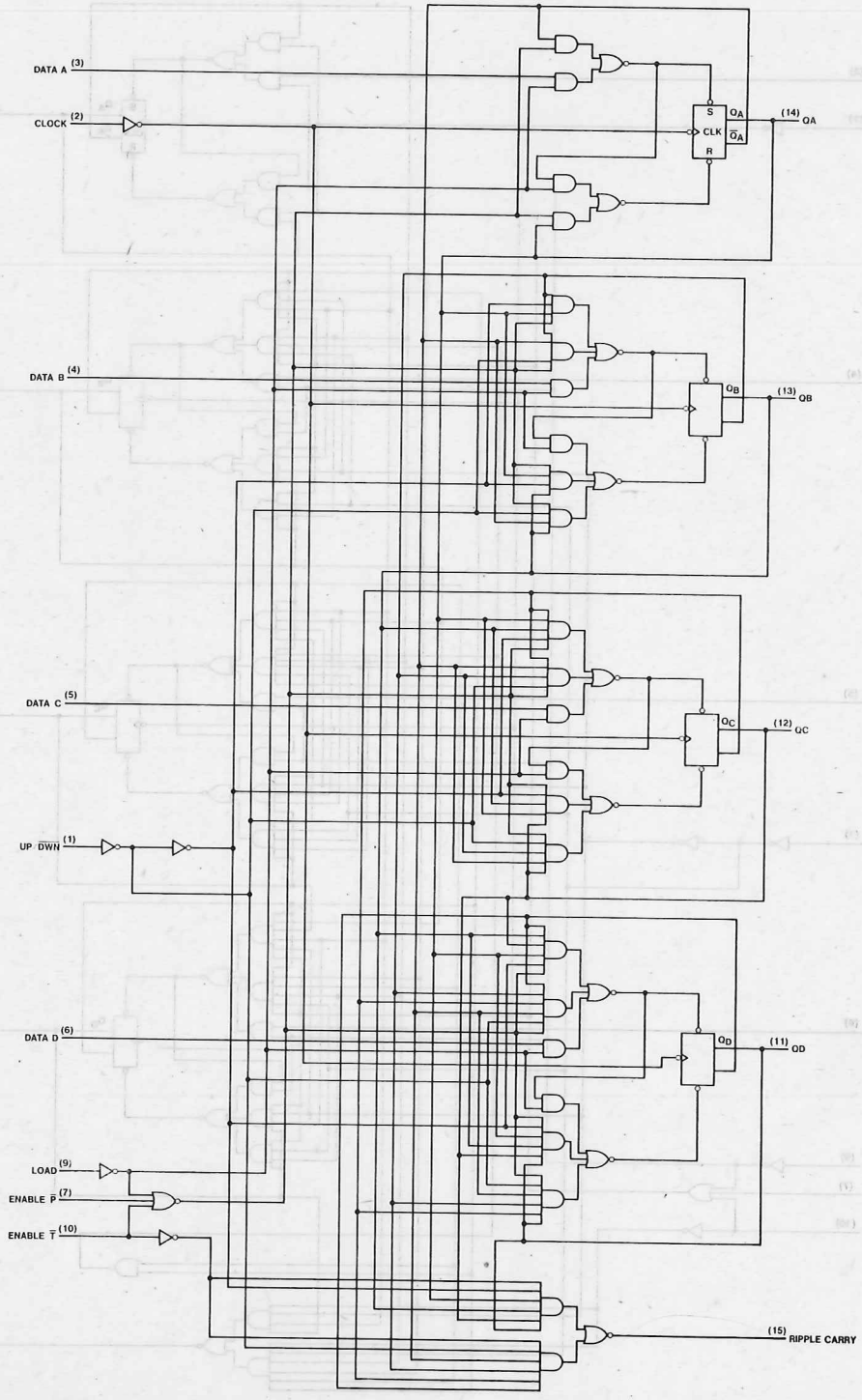
## Logic Diagram

LS168 Decade Counter



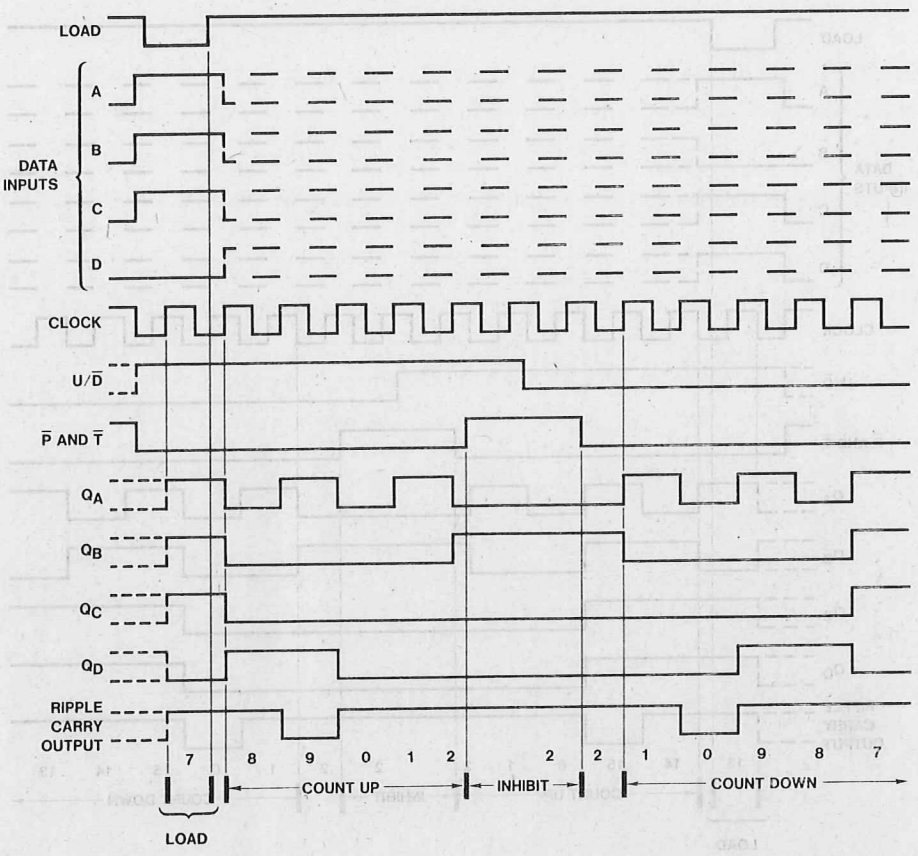
## Logic Diagram

LS169 Binary Counter



## Timing Diagrams

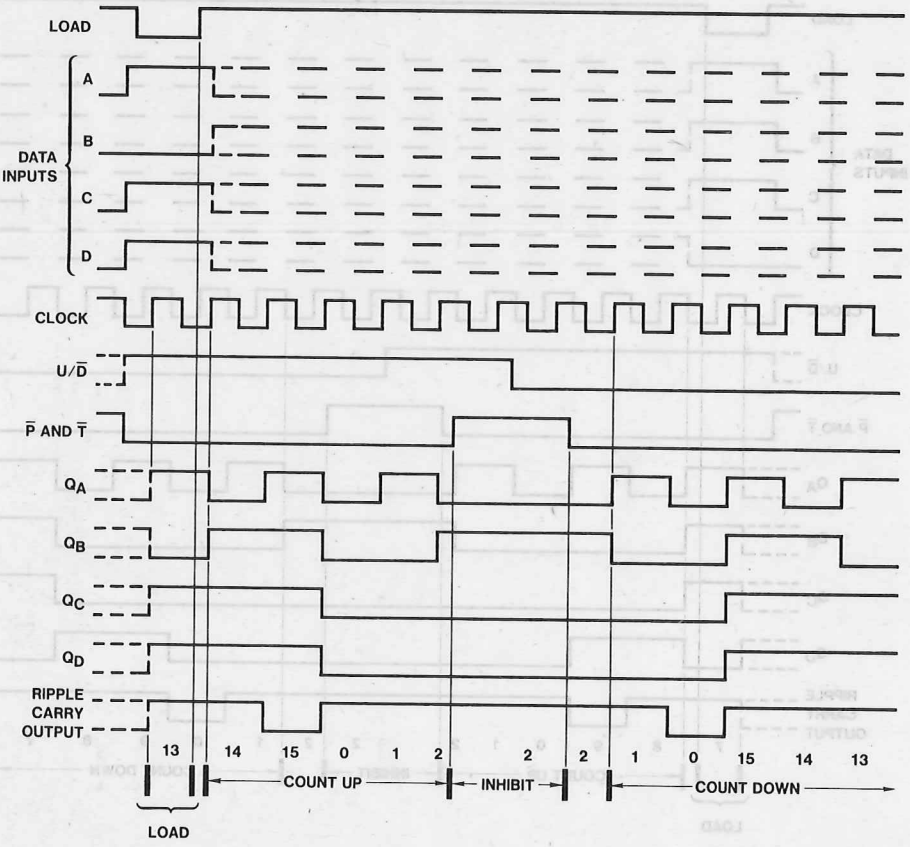
LS168 Decade Counters
Typical Load, Count, and Inhibit Sequences




**Sequence 1:** Load (preset) to BCD seven
**Sequence 2:** Count up to eight, nine, zero, one and two
**Sequence 3:** Inhibit
**Sequence 4:** Count down to one, zero, nine, eight and seven

## Timing Diagrams (Continued)

**LS169 Binary Counters**
**Typical Load, Count, and Inhibit Sequences**




**Sequence 1:** Load (preset) to binary thirteen
**Sequence 2:** Count up to fourteen, fifteen, zero, one and two
**Sequence 3:** Inhibit
**Sequence 4:** Count down to one, zero, fifteen, fourteen and thirteen

# 4 by 4 Register Files

## General Description

These 16-bit TTL register files are organized as 4 words of 4 bits each, and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits writing into one location and reading from another word location, simultaneously.

Four data inputs are available to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B, in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, $G_W$, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, $G_R$, is high, the data outputs are inhibited and remain high.

The individual address lines permit direct reading of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

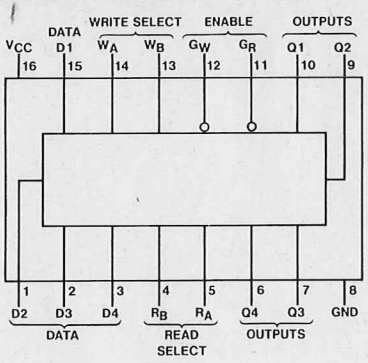
This arrangement—data entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (30 ns typical) and the read time (25 ns typical). The register file has a nondestructive readout in that data is not lost when addressed.

All 170 inputs and all inputs except the read enable and write enable of the LS170 are buffered to lower the drive requirements to one standard load. Input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

## Features

- Separate addressing permits simultaneous reading and writing
- Fast access times typically 20 ns
- Organized as 4 words of 4 bits
- Expandable to 1024 words of n-bits
- For use as:
  - Scratch-pad memory
  - Buffer storage between processors
  - Bit storage in fast multiplication designs
- Open-collector outputs with low maximum off-state current:
  - 170 30 $\mu$A
  - LS170 20 $\mu$A
- DM54LS670 and DM74LS670 are similar but have TRI-STATE outputs

## Connection Diagram




74170 (N)
54LS170 (J,W); 74LS170 (N)

## Truth Tables

**WRITE TRUTH TABLE (SEE NOTES A, B, AND C)**

| Write Inputs | | | Word | | | |
|---|---|---|---|---|---|---|
| $W_B$ | $W_A$ | $G_W$ | 0 | 1 | 2 | 3 |
| L | L | L | Q = D | $Q_0$ | $Q_0$ | $Q_0$ |
| L | H | L | $Q_0$ | Q = D | $Q_0$ | $Q_0$ |
| H | L | L | $Q_0$ | $Q_0$ | Q = D | $Q_0$ |
| H | H | L | $Q_0$ | $Q_0$ | $Q_0$ | Q = D |
| X | X | H | $Q_0$ | $Q_0$ | $Q_0$ | $Q_0$ |

**READ TRUTH TABLE (SEE NOTES A AND D)**

| Read Inputs | | | Outputs | | | |
|---|---|---|---|---|---|---|
| $R_B$ | $R_A$ | $G_R$ | Q1 | Q2 | Q3 | Q4 |
| L | L | L | W0B1 | W0B2 | W0B3 | W0B4 |
| L | H | L | W1B1 | W1B2 | W1B3 | W1B4 |
| H | L | L | W2B1 | W2B2 | W2B3 | W2B4 |
| H | H | L | W3B1 | W3B2 | W3B3 | W3B4 |
| X | X | H | H | H | H | H |

**Note A:** H = High Level, L = Low Level, X = Don't Care

**Note B:** (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

**Note C:** $Q_0$ = The level of Q before the indicated input conditions were established.

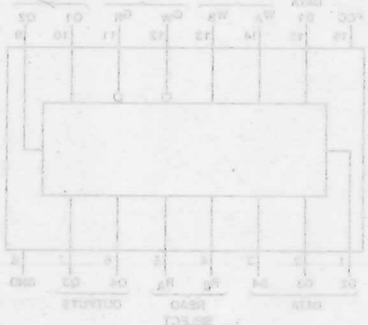
**Note D:** W0B1 = The first bit of word 0, etc.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM74 170 | | | DM54/74 LS170 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | DM54 | | | N/A | | | 0.8 | V |
| | | | | | DM74 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | | V |
| | | | | $I_I$ = −18 mA | | | | | | | −1.5 | |
| $I_{OH}$ | High Level Output Current | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $V_{OH}$ = 5.5 V | | | | | 30 | | | 20 | μA |
| $V_{OH}$ | High Level Output Voltage | | | | | | | 5.5 | | | 5.5 | V |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | N/A | | | 4 | mA |
| | | | | | DM74 | | | 16 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = 4 mA | DM74 | | | | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$ = Max | DM54 | | | N/A | | 0.25 | 0.4 | |
| | | | | | DM74 | | 0.2 | 0.4 | | 0.35 | 0.5 | |
| $I_I$ | Input Current at Maximum Input Voltage | Any | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | | mA |
| | | Any D, R, or W | | $V_I$ = 7 V | | | | | | | 0.1 | |
| | | $G_R$ or $G_W$ | | | | | | | | | 0.2 | |
| $I_{IH}$ | High Level Input Current | Any | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | | μA |
| | | Any D, R, or W | | $V_I$ = 2.7 V | | | | | | | 20 | |
| | | $G_R$ or $G_W$ | | | | | | | | | 40 | |
| $I_{IL}$ | Low Level Input Current | Any D, R, or W | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | | −1.6 | | | −0.4 | mA |
| | | $G_R$ or $G_W$ | | | | | | −1.6 | | | −0.8 | |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (2) | | | | 127 | 150 | | 25 | 40 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** $I_{CC}$ is measured under the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.



## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

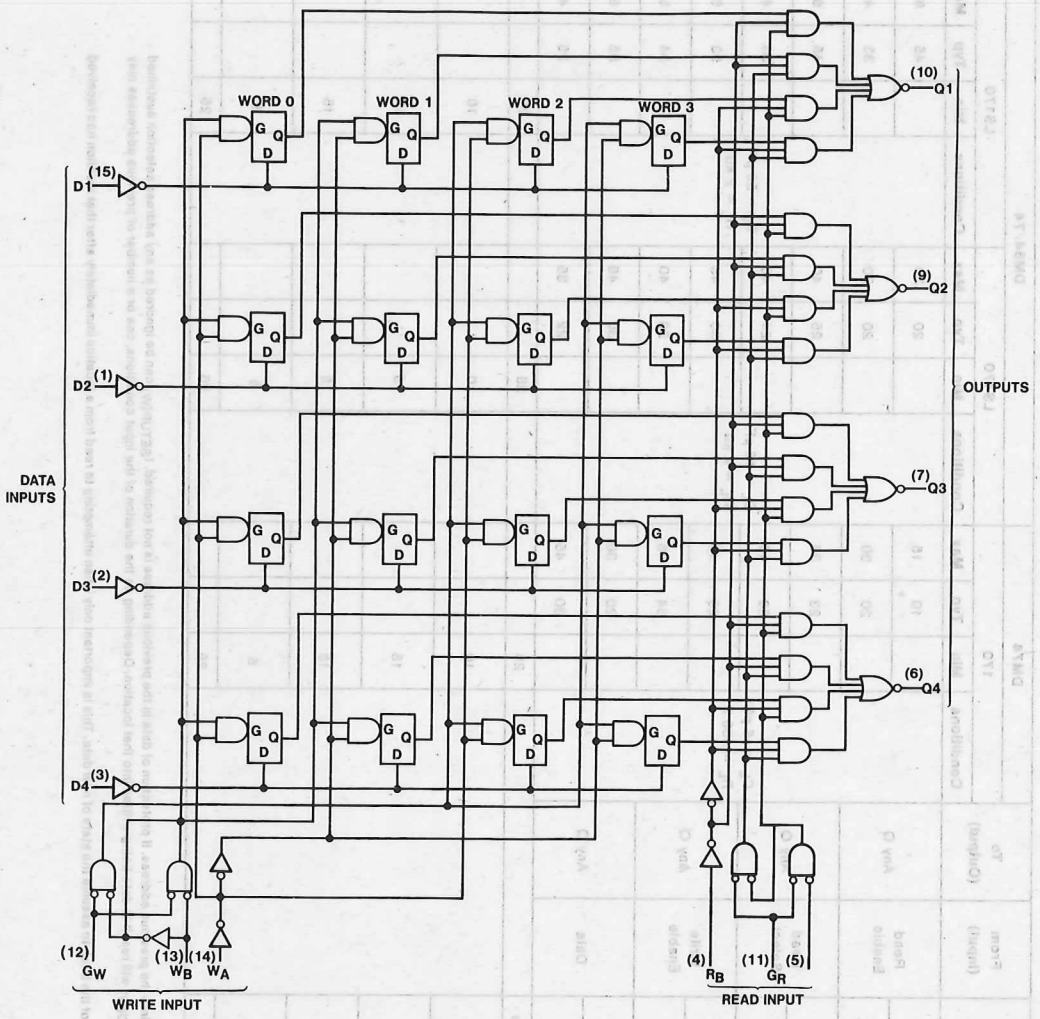
| Parameter | | | From (Input) | To (Output) | DM74 170 Conditions | DM74 170 Min | DM74 170 Typ | DM74 170 Max | DM54/74 LS170 Conditions | DM54/74 LS170 Min | DM54/74 LS170 Typ | DM54/74 LS170 Max | DM54/74 LS170 Conditions | DM54/74 LS170 Min | DM54/74 LS170 Typ | DM54/74 LS170 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Read Enable | Any Q | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 10 | 15 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 20 | 30 | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 45 | 60 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 20 | 30 | | | 20 | 30 | | | 33 | 40 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Read Select | Any Q | | | 23 | 35 | | | 25 | 40 | | | 45 | 60 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 30 | 40 | | | 24 | 40 | | | 33 | 40 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Write Enable | Any Q | | | 25 | 40 | | | 30 | 45 | | | 53 | 65 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 34 | 45 | | | 26 | 40 | | | 34 | 50 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Data | Any Q | | | 20 | 30 | | | 30 | 45 | | | 55 | 65 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 30 | 45 | | | 22 | 35 | | | 25 | 40 | |
| $t_W$ | Width of Write-Enable or Read-Enable Pulse | | | | | 25 | | | | 25 | | | | 25 | | | ns |
| $t_{SETUP}$ | Setup Time, High- or Low-Level Data (3) | Data Input With Respect to Write Enable, $t_{SETUP(D)}$ | | | | 10 | | | | 10 | | | | 10 | | | ns |
| | | Write Select With Respect to Write Enable, $t_{SETUP(W)}$ | | | | 15 | | | | 15 | | | | 15 | | | ns |
| $t_{HOLD}$ | Hold Times, High- or Low-Level Data (3) | Data Input With Respect to Write Enable, $t_{HOLD(D)}$ | | | | 15 | | | | 15 | | | | 15 | | | ns |
| | | Write Select With Respect to Write Enable, $t_{HOLD(W)}$ | | | | 5 | | | | 5 | | | | 5 | | | ns |
| $t_{LATCH}$ | Latch Time for New Data (4) | | | | | 25 | | | | 25 | | | | 25 | | | ns |

**Note 3:** Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{SETUP(W)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{HOLD(W)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

**Note 4:** Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.

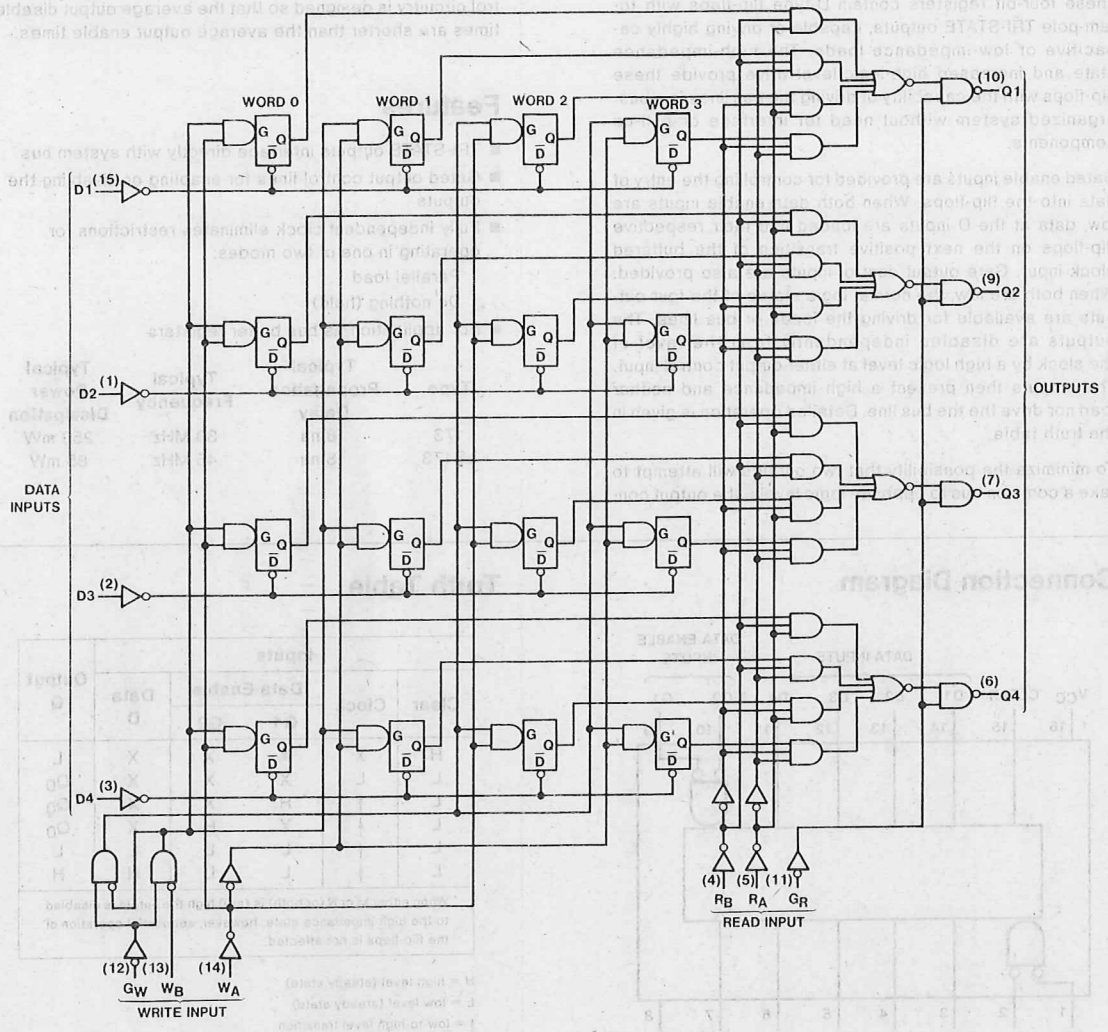
## Logic Diagrams

LS170



## Logic Diagrams (Continued)

170



# TRI-STATE® Quad D Registers

## General Description

These four-bit registers contain D-type flip-flops with totem-pole TRI-STATE outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.

Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the the bus line. Detailed operation is given in the truth table.

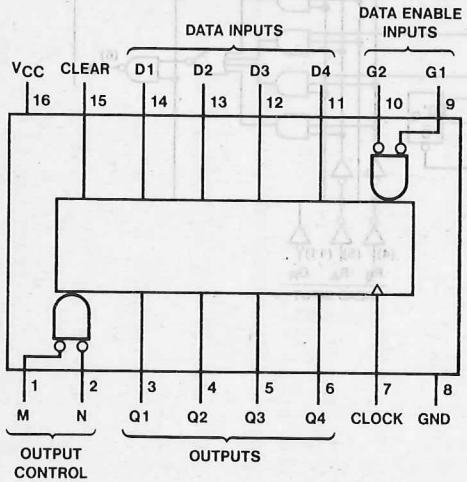
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

## Features

- TRI-STATE outputs interface directly with system bus
- Gated output control lines for enabling or disabling the outputs
- Fully independent clock eliminates restrictions for operating in one of two modes:
  - Parallel load
  - Do nothing (hold)
- For application as bus buffer registers

| Type | Typical Propagation Delay | Typical Frequency | Typical Power Dissipation |
|---|---|---|---|
| 173 | 18 ns | 30 MHz | 250 mW |
| LS173 | 18 ns | 45 MHz | 85 mW |

## Connection Diagram




**54173 (J,W)**
**54LS173 (J,W)**

**74173 (N)**
**74LS173 (N)**

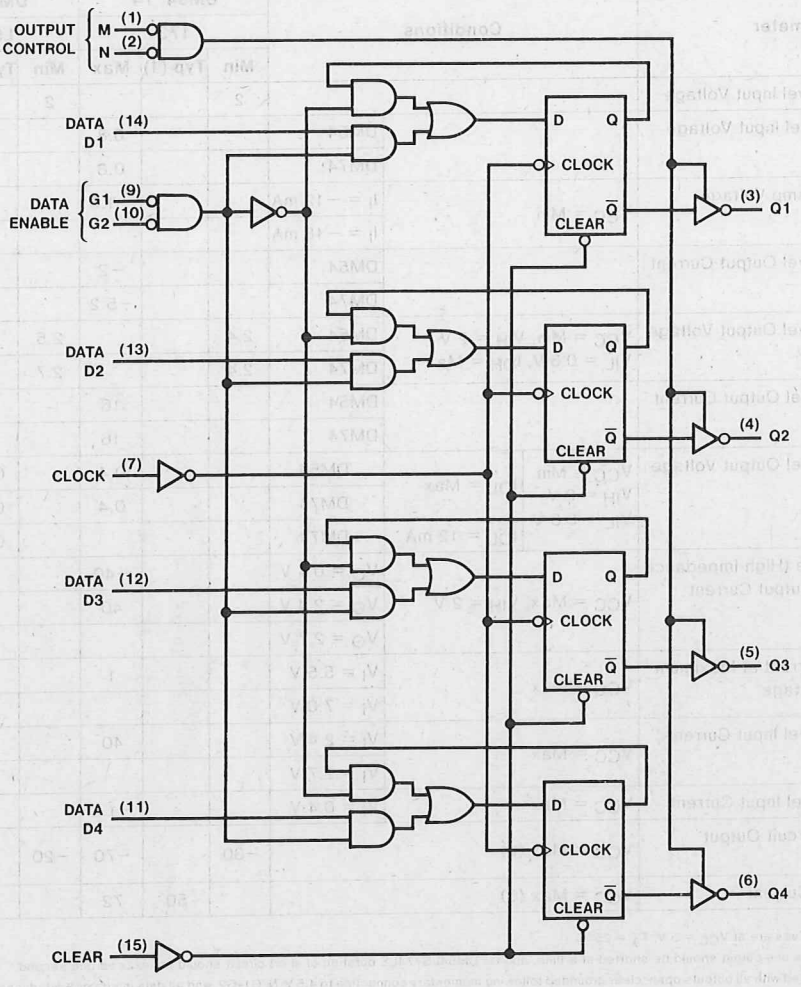
## Truth Table

| Inputs | | | | | Output |
|---|---|---|---|---|---|
| Clear | Clock | Data Enable G1 | Data Enable G2 | Data D | Q |
| H | X | X | X | X | L |
| L | L | X | X | X | $Q_0$ |
| L | ↑ | H | X | X | $Q_0$ |
| L | ↑ | X | H | X | $Q_0$ |
| L | ↑ | L | L | L | L |
| L | ↑ | L | L | H | H |

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

H = high level (steady state)
L = low level (steady state)
↑ = low-to-high level transition
X = don't care (any input including transitions)
$Q_0$ = the level of Q before the indicated steady state input conditions were established

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 173 | | | DM54/74 LS173 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | | $I_I$ = −12 mA | | | −1.5 | | | | V |
| | | | | $I_I$ = −18 mA | | | | | | −1.5 | |
| $I_{OH}$ | High Level Output Current | | | DM54 | | | −2 | | | −1.0 | mA |
| | | | | DM74 | | | −5.2 | | | −2.6 | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | DM54 | 2.4 | | | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.4 | | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | | | 12 | mA |
| | | | | DM74 | | | 16 | | | 24 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $I_{OL}$ = Max | DM54 | | | 0.4 | | 0.25 | 0.4 | V |
| | | | | DM74 | | | 0.4 | | 0.35 | 0.5 | |
| | | | $I_{OL}$ = 12 mA | DM74 | | | | | 0.25 | 0.4 | |
| $I_{O(OFF)}$ | Off-State (High-Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V | | $V_O$ = 0.4 V | | | −40 | | | −20 | μA |
| | | | | $V_O$ = 2.4 V | | | 40 | | | | |
| | | | | $V_O$ = 2.7 V | | | | | | 20 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | | $V_I$ = 5.5 V | | | 1 | | | | mA |
| | | | | $V_I$ = 7.0 V | | | | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | | $V_I$ = 2.4 V | | | 40 | | | | μA |
| | | | | $V_I$ = 2.7 V | | | | | | 20 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | | $V_I$ = 0.4 V | | | −1.6 | | | −0.4 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | | −30 | | −70 | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | | | 50 | 72 | | 17 | 24 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

**Note 3:** $I_{CC}$ is measured with all outputs open; clear grounded following momentary connection to 4.5 V; N, G1, G2, and all data inputs grounded; and the clock input and M at 4.5 V.

## Switching Characteristics $V_{CC}$ = 5 V; $T_A$ = 25°C

| Parameter | | | Conditions | DM54/74 173 | | | Conditions | DM54/74 LS173 | | | Conditions | DM54/74 LS173 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | Min | Typ | Max | | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | $C_L$ = 50 pF, $R_L$ = 400 Ω | 25 | 30 | | $C_L$ = 45 pF, $R_L$ = 2 kΩ | 30 | 45 | | $C_L$ 150 pF, $R_L$ = 2 kΩ | 20 | 30 | | MHz |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Clear | | | | 18 | 27 | | | 20 | 30 | | | 26 | 40 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output From Clock | | | | 16 | 25 | | | 16 | 25 | | | 21 | 34 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Clock | | | | 20 | 28 | | | 20 | 30 | | | 26 | 40 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | | | 7 | 16 | 30 | | 7 | 18 | 27 | | 9 | 27 | 40 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | 7 | 21 | 30 | | 7 | 18 | 27 | | 9 | 30 | 45 | ns |
| $t_{HZ}$ | Output Disable Time From High Level | | $C_L$ = 5 pF, $R_L$ = 400 Ω | 3 | 5 | 14 | $C_L$ = 5 pF, $R_L$ = 2 kΩ | 3 | 11 | 17 | | | | | ns |
| $t_{LZ}$ | Output Disable Time From Low Level | | | 3 | 11 | 20 | | 3 | 10 | 20 | | | | | ns |
| $t_W$ | Width of Clock or Clear Pulse | | | 20 | | | | 17 | | | | 17 | | | ns |
| $t_{SETUP}$ | Setup Time | Data Enable | | 17 | | | | 17 | | | | 17 | | | ns |
| | | Data | | 10 | | | | 10 | | | | 10 | | | |
| | | Clear Inactive State | | 10 | | | | 10 | | | | 10 | | | |
| $t_{HOLD}$ | Hold Time | Data Enable | | 2 | | | | 0 | | | | 0 | | | ns |
| | | Data | | 10 | | | | 0 | | | | 0 | | | |

# Hex/Quad D Flip-Flops with Clear

## General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) versions feature complementary outputs from each flip-flop.

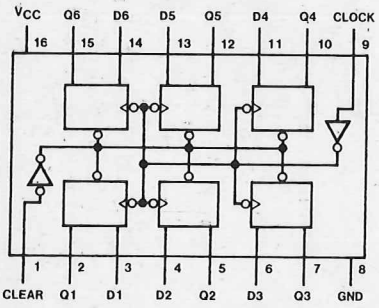
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

## Features

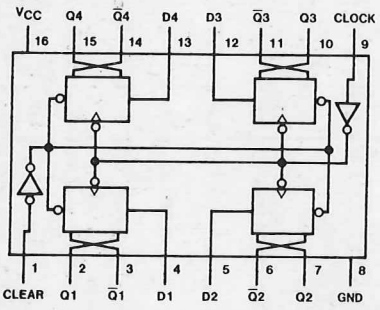
- 174, LS174, S174 contain six flip-flops with single-rail outputs.
- 175, LS175, S175 contain four flip-flops with double-rail outputs.
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers
  - Shift registers
  - Pattern generators

| Type | Typical Clock Frequency | Typical Power Dissipation Per Flip-Flop |
|---|---|---|
| 174, 175 | 40 MHz | 38 mW |
| LS174, LS175 | 40 MHz | 14 mW |
| S174, S175 | 110 MHz | 75 mW |

## Connection Diagrams

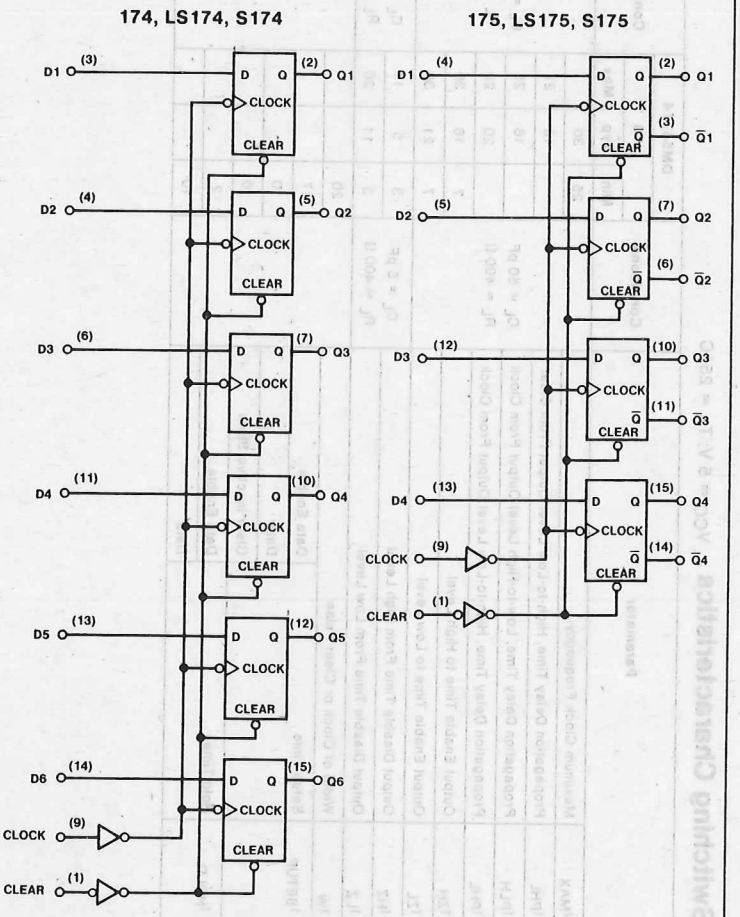



**54174 (J,W)** **74174 (N)**
**54LS174 (J,W)** **74LS174 (N)**
**54S174 (J,W)** **74S174 (N)**




**54175 (J,W)** **74175 (N)**
**54LS175 (J,W)** **74LS175 (N)**
**54S175 (J,W)** **74S175 (N)**

## Logic Diagrams



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM54/74 174, 175 Min | DM54/74 174, 175 Typ (1) | DM54/74 174, 175 Max | DM54/74 LS174, LS175 Min | DM54/74 LS174, LS175 Typ (1) | DM54/74 LS174, LS175 Max | DM54/74 S174, S175 Min | DM54/74 S174, S175 Typ (1) | DM54/74 S174, S175 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | DM54 | | | 0.8 | | | 0.8 | | | 0.8 | V |
| | | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | | | | | V |
| | | | | $I_I$ = −18 mA | | | | | | | −1.5 | | | −1.2 | |
| $I_{OH}$ | High Level Output Current | | | | | | | −800 | | | −400 | | | −1000 | µA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.4 | | | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | | DM74 | 2.4 | | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 16 | | | 4 | | | 20 | mA |
| | | | | | DM74 | | | 16 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | | 0.4 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | | DM74 | | | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| | | | | $I_{OL}$ = 4 mA | DM74 | | | | | 0.25 | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | | | | 1 | mA |
| | | | | $V_I$ = 7 V | | | | | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | | | | | µA |
| | | | | $V_I$ = 2.7 V | | | | | | | 20 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | Clock, Clear | $V_{CC}$ = Max | $V_I$ = 0.4 V | | | | −1.6 | | | −0.4 | | | | mA |
| | | Data | | | | | | −1.6 | | | −0.36 | | | | |
| | | Any | | $V_I$ = 0.5 V | | | | | | | | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | DM54 | −20 | | −57 | −20 | | −100 | −40 | | −100 | mA |
| | | | | | DM74 | −18 | | −57 | −20 | | −100 | −40 | | −100 | |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (3) | | LS174, S174 | | 45 | 65 | | 16 | 26 | | 90 | 144 | mA |
| | | | | | LS175, S175 | | 30 | 45 | | 11 | 18 | | 60 | 96 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS and DM54S/74S duration of short circuit should not exceed one second.

**Note 3:** With all outputs open and 4.5 V applied to all data and clear inputs, $I_{CC}$ is measured after a momentary ground, then 4.5 V applied to clock.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | Conditions | DM54/74 174, 175 | | | Conditions | DM54/74 LS174, LS175 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | $C_L$ = 15 pF, $R_L$ = 400 Ω | 30 | 40 | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 30 | 40 | | MHz |
| | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 25 | 35 | | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output From Clear (175 Only) | | | | 14 | 25 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 16 | 25 | ns |
| | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 19 | 29 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Clear | | | | 20 | 30 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 23 | 35 | ns |
| | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 28 | 42 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output From Clock | | | | 14 | 25 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 20 | 30 | ns |
| | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 21 | 32 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Clock | | | | 17 | 25 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 21 | 30 | ns |
| | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 24 | 36 | |
| $t_W$ | Pulse Width | Clock | | 20 | | | | 20 | | | ns |
| | | Clear | | 20 | | | | 20 | | | |
| $t_{SETUP}$ | Setup Time | Data Input | | 20 | | | | 20 | | | ns |
| | | Clear Inactive-State | | 30 | | | | 25 | | | |
| $t_{HOLD}$ | Data Hold Time | | | 0 | | | | 0 | | | ns |

## Switching Characteristics (Continued)

| Parameter | | | Conditions | DM54/74 S174, S175 Min | DM54/74 S174, S175 Typ | DM54/74 S174, S175 Max | Conditions | DM54/74 S174, S175 Min | DM54/74 S174, S175 Typ | DM54/74 S174, S175 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | | $C_L$ = 15 pF, $R_L$ = 280 Ω | 75 | 110 | | $C_L$ = 50 pF, $R_L$ = 280 Ω | 65 | 90 | | MHz |
| $t_{PLH}$ | Propagaton Delay Time, Low-to-High Level Output From Clear (175 Only) | | | | 10 | 15 | | | 12 | 18 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Clear | | | | 13 | 22 | | | 15 | 23 | ns |
| $t_{PLH}$ | Propagaton Delay Time, Low-to-High Level Output From Clock | | | | 8 | 12 | | | 10 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Clock | | | | 11.5 | 17 | | | 13.5 | 21 | ns |
| $t_W$ | Pulse Width | Clock | | 7 | | | | 9 | | | ns |
| | | Clear | | 10 | | | | 12 | | | |
| $t_{SETUP}$ | Setup Time | Data Input | | 5 | | | | 7 | | | ns |
| | | Clear Inactive-State | | 5 | | | | 7 | | | |
| $t_{HOLD}$ | Data Hold Time | | | 3 | | | | 5 | | | ns |

## Truth Table (Each Flip-Flop)

| Inputs | | | Outputs | |
|---|---|---|---|---|
| Clear | Clock | D | Q | $\overline{Q}$† |
| L | X | X | L | H |
| H | ↑ | H | H | L |
| H | ↑ | L | L | H |
| H | L | X | $Q_0$ | $\overline{Q}_0$ |

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care
↑ = Transition from low to high level
$Q_0$ = The level of Q before the indicated steady-state input conditions were established.
† = 175, LS175, and S175 only

# Presettable Decade and Binary Counters

## General Description

These high-speed counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (176, 196) or a divide-by-two and a divide-by-eight counter (177, 197). These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which, when taken low, sets all outputs low regardless of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

### TYPICAL COUNT CONFIGURATIONS 176, 196, LS196, AND S196

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a BCD decade counter, the clock-2 input must be externally connected to the $Q_A$ output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the $Q_D$ output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output $Q_A$ in accordance with the bi-quinary truth table.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the $Q_B$, $Q_C$, and $Q_D$ outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

### 177, 197, LS197, AND S197

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore the counter may be operated in two independent modes:

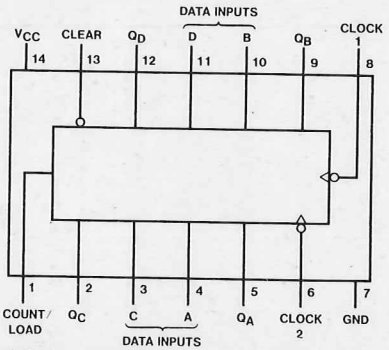
1. When used as a high-speed 4-bit ripple-through counter, output $Q_A$ must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the $Q_A$, $Q_B$, $Q_C$, and $Q_D$ outputs as shown in the truth table.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the $Q_B$, $Q_C$, and $Q_D$ outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

## Features

- Performs BCD, bi-quinary, or binary counting
- Fully programmable
- Fully independent clear input
- Output $Q_A$ maintains full fan-out capability in addition to driving clock-2 input

| Type | Typical Count Frequency | | Typical Power Dissipation |
|---|---|---|---|
| | Clock 1 | Clock 2 | |
| 176, 177 | 50 MHz | 25 MHz | 150 mW |
| 196, 197 | 50 MHz | 25 MHz | 240 mW |
| LS196, LS197 | 40 MHz | 20 MHz | 80 mW |
| S196, S197 | 100 MHz | 50 MHz | 375 mW |

## Connection Diagram




**Note:** Low input to clear sets $Q_A$, $Q_B$, $Q_C$ and $Q_D$ low.

**54176 (J)**
**54177 (J)**
**54196 (J)**
**54LS196 (J,W)**
**54S196 (J,W)**
**54197 (J)**
**54LS197 (J,W)**
**54S197 (J,W)**

**74176 (N)**
**74177 (N)**
**74196 (N)**
**74LS196 (N)**
**74S196 (N)**
**74197 (N)**
**74LS197 (N)**
**74S197 (N)**

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM54/74 176, 177 Min | DM54/74 176, 177 Typ (1) | DM54/74 176, 177 Max | DM54/74 196, 197 Min | DM54/74 196, 197 Typ (1) | DM54/74 196, 197 Max | DM54/74 LS196, LS197 Min | DM54/74 LS196, LS197 Typ (1) | DM54/74 LS196, LS197 Max | DM54/74 S196, S197 Min | DM54/74 S196, S197 Typ (1) | DM54/74 S196, S197 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | DM54 | | | 0.8 | | | 0.8 | | | 0.8 | | | 0.8 | V |
| | | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | | | | | | | V |
| | | | | $I_I$ = −18 mA | | | | | | | | | | −1.5 | | | −1.2 | |
| $I_{OH}$ | High Level Output Current | | | | | | | −800 | | | −800 | | | −400 | | | −1000 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | DM54 | 2.4 | 3.4 | | 2.4 | 3.4 | | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | | DM74 | 2.4 | 3.4 | | 2.4 | 3.4 | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 16 | | | 16 | | | 4 | | | 20 | mA |
| | | | | | DM74 | | | 16 | | | 16 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min (3), $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $I_{OL}$ = 4 mA | | | | | | | | | 0.25 | 0.4 | | | | V |
| | | | | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.25 | 0.4 | | | 0.5 | |
| | | | | $I_{OL}$ = Max | DM74 | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| $I_I$ | Input Current at Maximum Input Voltage | Data, Count/Load | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | | 1 | | | 1 | | | 0.1 | | | 1 | mA |
| | | Clear, Clock 1 | | | | | | 1 | | | 1 | | | 0.2 | | | 1 | |
| | | Clock 2 | | | 176, 196 | | | 1 | | | 1 | | | 0.4 | | | 1 | |
| | | | | | 177, 197 | | | 1 | | | 1 | | | 0.2 | | | 1 | |
| $I_{IH}$ | High Level Input Current | Data, Count/Load | $V_{CC}$ = Max, $V_I$ = 2.4 V, $V_I$ = 2.7 V (LS196, LS197, S196, S197) | | | | | 40 | | | 40 | | | 20 | | | 50 | μA |
| | | Clear, Clock 1 | | | | | | 80 | | | 80 | | | 40 | | | 50 | |
| | | Clock 2 | | | 176, 196 | | | 120 | | | 120 | | | 80 | | | 50 | |
| | | | | | 177, 197 | | | 80 | | | 80 | | | 40 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | Data, Count/Load | $V_{CC}$ = Max, $V_I$ = 0.4 V, $V_I$ = 0.5 V (S196, S197) | | | | | −1.6 | | | −1.6 | | | −0.4 | | | −0.75 | mA |
| | | Clear | | | | | | −3.2 | | | −3.2 | | | −0.8 | | | −0.75 | |
| | | Clock 1 | | | | | | −4.8 | | | −4.8 | | | −2.4 | | | −8 | |
| | | Clock 2 | | | 176, 196 | | | −4.8 | | | −6.4 | | | −2.8 | | | −10 | |
| | | | | | 177, 197 | | | −3.2 | | | −3.2 | | | −1.3 | | | −6 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | DM54 | −20 | | −57 | −20 | | −57 | −20 | | −100 | −40 | | −100 | mA |
| | | | | | DM74 | −18 | | −57 | −18 | | −57 | −20 | | −100 | −40 | | −100 | |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (4) | | | | 30 | 48 | | 39 | 54 | | 16 | 27 | | 75 | 110 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS or DM54S/74S duration of short circuit should not exceed one second.

**Note 3:** $Q_A$ outputs are tested at specified $I_{OL}$ plus the limit value of $I_{IL}$ for the clock-2 input. This permits driving the clock-2 input while maintaining full fan-out capability.

**Note 4:** $I_{CC}$ is measured with all inputs grounded and all outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | To (Output) | Conditions | DM54/74 176, 177 Min | 176, 177 Typ | 176, 177 Max | 196, 197 Min | 196, 197 Typ | 196, 197 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Input Count Frequency | | Clock 1 | $Q_A$ | $C_L$ = 15 pF, $R_L$ = 400 Ω | 35 | 50 | | 40 | 50 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock 1 | $Q_A$ | | | 9 | 13 | | 9 | 13 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 11 | 17 | | 11 | 16 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock 2 | $Q_B$ | | | 12 | 18 | | 12 | 18 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 14 | 21 | | 14 | 21 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock 2 | $Q_C$ | | | 27 | 41 | | 24 | 36 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 34 | 51 | | 28 | 42 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock 2 | $Q_D$ | | | 13 | 20 | | 14 | 21 | ns |
| | | | | | | | 44 | 66 | | 36 | 54 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 17 | 26 | | 16 | 23 | ns |
| | | | | | | | 50 | 75 | | 42 | 63 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | A, B, C, D | $Q_A$, $Q_B$, $Q_C$, $Q_D$ | | | 19 | 29 | | 16 | 24 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 31 | 46 | | 25 | 38 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Load | Any | | | 29 | 43 | | 22 | 33 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 32 | 48 | | 24 | 36 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clear | Any | | | 32 | 48 | | 25 | 37 | ns |
| $t_W$ | Pulse Width | Clock-1 Input | | | | 14 | | | 14 | | | ns |
| | | Clock-2 Input | | | | 28 | | | 28 | | | |
| | | Clear | | | | 25 | | | 25 | | | |
| | | Load | | | | 20 | | | 20 | | | |
| $t_{HOLD}$ | Input Hold Time | High-Level Data | | | | $t_{W(LOAD)}$ | | | $t_{W(LOAD)}$ | | | ns |
| | | Low-Level Data | | | | $t_{W(LOAD)}$ | | | $t_{W(LOAD)}$ | | | |
| $t_{SETUP}$ | Input Setup Time | High-Level Data | | | | 15 | | | 10 | | | ns |
| | | Low-Level Data | | | | 20 | | | 15 | | | |
| $t_{ENABLE}$ | Count Enable Time (5) | | | | | 25 | | | 30 | | | ns |

**Note 5:** Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | To (Output) | | DM54/74 | | | | | | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Conditions | S196 | | | S197 | | | Conditions | S196 | | | S197 | | | |
| | | | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $f_{MAX}$ | Maximum Input Count Frequency | | Clock 1 | $Q_A$ | | $C_L$ = 15 pF, $R_L$ = 280 Ω | 100 | 140 | | 100 | 140 | | $C_L$ = 50 pF, $R_L$ = 280 Ω | 80 | 110 | | 80 | 110 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock 1 | $Q_A$ | | | | 5 | 10 | | 5 | 10 | | | 7 | 11 | | 7 | 11 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | | | 6 | 10 | | 6 | 10 | | | 8 | 12 | | 8 | 12 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock 2 | $Q_B$ | | | | 5 | 10 | | 5 | 10 | | | 7 | 11 | | 7 | 11 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | | 8 | 12 | | 8 | 12 | | | 10 | 15 | | 10 | 15 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock 2 | $Q_C$ | | | | 12 | 18 | | 12 | 18 | | | 14 | 21 | | 14 | 21 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | | 16 | 24 | | 15 | 22 | | | 18 | 27 | | 17 | 26 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock 2 | $Q_D$ | 196 | | | 5 | 10 | | | | | | 7 | 11 | | | | ns |
| | | | | | 197 | | | | | | 18 | 27 | | | | | | 20 | 30 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | 196 | | | 8 | 12 | | | | | | 10 | 15 | | | | ns |
| | | | | | 197 | | | | | | 22 | 33 | | | | | | 25 | 38 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | A, B, C, D | $Q_A$, $Q_B$, $Q_C$, $Q_D$ | | | | 7 | 12 | | 7 | 12 | | | 9 | 14 | | 9 | 14 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | | 12 | 18 | | 12 | 18 | | | 14 | 21 | | 14 | 21 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Load | Any | | | | 10 | 18 | | 10 | 18 | | | 12 | 18 | | 12 | 18 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | | 12 | 18 | | 12 | 18 | | | 14 | 21 | | 14 | 21 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clear | Any | | | | 26 | 37 | | 26 | 37 | | | 30 | 45 | | 30 | 45 | ns |
| $t_W$ | Pulse Width | Clock-1 Input | | | | | 5 | | | 5 | | | | 7 | | | 7 | | | ns |
| | | Clock-2 Input | | | | | 10 | | | 10 | | | | 12 | | | 12 | | | |
| | | Clear | | | | | 30 | | | 30 | | | | 35 | | | 35 | | | |
| | | Load | | | | | 5 | | | 5 | | | | 7 | | | 7 | | | |
| $t_{HOLD}$ | Input Hold Time | High-Level Data | | | | | 3↑ | | | 3↑ | | | | 5↑ | | | 5↑ | | | ns |
| | | Low-Level Data | | | | | 3↑ | | | 3↑ | | | | 5↑ | | | 5↑ | | | |
| $t_{SETUP}$ | Input Setup Time | High-Level Data | | | | | 6↑ | | | 6↑ | | | | 8↑ | | | 8↑ | | | ns |
| | | Low-Level Data | | | | | 6↑ | | | 6↑ | | | | 8↑ | | | 8↑ | | | |
| $t_{ENABLE}$ | Count Enable Time (5) | | | | | | 12 | | | 12 | | | | 14 | | | 14 | | | ns |

**Note 5:** Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

↑ —The arrow indicates that the rising edge of the count/load input is used as reference.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| | Parameter | | From (Input) | To (Output) | DM54/74 | | | | | | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Conditions | LS196 | | | LS197 | | | Conditions | LS196 | | | LS197 | | | |
| | | | | | | Min | Typ | Max | Min | Typ | Max | | Min | Typ | Max | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Input Count Frequency | | Clock 1 | $Q_A$ | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 30 | 40 | | 30 | 40 | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 20 | 30 | | 20 | 30 | | MHz |
| $t_{PLH}$ | Delay Time, Low-to-High Level Output | | Clock 1 | $Q_A$ | | | 8 | 15 | | 8 | 15 | | | 11 | 20 | | 11 | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 13 | 20 | | 14 | 21 | | | 20 | 30 | | 20 | 30 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock 2 | $Q_B$ | | | 10 | 24 | | 12 | 19 | | | 19 | 29 | | 15 | 23 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 22 | 33 | | 15 | 35 | | | 28 | 42 | | 29 | 44 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock 2 | $Q_C$ | | | 22 | 57 | | 22 | 51 | | | 45 | 68 | | 40 | 60 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 22 | 62 | | 25 | 63 | | | 48 | 72 | | 50 | 75 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock 2 | $Q_D$ | | | 12 | 18 | | 30 | 78 | | | 15 | 23 | | 65 | 98 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 12 | 45 | | 35 | 95 | | | 36 | 54 | | 71 | 106 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | A, B, C, D | $Q_A$, $Q_B$ $Q_C$, $Q_D$ | | | 11 | 30 | | 15 | 27 | | | 23 | 35 | | 21 | 32 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 29 | 44 | | 29 | 44 | | | 35 | 53 | | 35 | 53 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Load | Any | | | 27 | 41 | | 20 | 39 | | | 30 | 45 | | 29 | 45 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 30 | 45 | | 30 | 45 | | | 36 | 54 | | 36 | 54 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clear | Any | | | 29 | 51 | | 29 | 51 | | | 40 | 60 | | 40 | 60 | ns |
| $t_W$ | Pulse Width | Clock-1 Input | | | | 20 | | | 20 | | | | 20 | | | 20 | | | ns |
| | | Clock-2 Input | | | | 30 | | | 30 | | | | 30 | | | 30 | | | |
| | | Clear | | | | 15 | | | 15 | | | | 15 | | | 15 | | | |
| | | Load | | | | 20 | | | 20 | | | | 20 | | | 20 | | | |
| $t_{HOLD}$ | Input Hold Time | High-Level Data | | | | 0↑ | | | 0↑ | | | | 0↑ | | | 0↑ | | | ns |
| | | Low-Level Data | | | | 6↑ | | | 6↑ | | | | 6↑ | | | 6↑ | | | |
| $t_{SETUP}$ | Input Setup Time | High-Level Data | | | | 8↑ | | | 8↑ | | | | 8↑ | | | 8↑ | | | ns |
| | | Low-Level Data | | | | 12↑ | | | 12↑ | | | | 12↑ | | | 12↑ | | | |
| $t_{ENABLE}$ | Count Enable Time (5) | | | | | 30 | | | 30 | | | | 30 | | | 30 | | | ns |

**Note 5:** Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.
↑ —The arrow indicates that the rising edge of the count/load input is used as reference.

## Truth Tables

176, 196
LS196, S196
Decade (BCD)
(See Note A)

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

176, 196
LS196, S196
(See Note B)

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_A$ | $Q_D$ | $Q_C$ | $Q_B$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

177, 197
LS197, S197
(See Note A)

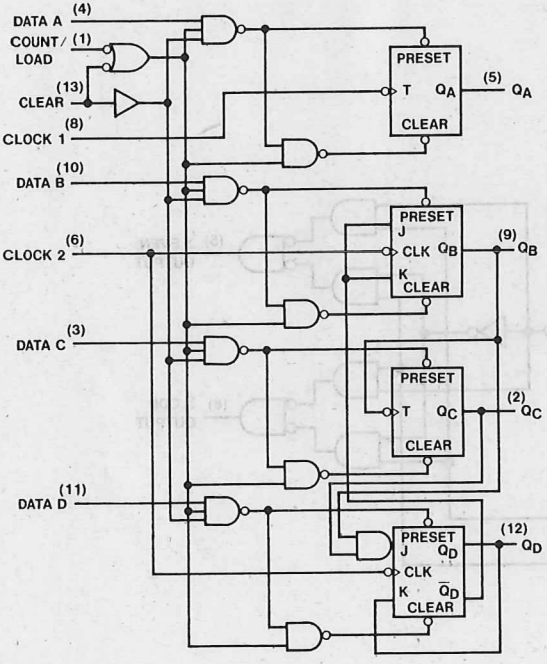
| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

H = High Level, L = Low Level

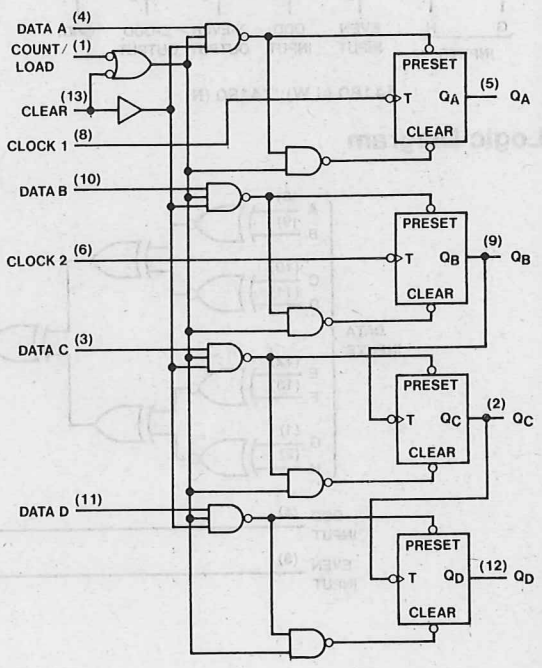
Note A: Output $Q_A$ connected to clock-2 input.
Note B: Output $Q_D$ connected to clock-1 input.

## Logic Diagrams

196
LS196, S196




197
LS197, S197




6

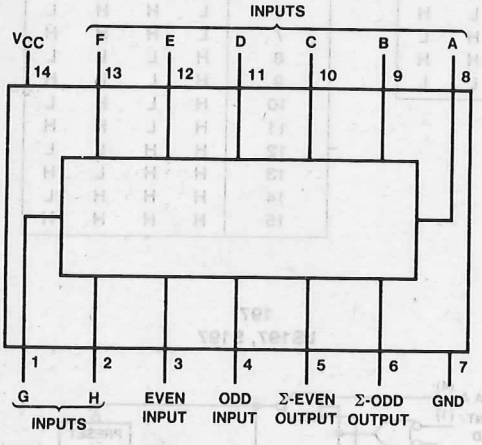
# 9-Bit Parity Generators/Checkers

## General Description

These universal 9-bit (8 data bits plus 1 parity bit) parity generators/checkers feature odd/even outputs and control inputs to facilitate operation in either odd or even parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd inputs can be utilized as the parity or 9th-bit input. The word-length capability is easily expanded by cascading.

Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs at a low logic level. A fan-out to 20 normalized loads is provided at a high logic level to facilitate the connection of unused inputs to used inputs.

## Connection Diagram



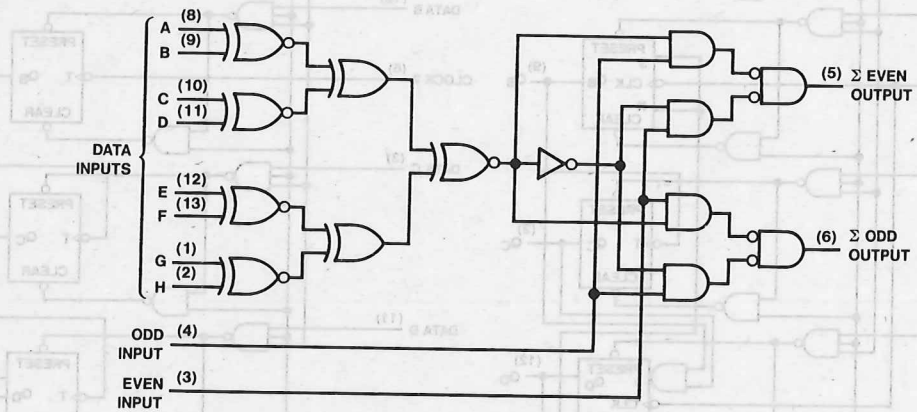

54180 (J,W); 74180 (N)

## Truth Table

| Inputs | | | Outputs | |
|---|---|---|---|---|
| Σ of H's at A thru H | Even | Odd | Σ Even | Σ Odd |
| Even | H | L | H | L |
| Odd | H | L | L | H |
| Even | L | H | L | H |
| Odd | L | H | H | L |
| X | H | H | L | L |
| X | L | L | H | H |

H = High Level, L = Low Level, X = Don't Care

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | DM54/74 180 Min | DM54/74 180 Typ (1) | DM54/74 180 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | | −800 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OH}$ = −800 μA | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | Any Data Input | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | μA |
| | | Even or Odd Input | | | | | 80 | |
| $I_{IL}$ | Low Level Input Current | Any Data Input | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −1.6 | mA |
| | | Even or Odd Input | | | | | −3.2 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | DM54 | −20 | | −55 | mA |
| | | | | DM74 | −18 | | −55 | |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (3) | DM54 | | 34 | 49 | mA |
| | | | | DM74 | | 34 | 56 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time.

**Note 3:** $I_{CC}$ is measured with even and odd inputs at 4.5 V, all other inputs and outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Conditions | DM54/74 180 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Σ Even | CL = 15 pF, RL = 400 Ω Odd Input Grounded | | 40 | 60 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 45 | 68 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Σ Odd | | | 32 | 48 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 25 | 38 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Σ Even | CL = 15 pF, RL = 400 Ω Odd Input Grounded | | 32 | 48 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 25 | 38 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Σ Odd | | | 40 | 60 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 45 | 68 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Even or Odd | Σ Even or Σ Odd | CL = 15 pF, RL = 400 Ω | | 13 | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 7 | 10 | ns |

# Arithmetic Logic Unit/Function Generators

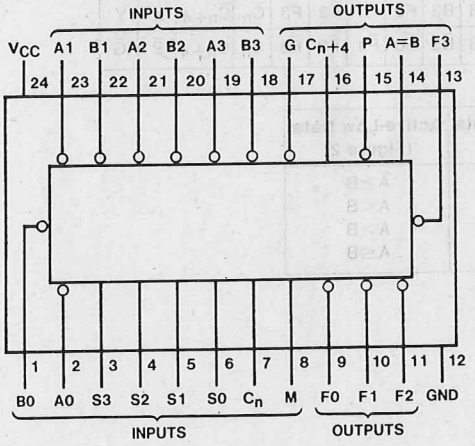
## General Description

These arithmetic logic units (ALU)/function generators perform 16 binary arithmetic operations on two 4-bit words, as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (P and G) for the four bits in the package. When used in conjunction with the DM54S182/DM74S182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown below illustrate how little time is required for addition of longer words, when full carry look-ahead is employed. The method of cascading 182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the DM54S182/DM74S182. (Continued)

## Features

- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - EXCLUSIVE-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Full look-ahead for high-speed operations on long words

## Connection Diagram




**54181 (J)**
**54S181 (J)**

**74181 (N)**
**74S181 (N)**

## Pin Designations

| Designation | Pin Nos. | Function |
|---|---|---|
| A3, A2, A1, A0 | 19, 21, 23, 2 | Word A Inputs |
| B3, B2, B1, B0 | 18, 20, 22, 1 | Word B Inputs |
| S3, S2, S1, S0 | 3, 4, 5, 6 | Function-Select Inputs |
| $C_n$ | 7 | Inv. Carry Input |
| M | 8 | Mode Control Input |
| F3, F2, F1, F0 | 13, 11, 10, 9 | Function Outputs |
| A = B | 14 | Comparator Output |
| P | 15 | Carry Propagate Output |
| $C_{n+4}$ | 16 | Inv. Carry Output |
| G | 17 | Carry Generate Output |
| $V_{CC}$ | 24 | Supply Voltage |
| GND | 12 | Ground |

| Number of Bits | Typical Addition Times | Package Count | | Carry Method Between ALU's |
|---|---|---|---|---|
| | | Arithmetic/ Logic Units | Look Ahead Carry Generators | |
| 1 to 4 | 20 ns | 1 | 0 | None |
| 5 to 8 | 30 ns | 2 | 0 | Ripple |
| 9 to 16 | 30 ns | 3 or 4 | 1 | Full Look-Ahead |
| 17 to 64 | 50 ns | 5 to 16 | 2 to 5 | Full Look-Ahead |

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## General Description (Continued)

If high speed is not important, a ripple-carry input ($C_n$) and a ripple-carry output ($C_{n+4}$) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1, which requires an end-around or forced carry to provide A—B.

The 181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with $C_n$ = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output ($C_{n+4}$) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

### ALU SIGNAL DESIGNATIONS

The DM54181/DM74181 and DM54S181/DM74S181 can be used with the signal designations of either *Figure 1* or *Figure 2*.

The logic functions and arithmetic operations obtained with signal designations as in *Figure 1* are given in Table 1; those obtained with the signal designations of *Figure 2* are given in Table 2.

| Pin Number | 2 | 1 | 23 | 22 | 21 | 20 | 19 | 18 | 9 | 10 | 11 | 13 | 7 | 16 | 15 | 17 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Active-High Data (Table I) | A0 | B0 | A1 | B1 | A2 | B2 | A3 | B3 | F0 | F1 | F2 | F3 | $\overline{C}_n$ | $\overline{C}_{n+4}$ | X | Y |
| Active-Low Data (Table II) | $\overline{A}$0 | $\overline{B}$0 | $\overline{A}$1 | $\overline{B}$1 | $\overline{A}$2 | $\overline{B}$2 | $\overline{A}$3 | $\overline{B}$3 | $\overline{F}$0 | $\overline{F}$1 | $\overline{F}$2 | $\overline{F}$3 | $C_n$ | $C_{n+4}$ | $\overline{P}$ | $\overline{G}$ |

| Input $C_n$ | Output $C_{n+4}$ | Active-High Data (Figure 1) | Active-Low Data (Figure 2) |
|---|---|---|---|
| H | H | A≤B | A≥B |
| H | L | A>B | A<B |
| L | H | A<B | A>B |
| L | L | A≥B | A≤B |

## General Description (Continued)

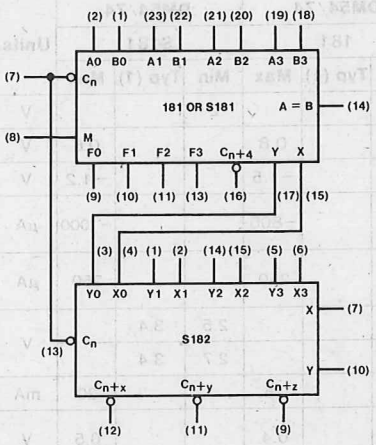



Figure 1

Table 1

| Selection | | | | Active High Data | | |
|---|---|---|---|---|---|---|
| | | | | M = H | M = L; Arithmetic Operations | |
| S3 | S2 | S1 | S0 | Logic Functions | $C_n$ = H (no carry) | $C_n$ = L (with carry) |
| L | L | L | L | $F = \overline{A}$ | F = A | F = A Plus 1 |
| L | L | L | H | $F = \overline{A + B}$ | F = A + B | F = (A + B) Plus 1 |
| L | L | H | L | $F = \overline{A}B$ | F = A + $\overline{B}$ | F = (A + $\overline{B}$) Plus 1 |
| L | L | H | H | F = 0 | F = Minus 1 (2's Compl) | F = Zero |
| L | H | L | L | $F = \overline{AB}$ | F = A Plus A$\overline{B}$ | F = A Plus A$\overline{B}$ Plus 1 |
| L | H | L | H | $F = \overline{B}$ | F = (A + B) Plus A$\overline{B}$ | F = (A + B) Plus A$\overline{B}$ Plus 1 |
| L | H | H | L | $F = A \oplus B$ | F = A Minus B Minus 1 | F = A Minus B |
| L | H | H | H | F = A$\overline{B}$ | F = A$\overline{B}$ Minus 1 | F = A$\overline{B}$ |
| H | L | L | L | $F = \overline{A} + B$ | F = A Plus AB | F = A Plus AB Plus 1 |
| H | L | L | H | $F = \overline{A \oplus B}$ | F = A Plus B | F = A Plus B Plus 1 |
| H | L | H | L | F = B | F = (A + $\overline{B}$) Plus AB | F = (A + $\overline{B}$) Plus AB Plus 1 |
| H | L | H | H | F = AB | F = AB Minus 1 | F = AB |
| H | H | L | L | F = 1 | F = A Plus A* | F = A Plus A Plus 1 |
| H | H | L | H | F = A + $\overline{B}$ | F = (A + B) Plus A | F = (A + B) Plus A Plus 1 |
| H | H | H | L | F = A + B | F = (A + $\overline{B}$) Plus A | F = (A + $\overline{B}$) Plus A Plus 1 |
| H | H | H | H | F = A | F = A Minus 1 | F = A |

*Each bit is shifted to the next more significant position.

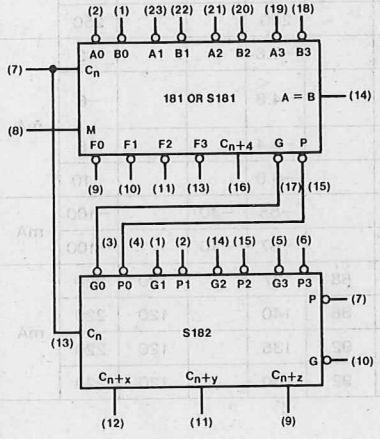



Figure 2

Table 2

| Selection | | | | Active Low Data | | |
|---|---|---|---|---|---|---|
| | | | | M = H | M = L; Arithmetic Operations | |
| S3 | S2 | S1 | S0 | Logic Functions | $C_n$ = L (no carry) | $C_n$ = H (with carry) |
| L | L | L | L | $F = \overline{A}$ | F = A Minus 1 | F = A |
| L | L | L | H | $F = \overline{AB}$ | F = AB Minus 1 | F = AB |
| L | L | H | L | $F = \overline{A} + B$ | F = A$\overline{B}$ Minus 1 | F = A$\overline{B}$ |
| L | L | H | H | F = 1 | F = Minus 1 (2's Compl) | F = Zero |
| L | H | L | L | $F = \overline{A + B}$ | F = A Plus (A + $\overline{B}$) | F = A Plus (A + $\overline{B}$) Plus 1 |
| L | H | L | H | $F = \overline{B}$ | F = AB Plus (A + B) | F = AB Plus (A + $\overline{B}$) Plus 1 |
| L | H | H | L | $F = \overline{A + B}$ | F = A Minus B Minus 1 | F = A Minus B |
| L | H | H | H | F = A + $\overline{B}$ | F = A + $\overline{B}$ | F = (A + $\overline{B}$) Plus 1 |
| H | L | L | L | F = $\overline{A}$B | F = A Plus (A + B) | F = A Plus (A + B) Plus 1 |
| H | L | L | H | F = A + B | F = A Plus B | F = A Plus B Plus 1 |
| H | L | H | L | F = B | F = A$\overline{B}$ Plus (A + B) | F = A$\overline{B}$ Plus (A + B) Plus 1 |
| H | L | H | H | F = A + B | F = A + B | F = (A + B) Plus 1 |
| H | H | L | L | F = 0 | F = A Plus A* | F = A Plus A Plus 1 |
| H | H | L | H | F = A$\overline{B}$ | F = AB Plus A | F = AB Plus A Plus 1 |
| H | H | H | L | F = AB | F = A$\overline{B}$ Plus A | F = A$\overline{B}$ Plus A Plus 1 |
| H | H | H | H | F = A | F = A | F = A Plus 1 |

*Each bit is shifted to the next more significant position.

6

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM54/74 181 Min | DM54/74 181 Typ (1) | DM54/74 181 Max | DM54/74 S181 Min | DM54/74 S181 Typ (1) | DM54/74 S181 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | | −1.5 | | | −1.2 | V |
| $I_{OH}$ | High Level Output Current (Any Output Except A = B) | | | | | | | −800 | | | −1000 | μA |
| $I_{OH}$ | High Level Output Current (A = B Output Only) | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $V_{OH}$ = 5.5 V | | | | | 250 | | | 250 | μA |
| $V_{OH}$ | High Level Output Voltage (Any Output Except A = B) | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | DM54 | 2.4 | | | 2.5 | 3.4 | | V |
| | | | | | DM74 | 2.4 | | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | | | | 16 | | | 20 | mA |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = Max | | | | | 0.4 | | | 0.5 | V |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | Mode Input | $V_{CC}$ = Max, $V_I$ = 2.4 V, $V_I$ = 2.5 V (S181) | | | | | 40 | | | 50 | μA |
| | | Any A or B Input | | | | | | 120 | | | 150 | |
| | | Any S Input | | | | | | 160 | | | 200 | |
| | | Carry Input | | | | | | 200 | | | 250 | |
| $I_{IL}$ | Low Level Input Current | Mode Input | $V_{CC}$ = Max, $V_I$ = 0.4 V, $V_I$ = 0.5 V (S181) | | | | | −1.6 | | | −2 | mA |
| | | Any A or B Input | | | | | | −4.8 | | | −6 | |
| | | Any S Input | | | | | | −6.4 | | | −8 | |
| | | Carry Input | | | | | | −8.0 | | | −10 | |
| $I_{OS}$ | Short Circuit Output Current (Any Output Except A = B) | | $V_{CC}$ = Max (2) | | DM54 | −20 | | −55 | −40 | | −100 | mA |
| | | | | | DM74 | −18 | | −57 | −40 | | −100 | |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (3) | Condition A | DM54 | | 88 | 127 | | 120 | 220 | mA |
| | | | | | DM74 | | 88 | 140 | | 120 | 220 | |
| | | | | Condition B | DM54 | | 92 | 135 | | 120 | 220 | |
| | | | | | DM74 | | 92 | 150 | | 120 | 220 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time and for S181 duration should not exceed one second.

**Note 3:** With outputs open, $I_{CC}$ is measured for the following conditions:

A. S0 through S3, M, and A inputs are at 4.5 V, all other inputs are grounded, and all outputs are open.

B. S0 through S3 and M are at 4.5 V, all other inputs are grounded, and all outputs are open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Conditions | DM54/74 181 $R_L$ = 400 Ω, $C_L$ = 15 pF | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $C_n$ | $C_{n+4}$ | | | 9 | 18 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 13 | 19 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any A or B | $C_{n+4}$ | M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode) | | 20 | 30 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 22 | 33 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any A or B | $C_{n+4}$ | M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode) | | 20 | 30 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 22 | 33 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $C_n$ | Any F | M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode) | | 11 | 19 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 12 | 18 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any A or B | G | M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode) | | 13 | 19 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 14 | 19 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any A or B | G | M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode) | | 12 | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 15 | 25 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any A or B | P | M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode) | | 12 | 19 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 17 | 25 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any A or B | P | M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode) | | 14 | 25 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 17 | 25 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $A_i$ or $B_i$ | $F_i$ | M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode) | | 18 | 30 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 19 | 30 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $A_i$ or $B_i$ | $F_i$ | M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode) | | 14 | 24 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 14 | 24 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $A_i$ or $B_i$ | $F_i$ | M = 4.5 V (logic mode) | | 17 | 28 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 19 | 30 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any A or B | A = B | M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode) | | 26 | 40 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 25 | 40 | |

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## Switching Characteristics (Continued) $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Conditions | DM54/74 S181 | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | $R_L$ = 280 Ω, $C_L$ = 15 pF | | | $R_L$ = 280 Ω, $C_L$ = 50 pF | | | |
| | | | | | Min | Typ | Max | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $C_n$ | $C_{n+4}$ | | | 7 | 10.5 | | 9 | 14 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 7 | 10.5 | | 9 | 14 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any A or B | $C_{n+4}$ | M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode) | | 12.5 | 18.5 | | 14.5 | 22 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 12.5 | 18.5 | | 14.5 | 22 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any A or B | $C_{n+4}$ | M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode) | | 15.5 | 23 | | 17.5 | 27 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 15.5 | 23 | | 17.5 | 27 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $C_n$ | Any F | M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode) | | 7 | 12 | | 9 | 14 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 7 | 12 | | 9 | 14 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any A or B | G | M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode) | | 8 | 12 | | 10 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 7.5 | 12 | | 10 | 15 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any A or B | G | M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode) | | 10.5 | 15 | | 12.5 | 19 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 10.5 | 15 | | 13 | 20 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any A or B | P | M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode) | | 7.5 | 12 | | 9.5 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 7.5 | 12 | | 10 | 15 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any A or B | P | M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode) | | 10.5 | 15 | | 12.5 | 19 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 10.5 | 15 | | 13 | 20 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $A_i$ or $B_i$ | $F_i$ | M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode) | | 11 | 16.5 | | 13 | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 11 | 16.5 | | 13 | 20 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $A_i$ or $B_i$ | $F_i$ | M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode) | | 14 | 20 | | 16 | 24 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 14 | 22 | | 16 | 24 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $A_i$ or $B_i$ | $F_i$ | M = 4.5 V (logic mode) | | 14 | 20 | | 16 | 24 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 14 | 22 | | 16 | 24 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any A or B | A = B | M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode) | | 15 | 23 | | 17 | 26 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 20 | 30 | | 22 | 33 | |

## Parameter Measurement Information

**Logic Mode Test Table**
**Function Inputs: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V**

| Parameter | Input Under Test | Other Input Same Bit | | Other Data Inputs | | Output Under Test | Output Waveform |
|---|---|---|---|---|---|---|---|
| | | Apply 4.5 V | Apply GND | Apply 4.5 V | Apply GND | | |
| $t_{PLH}$ | $A_i$ | $B_i$ | None | None | Remaining A and B, $C_n$ | $F_i$ | Out-of-Phase |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | $B_i$ | $A_i$ | None | None | Remaining A and B, $C_n$ | $F_i$ | Out-of-Phase |
| $t_{PHL}$ | | | | | | | |

**$\overline{SUM}$ Mode Test Table**
**Function Inputs: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V**

| Parameter | Input Under Test | Other Input Same Bit | | Other Data Inputs | | Output Under Test | Output Waveform |
|---|---|---|---|---|---|---|---|
| | | Apply 4.5 V | Apply GND | Apply 4.5 V | Apply GND | | |
| $t_{PLH}$ | $A_i$ | $B_i$ | None | Remaining A and B | $C_n$ | $F_i$ | In-Phase |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | $B_i$ | $A_i$ | None | Remaining A and B | $C_n$ | $F_i$ | In-Phase |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | $A_i$ | $B_i$ | None | None | Remaining A and B, $C_n$ | P | In-Phase |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | $B_i$ | $A_i$ | None | None | Remaining A and B, $C_n$ | P | In-Phase |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | $A_i$ | None | $B_i$ | Remaining B | Remaining A, $C_n$ | G | In-Phase |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | $B_i$ | None | $A_i$ | Remaining B | Remaining A, $C_n$ | G | In-Phase |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | $C_n$ | None | None | All A | All B | Any F or $C_{n+4}$ | In-Phase |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | $A_i$ | None | $B_i$ | Remaining B | Remaining A, $C_n$ | $C_{n+4}$ | Out-of-Phase |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | $B_i$ | None | $A_i$ | Remaining B | Remaining A, $C_n$ | $C_{n+4}$ | Out-of-Phase |
| $t_{PHL}$ | | | | | | | |

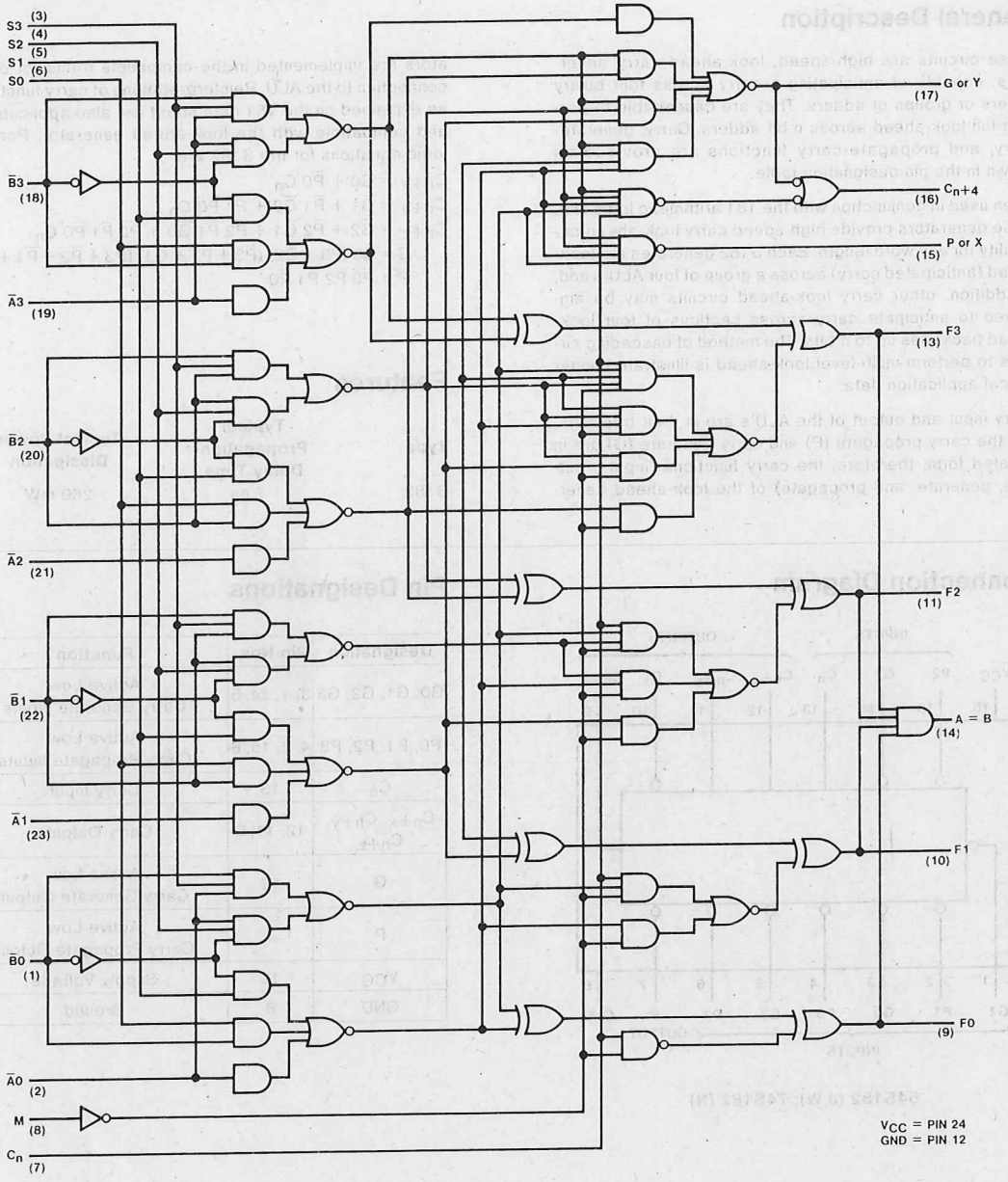
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## Parameter Measurement Information (Continued)

**$\overline{\text{DIFF}}$ Mode Test Table**
**Function Inputs: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V**

| Parameter | Input Under Test | Other Input Same Bit | | Other Data Inputs | | Output Under Test | Output Waveform |
|---|---|---|---|---|---|---|---|
| | | Apply 4.5 V | Apply GND | Apply 4.5 V | Apply GND | | |
| $t_{PLH}$ / $t_{PHL}$ | $A_i$ | None | $B_i$ | Remaining A | Remaining B, $C_n$ | $F_i$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $B_i$ | $A_i$ | None | Remaining A | Remaining B, $C_n$ | $F_i$ | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $A_i$ | None | $B_i$ | None | Remaining A and B, $C_n$ | P | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $B_i$ | $A_i$ | None | None | Remaining A and B, $C_n$ | P | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $A_i$ | $B_i$ | None | None | Remaining A and B, $C_n$ | G | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $B_i$ | None | $A_i$ | None | Remaining A and B, $C_n$ | G | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $A_i$ | None | $B_i$ | Remaining A | Remaining B, $C_n$ | A = B | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $B_i$ | $A_i$ | None | Remaining A | Remaining B, $C_n$ | A = B | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $C_n$ | None | None | All A and B | None | $C_{n+4}$ or any F | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $A_i$ | $B_i$ | None | None | Remaining A, B, $C_n$ | $C_{n+4}$ | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $B_i$ | None | $A_i$ | None | Remaining A, B, $C_n$ | $C_{n+4}$ | In-Phase |

## Logic Diagram



# Look-Ahead Carry Generators

## General Description

These circuits are high-speed, look-ahead carry generators, capable of anticipating a carry across four binary adders or groups of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the 181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each S182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the S182 are:

$C_{n+x} = \overline{G}0 + \overline{P}0\, C_n$

$C_{n+y} = \overline{G}1 + \overline{P}1\,\overline{G}0 + \overline{P}1\,\overline{P}0\, C_n$

$C_{n+z} = \overline{G}2 + \overline{P}2\,\overline{G}1 + \overline{P}2\,\overline{P}1\,\overline{G}0 + \overline{P}2\,\overline{P}1\,\overline{P}0\, C_n$

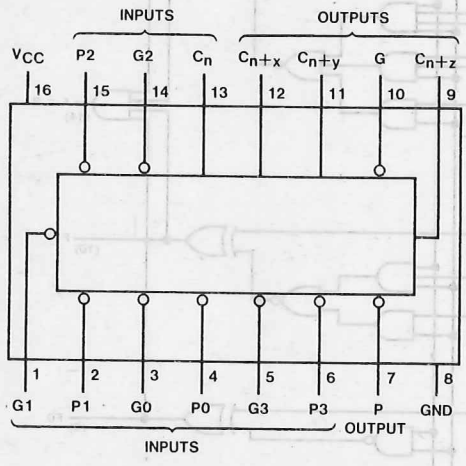
$\overline{G} = \overline{G}3\,(\overline{P}3 + \overline{G}2)\,(\overline{P}3 + \overline{P}2 + \overline{G}1)\,(\overline{P}3 + \overline{P}2 + \overline{P}1 + \overline{G}0)$

$\overline{P} = \overline{P}3\,\overline{P}2\,\overline{P}1\,\overline{P}0$

## Features

| Type | Typical Propagation Delay Time | Typical Power Dissipation |
|---|---|---|
| S182 | 7 ns | 260 mW |

## Connection Diagram




54S182 (J,W); 74S182 (N)

## Pin Designations

| Designation | Pin Nos. | Function |
|---|---|---|
| G0, G1, G2, G3 | 3, 1, 14, 5 | Active Low Carry Generate Inputs |
| P0, P1, P2, P3 | 4, 2, 15, 6 | Active Low Carry Propagate Inputs |
| $C_n$ | 13 | Carry Input |
| $C_{n+x}$, $C_{n+y}$, $C_{n+z}$ | 12, 11, 9 | Carry Outputs |
| G | 10 | Active Low Carry Generate Output |
| P | 7 | Active Low Carry Propagate Output |
| $V_{CC}$ | 16 | Supply Voltage |
| GND | 8 | Ground |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | DM54/74 S182 Min | DM54/74 S182 Typ (1) | DM54/74 S182 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | −1.2 | V |
| $I_{OH}$ | High Level Output Current | | | | | | −1000 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | DM54 | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | | | 20 | mA |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = Max | | | | 0.5 | V |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $C_n$ Input | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | 50 | μA |
| | | P3 Input | | | | | 100 | |
| | | P2 Input | | | | | 150 | |
| | | P0, P1, or G3 Input | | | | | 200 | |
| | | G0 or G2 Input | | | | | 350 | |
| | | G1 input | | | | | 400 | |
| $I_{IL}$ | Low Level Input Current | $C_n$ Input | $V_{CC}$ = Max, $V_I$ = 0.5 V | | | | −2 | mA |
| | | P3 Input | | | | | −4 | |
| | | P2 Input | | | | | −6 | |
| | | P0, P1, or G3 Input | | | | | −8 | |
| | | G0 or G2 Input | | | | | −14 | |
| | | G1 Input | | | | | −16 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | −40 | | −100 | mA |
| $I_{CCH}$ | Supply Current, All Outputs High | | $V_{CC}$ = 5 V (3) | | | 35 | | mA |
| $I_{CCL}$ | Supply Current, All Outputs Low | | $V_{CC}$ = Max (4) | DM54 | | 69 | 99 | mA |
| | | | | DM74 | | 69 | 109 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

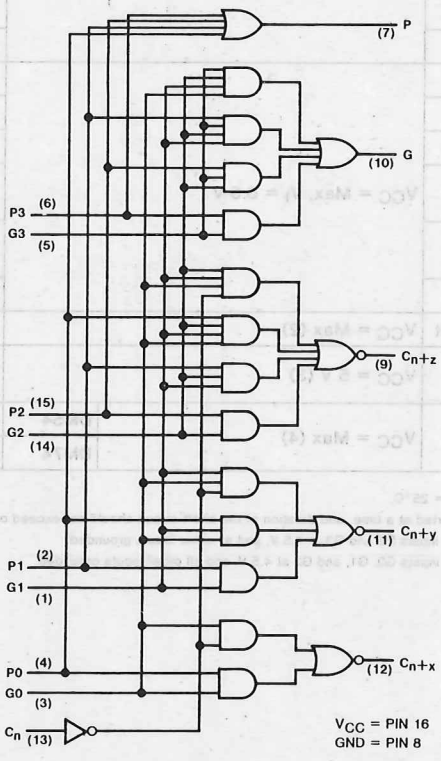
**Note 3:** $I_{CCH}$ is measured with all outputs open, inputs P3 and G3 at 4.5 V, and all other inputs grounded.

**Note 4:** $I_{CCL}$ is measured with all outputs open; inputs G0, G1, and G2 at 4.5 V, and all other inputs grounded.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

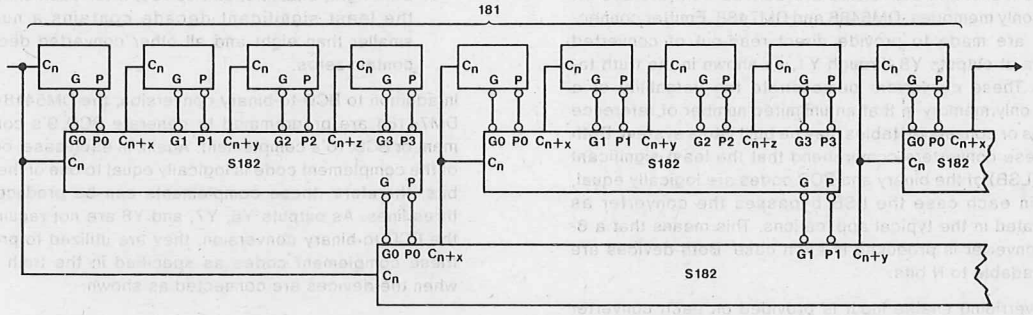
| Parameter | | From (Input) | To (Output) | DM54/74 S182 | | | | DM54/74 S182 | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | G0, G1 G2, G3, P0, P1, P2, or P3 | $C_{n+x}$, $C_{n+y}$, or $C_{n+z}$ | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 4.5 | 7 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 6.5 | 10 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 4.5 | 7 | | | 7 | 11 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | G0, G1 G2, G3, P1, P2, or P3 | G | | | 5 | 7.5 | | | 7 | 11 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 7 | 10.5 | | | 9 | 14 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | P0, P1, P2, or P3 | P | | | 4.5 | 6.5 | | | 6.5 | 10 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 6.5 | 10 | | | 9 | 14 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $C_n$ | $C_{n+x}$, $C_{n+y}$, or $C_{n+z}$ | | | 6.5 | 10 | | | 8.5 | 13 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 7 | 10.5 | | | 9 | 14 | |

## Logic Diagram



## Typical Application

64-BIT ALU, FULL-CARRY LOOK AHEAD IN THREE LEVELS




A and B inputs, and F outputs of 181 are not shown.

# BCD-to-Binary and Binary-to-BCD Converters

## General Description

These monolithic converters are derived from the 256-bit read only memories, DM5488 and DM7488. Emitter connections are made to provide direct read-out of converted codes at outputs Y8 through Y1, as shown in the truth tables. These converters demonstrate the versatility of a read only memory in that an unlimited number of reference tables or conversion tables may be built into a system. Both of these converters comprehend that the least significant bits (LSB) of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter as illustrated in the typical applications. This means that a 6-bit converter is produced in each case. Both devices are cascadable to N bits.

An overriding enable input is provided on each converter which when taken high inhibits the function, causing all outputs to go high. For this reason, and to minimize power consumption, unused outputs Y7 and Y8 of the 185A and all "don't care" conditions of the 184 are programmed high. The outputs are of the open-collector type.

### DM54184 AND DM74184 BCD-TO-BINARY CONVERTERS

The 6-bit BCD-to-binary function of the DM54184 and DM74184 is analogous to the algorithm:

a. Shift BCD number right one bit and examine each decade. Subtract three from each 4-bit decade containing a binary value greater than seven.

b. Shift right, examine, and correct after each shift until the least significant decade contains a number smaller than eight and all other converted decades contain zeros.

In addition to BCD-to-binary conversion, the DM54184 and DM74184 are programmed to generate BCD 9's complement or BCD 10's complement. Again, in each case, one bit of the complement code is logically equal to one of the BCD bits; therefore, these complements can be produced on three lines. As outputs Y6, Y7, and Y8 are not required in the BCD-to-binary conversion, they are utilized to provide these complement codes as specified in the truth table when the devices are connected as shown.

### DM54185A AND DM74185A BINARY-TO-BCD CONVERTERS

The function performed by these 6-bit binary-to-BCD converters is analogous to the algorithm:

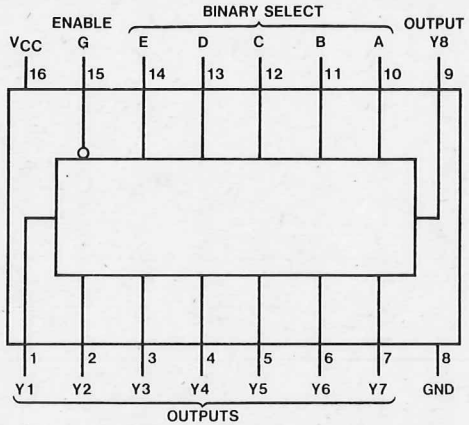
a. Examine the three most significant bits. If the sum is greater than four, add three and shift left one bit.

b. Examine each BCD decade. If the sum is greater than four, add three and shift left one bit.

c. Repeat step b until the least-significant binary bit is in the least-significant BCD location.

(Continued)

## Connection Diagram




54184 (J,W)
54185A (J,W)

74184 (N)
74185A (N)

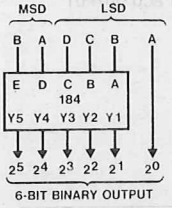
## General Description (Continued)

DM54184 AND DM74184 BCD-TO-BINARY

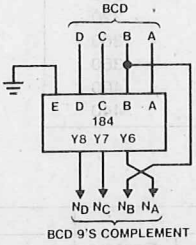
TABLE 1
PACKAGE COUNT AND DELAY TIMES
FOR BCD-TO-BINARY CONVERSION

| Input (Decades) | Packages Required | Total Delay Times (ns) | |
|---|---|---|---|
| | | Typ | Max |
| 2 | 2 | 56 | 80 |
| 3 | 6 | 140 | 200 |
| 4 | 11 | 196 | 280 |
| 5 | 19 | 280 | 400 |
| 6 | 28 | 364 | 520 |

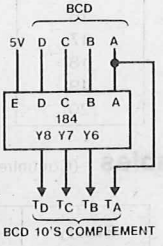
6-Bit Converter




BCD 9's Complement Converter




BCD's 10's Complement Converter




## Truth Tables

BCD-TO-BINARY CONVERTER

| BCD WORDS | | Inputs (See Note A) | | | | | | Outputs (See Note B) | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | E | D | C | B | A | G | Y5 | Y4 | Y3 | Y2 | Y1 |
| 0 | 1 | L | L | L | L | L | L | L | L | L | L | L |
| 2 | 3 | L | L | L | L | H | L | L | L | L | L | H |
| 4 | 5 | L | L | L | H | L | L | L | L | L | H | L |
| 6 | 7 | L | L | L | H | H | L | L | L | L | H | H |
| 8 | 9 | L | L | H | L | L | L | L | L | H | L | L |
| 10 | 11 | L | H | L | L | L | L | L | L | H | L | H |
| 12 | 13 | L | H | L | L | H | L | L | L | H | H | L |
| 14 | 15 | L | H | L | H | L | L | L | L | H | H | H |
| 16 | 17 | L | H | L | H | H | L | L | H | L | L | L |
| 18 | 19 | L | H | H | L | L | L | L | H | L | L | H |
| 20 | 21 | H | L | L | L | L | L | L | H | L | H | L |
| 22 | 23 | H | L | L | L | H | L | L | H | L | H | H |
| 24 | 25 | H | L | L | H | L | L | L | H | H | L | L |
| 26 | 27 | H | L | L | H | H | L | L | H | H | L | H |
| 28 | 29 | H | L | H | L | L | L | L | H | H | H | L |
| 30 | 31 | H | H | L | L | L | L | L | H | H | H | H |
| 32 | 33 | H | H | L | L | H | L | H | L | L | L | L |
| 34 | 35 | H | H | L | H | L | L | H | L | L | L | H |
| 36 | 37 | H | H | L | H | H | L | H | L | L | H | L |
| 38 | 39 | H | H | H | L | L | L | H | L | L | H | H |
| ANY | | X | X | X | X | X | H | H | H | H | H | H |

BCD 9'S OR BCD 10'S COMPLEMENT CONVERTER

| BCD WORD | Inputs (See Note C) | | | | | | Outputs (See Note D) | | |
|---|---|---|---|---|---|---|---|---|---|
| | E† | D | C | B | A | G | Y8 | Y7 | Y6 |
| 0 | L | L | L | L | L | L | H | L | H |
| 1 | L | L | L | L | H | L | H | L | L |
| 2 | L | L | L | H | L | L | L | H | H |
| 3 | L | L | L | H | H | L | L | H | L |
| 4 | L | L | H | L | L | L | L | H | H |
| 5 | L | L | H | L | H | L | L | H | L |
| 6 | L | L | H | H | L | L | L | L | H |
| 7 | L | L | H | H | H | L | L | L | L |
| 8 | L | H | L | L | L | L | L | L | H |
| 9 | L | H | L | L | H | L | L | L | L |
| 0 | H | L | L | L | L | L | L | L | L |
| 1 | H | L | L | L | H | L | H | L | L |
| 2 | H | L | L | H | L | L | H | L | L |
| 3 | H | L | L | H | H | L | L | H | H |
| 4 | H | L | H | L | L | L | L | H | H |
| 5 | H | L | H | L | H | L | L | H | L |
| 6 | H | L | H | H | L | L | L | H | L |
| 7 | H | L | H | H | H | L | L | L | H |
| 8 | H | H | L | L | L | L | L | L | H |
| 9 | H | H | L | L | H | L | L | L | L |
| ANY | X | X | X | X | X | H | H | H | H |

H = High Level, L = Low Level, X = Don't Care

**Note A:** Input Conditions other than those shown produce highs at outputs Y1 through Y5.

**Note B:** Output Y6, Y7, and Y8 are not used for BCD-to-binary conversion.

**Note C:** Input conditions other than those shown produce highs at outputs Y6, Y7, and Y8.

**Note D:** Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.

†When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated; when it is high, the BCD 10's complement is generated.

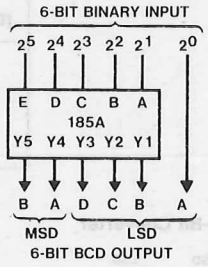
## General Description (Continued)

### DM54185A AND DM74185A BINARY-TO-BCD

TABLE II
PACKAGE COUNT AND DELAY TIMES
FOR BINARY-TO-BCD CONVERSION

| Input (Bits) | Packages Required | Total Delay Times (ns) | |
|---|---|---|---|
| | | Typ | Max |
| 4 to 6 | 1 | 25 | 40 |
| 7 or 8 | 3 | 50 | 80 |
| 9 | 4 | 75 | 120 |
| 10 | 6 | 100 | 160 |
| 11 | 7 | 125 | 200 |
| 12 | 8 | 125 | 200 |
| 13 | 10 | 150 | 240 |
| 14 | 12 | 175 | 280 |
| 15 | 14 | 175 | 280 |
| 16 | 16 | 200 | 320 |
| 17 | 19 | 225 | 360 |
| 18 | 21 | 225 | 360 |
| 19 | 24 | 250 | 400 |
| 20 | 27 | 275 | 440 |

**6-Bit Converter**




## Truth Tables (Continued)

| Binary Words | | Inputs | | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Binary Select | | | | | Enable | | | | | | | | |
| | | E | D | C | B | A | G | Y8 | Y7 | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 |
| 0 | 1 | L | L | L | L | L | L | H | H | L | L | L | L | L | L |
| 2 | 3 | L | L | L | L | H | L | H | H | L | L | L | L | L | H |
| 4 | 5 | L | L | L | H | L | L | H | H | L | L | L | L | H | L |
| 6 | 7 | L | L | L | H | H | L | H | H | L | L | L | L | H | H |
| 8 | 9 | L | L | H | L | L | L | H | H | L | L | L | H | L | L |
| 10 | 11 | L | L | H | L | H | L | H | H | L | L | H | L | L | L |
| 12 | 13 | L | L | H | H | L | L | H | H | L | L | H | L | L | H |
| 14 | 15 | L | L | H | H | H | L | H | H | L | L | H | L | H | L |
| 16 | 17 | L | H | L | L | L | L | H | H | L | L | H | L | H | H |
| 18 | 19 | L | H | L | L | H | L | H | H | L | L | H | H | L | L |
| 20 | 21 | L | H | L | H | L | L | H | H | L | H | L | L | L | L |
| 22 | 23 | L | H | L | H | H | L | H | H | L | H | L | L | L | H |
| 24 | 25 | L | H | H | L | L | L | H | H | L | H | L | L | H | L |
| 26 | 27 | L | H | H | L | H | L | H | H | L | H | L | L | H | H |
| 28 | 29 | L | H | H | H | L | L | H | H | L | H | L | H | L | L |
| 30 | 31 | L | H | H | H | H | L | H | H | L | H | H | L | L | L |
| 32 | 33 | H | L | L | L | L | L | H | H | L | H | H | L | L | H |
| 34 | 35 | H | L | L | L | H | L | H | H | L | H | H | L | H | L |
| 36 | 37 | H | L | L | H | L | L | H | H | L | H | H | L | H | H |
| 38 | 39 | H | L | L | H | H | L | H | H | L | H | H | H | L | L |
| 40 | 41 | H | L | H | L | L | L | H | H | H | L | L | L | L | L |
| 42 | 42 | H | L | H | L | H | L | H | H | H | L | L | L | L | H |
| 44 | 45 | H | L | H | H | L | L | H | H | H | L | L | L | H | L |
| 46 | 47 | H | L | H | H | H | L | H | H | H | L | L | L | H | H |
| 48 | 49 | H | H | L | L | L | L | H | H | H | L | L | H | L | L |
| 50 | 51 | H | H | L | L | H | L | H | H | H | L | H | L | L | L |
| 52 | 53 | H | H | L | H | L | L | H | H | H | L | H | L | L | H |
| 54 | 55 | H | H | L | H | H | L | H | H | H | L | H | L | H | L |
| 56 | 57 | H | H | H | L | L | L | H | H | H | L | H | L | H | H |
| 58 | 59 | H | H | H | L | H | L | H | H | H | L | H | H | L | L |
| 60 | 61 | H | H | H | H | L | L | H | H | H | H | L | L | L | L |
| 62 | 63 | H | H | H | H | H | L | H | H | H | H | L | L | L | H |
| ALL | | X | X | X | X | X | H | H | H | H | H | H | H | H | H |

H = High Level, L = Low Level, X = Don't Care

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | DM54/74 184, 185A | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $V_{OH}$ = 5.5 V | | | 100 | μA |
| $I_{OL}$ | Low Level Output Current | | | | 12 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 12 mA | | | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | 25 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | −1 | mA |
| $I_{CCH}$ | Supply Current, All Outputs High | $V_{CC}$ = Max | | 40 | 65 | mA |
| $I_{CCL}$ | Supply Current, All Programmed Outputs Low | $V_{CC}$ = Max | | 50 | 80 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output From Enable G | $C_L$ = 15 pF<br>$R_{L1}$ = 400 Ω<br>$R_{L2}$ = 600 Ω | | 20 | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output from Enable G | | | 20 | 35 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output From Binary Select | | | 20 | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Binary Select | | | 20 | 35 | ns |

6

## Typical Applications

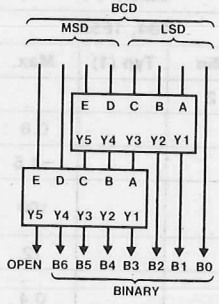



**FIGURE 1. BCD-to-Binary Converter For Two BCD Decades**

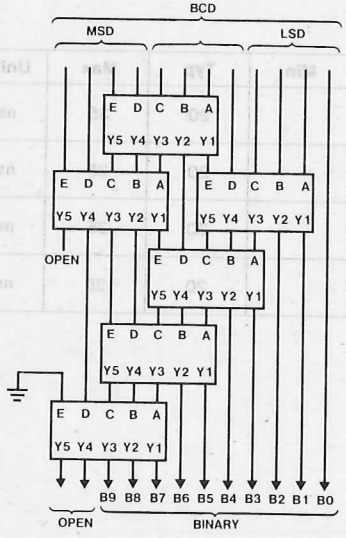



**FIGURE 2. BCD-to-Binary Converter For Three BCD Decades**

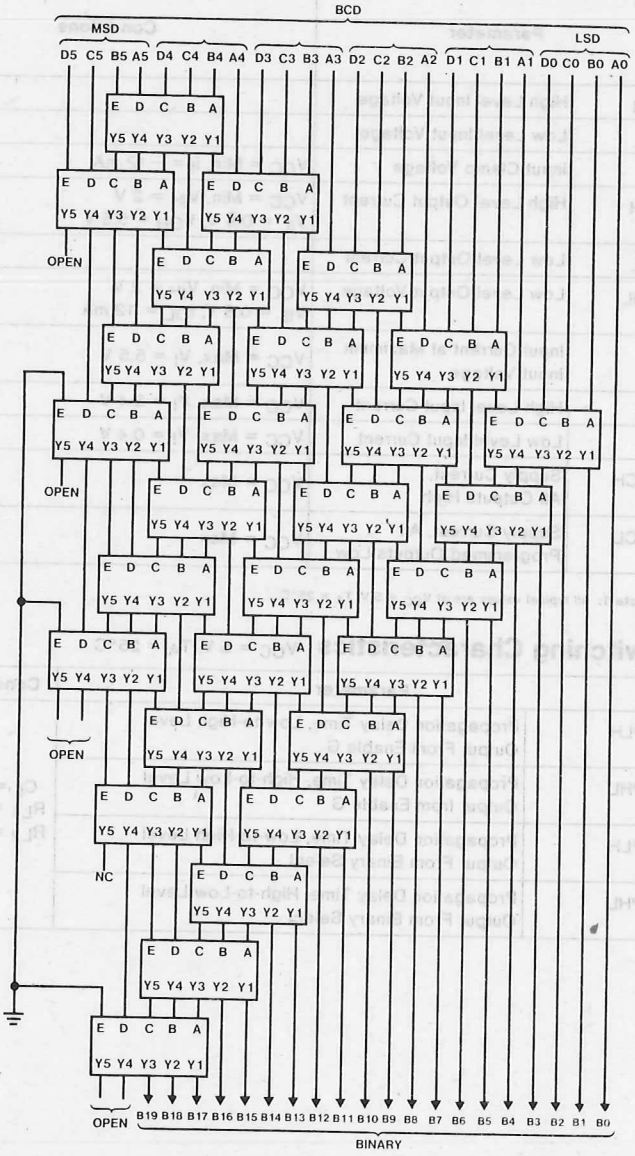



**FIGURE 3. BCD-to-Binary Converter For Six BCD Decades**

MSD—Most significant decade
LSD—Least significant decade
Each rectangle represents a DM54184 or DM74184

## Typical Applications (Continued)

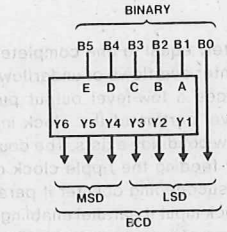



FIGURE 4. 6-Bit Binary-to-BCD Converter

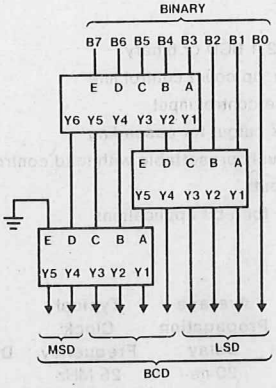



FIGURE 5. 8-Bit Binary-to-BCD Converter

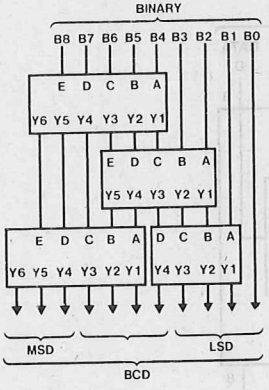



FIGURE 6. 9-Bit Binary-to-BCD Converter

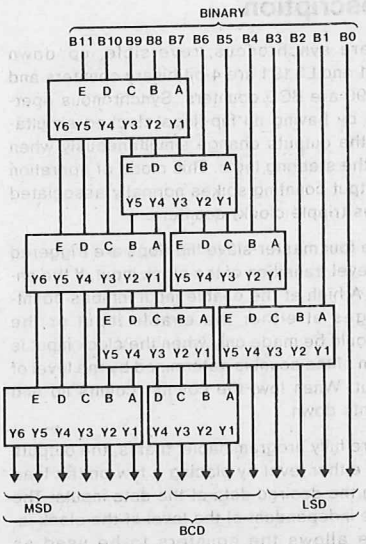



FIGURE 7. 12-Bit Binary-to-BCD Converter (See Note B)

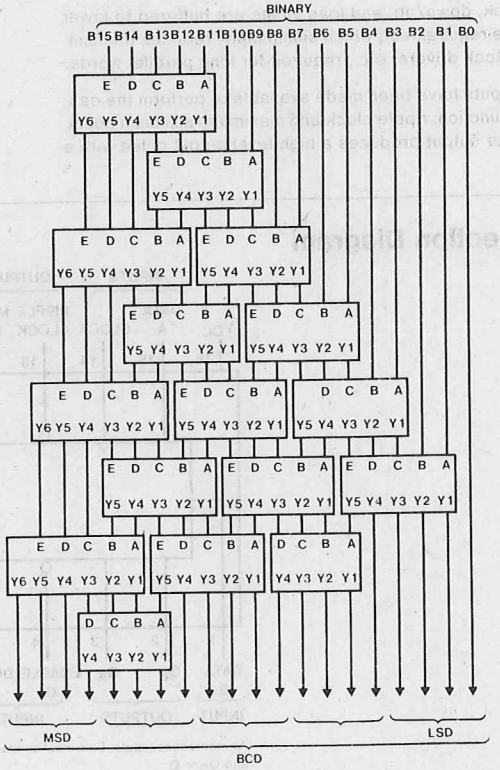



FIGURE 8. 16-Bit Binary-to-BCD Converter (See Note B)

MSD—Most significant decade
LSD—Least significant decade

**Note A:** Each rectangle represents a DM54185A or a DM74185A.
**Note B:** All unused E inputs are grounded.

# Synchronous Up/Down Counters with Mode Control

## General Description

These circuits are synchronous, reversible, up/down counters. The 191 and LS191 are 4-bit binary counters and the 190 and LS190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement; which significantly reduces the number of clock drivers, etc., required for long parallel words.

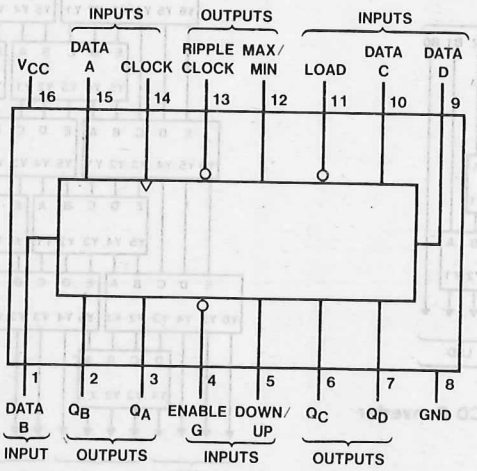
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

## Features

- Counts 8-4-2-1 BCD or binary
- Single down/up count control line
- Count enable control input
- Ripple clock output for cascading
- Asynchronously presettable with load control
- Parallel outputs
- Cascadable for n-bit applications

| Type | Average Propagation Delay | Typical Clock Frequency | Typical Power Dissipation |
|---|---|---|---|
| 190, 191 | 20 ns | 25 MHz | 325 mW |
| LS190, LS191 | 20 ns | 25 MHz | 100 mW |

## Connection Diagram




Asynchronous inputs: Low input to load sets $Q_A$ = A, $Q_B$ = B, $Q_C$ = C, and $Q_D$ = D

| | |
|---|---|
| 54190 (J,W) | 74190 (N) |
| 54LS190 (J,W) | 74LS190 (N) |
| 54191 (J,W) | 74191 (N) |
| 54LS191 (J,W) | 74LS191 (N) |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM54/74 190, 191 | | | DM54/74 LS190, LS191 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | DM54 | | | 0.8 | | | 0.8 | V |
| | | | | | DM74 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | | V |
| | | | | $I_I$ = −18 mA | | | | | | | −1.5 | |
| $I_{OH}$ | High Level Output Current | | | | | | | −800 | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | DM54 | 2.4 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | | DM74 | 2.4 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 16 | | | 4 | mA |
| | | | | | DM74 | | | 16 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | 0.25 | 0.4 | V |
| | | | | | DM74 | | 0.2 | 0.4 | | 0.35 | 0.5 | |
| | | | | $I_{OL}$ = 4 mA | DM74 | | | | | 0.25 | 0.4 | |
| $I_I$ | Input Current at Maximum Input Voltage | Enable | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | | mA |
| | | | | $V_I$ = 7 V | | | | | | | 0.3 | |
| | | Others | | $V_I$ = 5.5 V | | | | 1 | | | | |
| | | | | $V_I$ = 7 V | | | | | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | Enable | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 120 | | | | μA |
| | | | | $V_I$ = 2.7 V | | | | | | | 60 | |
| | | Others | | $V_I$ = 2.4 V | | | | 40 | | | | |
| | | | | $V_I$ = 2.7 V | | | | | | | 20 | |
| $I_{IL}$ | Low Level Input Current | Enable | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | | −4.8 | | | −1.08 | mA |
| | | Others | | | | | | −1.6 | | | −0.4 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | DM54 | −20 | | −65 | −20 | | −100 | mA |
| | | | | | DM74 | −18 | | −65 | −20 | | −100 | |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (3) | | DM54 | | 65 | 99 | | 20 | 35 | mA |
| | | | | | DM74 | | 65 | 105 | | 20 | 35 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

**Note 3:** $I_{CC}$ is measured with all inputs grounded and all outputs open.

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## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Conditions | DM54/74 190, 191 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | | $C_L$ = 15 pF, $R_L$ = 400 Ω | 20 | 25 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Load | $Q_A$, $Q_B$ $Q_C$, $Q_D$ | | | 22 | 33 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 33 | 50 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data A, B, C, D | $Q_A$, $Q_B$ $Q_C$, $Q_D$ | | | 14 | 22 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 35 | 50 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Clock | Ripple Clock | | | 13 | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 16 | 24 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Clock | $Q_A$, $Q_B$ $Q_C$, $Q_D$ | | | 16 | 24 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 24 | 36 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Clock | Max/Min | | | 28 | 42 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 37 | 52 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Down/Up | Ripple Clock | | | 30 | 45 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 30 | 45 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Down/Up | Max/Min | | | 21 | 33 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 22 | 33 | |
| $t_{W(CLOCK)}$ | Width of Clock Input Pulse | | | | 25 | | | ns |
| $t_{W(LOAD)}$ | Width of Load Input Pulse | | | | 35 | | | ns |
| $t_{SETUP}$ | Data Setup Time | | | | 20 | | | ns |
| $t_{HOLD}$ | Data Hold Time | | | | 0 | | | ns |

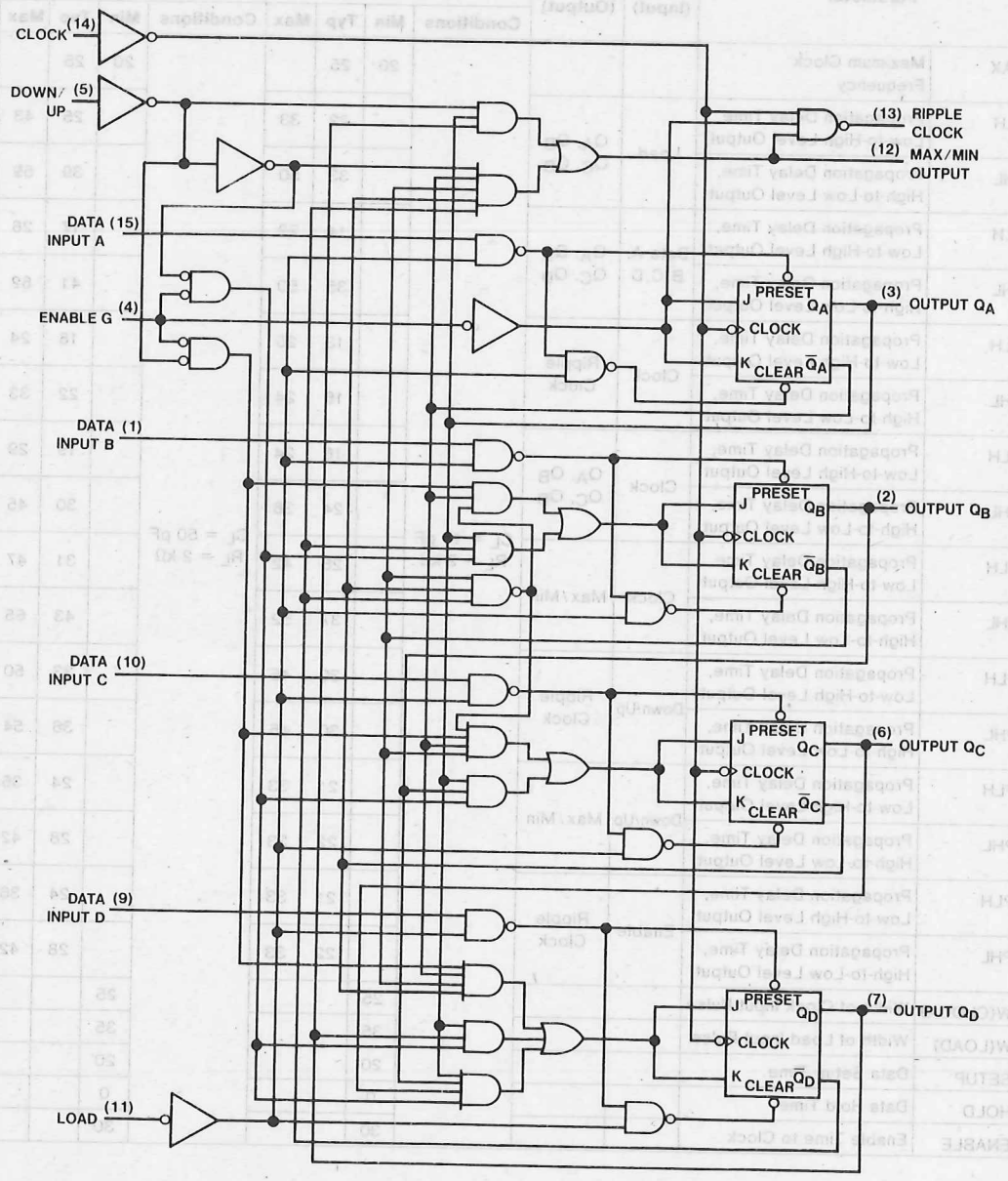
## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | DM54/74 LS190, LS191 | | | | DM54/74 LS190, LS191 | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 20 | 25 | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 20 | 25 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Load | $Q_A$, $Q_B$ $Q_C$, $Q_D$ | | | 22 | 33 | | | 25 | 43 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 33 | 50 | | | 39 | 59 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data A, B, C, D | $Q_A$, $Q_B$ $Q_C$, $Q_D$ | | | 14 | 22 | | | 17 | 26 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 35 | 50 | | | 41 | 62 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Clock | Ripple Clock | | | 13 | 20 | | | 16 | 24 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 16 | 24 | | | 22 | 33 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Clock | $Q_A$, $Q_B$ $Q_C$, $Q_D$ | | | 16 | 24 | | | 19 | 29 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 24 | 36 | | | 30 | 45 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Clock | Max/Min | | | 28 | 42 | | | 31 | 47 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 37 | 52 | | | 43 | 65 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Down/Up | Ripple Clock | | | 30 | 45 | | | 33 | 50 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 30 | 45 | | | 36 | 54 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Down/Up | Max/Min | | | 21 | 33 | | | 24 | 36 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 22 | 33 | | | 28 | 42 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Enable | Ripple Clock | | | 21 | 33 | | | 24 | 36 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 22 | 33 | | | 28 | 42 | |
| $t_{W(CLOCK)}$ | Width of Clock Input Pulse | | | | 25 | | | | 25 | | | ns |
| $t_{W(LOAD)}$ | Width of Load Input Pulse | | | | 35 | | | | 35 | | | ns |
| $t_{SETUP}$ | Data Setup Time | | | | 20 | | | | 20 | | | ns |
| $t_{HOLD}$ | Data Hold Time | | | | 0 | | | | 0 | | | ns |
| $t_{ENABLE}$ | Enable Time to Clock | | | | 30 | | | | 30 | | | ns |

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## Logic Diagrams

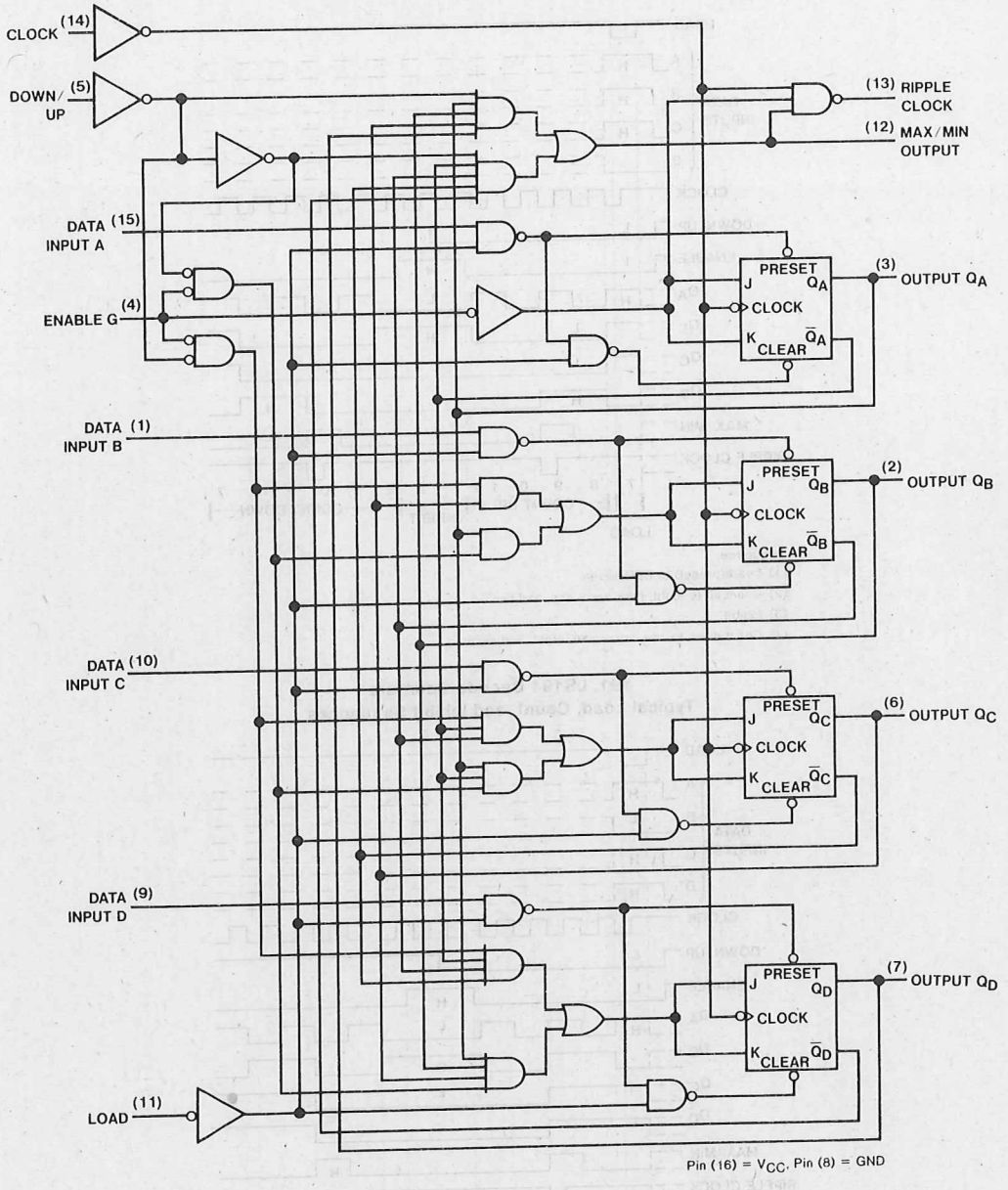
190, LS190 Decade Counters




Pin (16) = $V_{CC}$, Pin (8) = GND

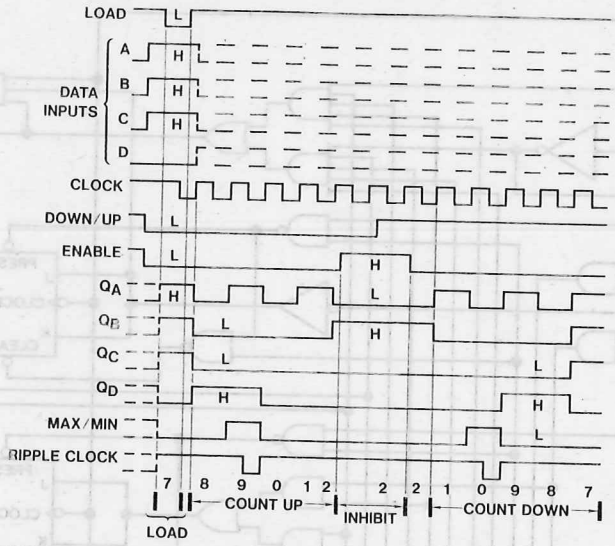
## Logic Diagrams (Continued)

191, LS191 Binary Counters



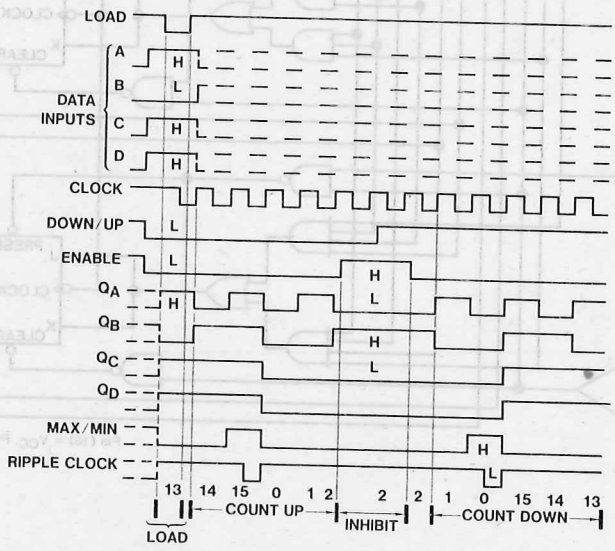
## Timing Diagrams

### 190, LS190 Decade Counters
### Typical Load, Count, and Inhibit Sequences




**Sequence:**
(1) Load (preset) to BCD seven
(2) Count up to eight, nine, zero, one, and two
(3) Inhibit
(4) Count down to one, zero, nine, eight, and seven

### 191, LS191 Decode Counters
### Typical Load, Count, and Inhibit Sequences




**Sequence:**
(1) Load (preset) to binary thirteen
(2) Count up to fourteen, fifteen, zero, one, and two
(3) Inhibit
(4) Count down to one, zero, fifteen, fourteen, and thirteen

# Synchronous Up/Down Counters with Dual Clock

## General Description

These circuits are synchronous up/down counters; the 192, L192 and LS192 circuits are BCD counters and the 193, L193 and LS193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed, while the other count input is held high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

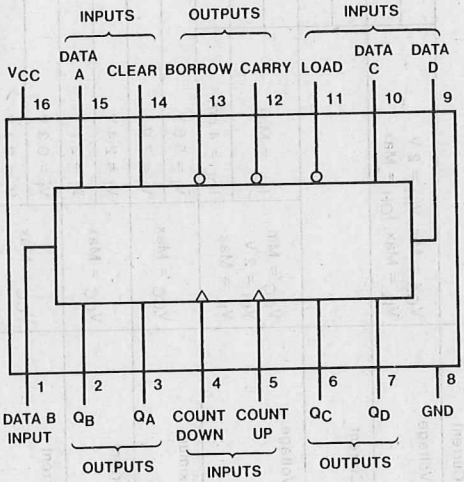
These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

## Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset each flip-flop

| Type | Typical Count Frequency | Typical Power Dissipation |
|---|---|---|
| 192, 193 | 25 MHz | 325 mW |
| L192, L193 | 12 MHz | 40 mW |
| LS192, LS193 | 32 MHz | 95 mW |

## Connection Diagram




Note: Low input to load sets $Q_A$ = A, $Q_B$ = B, $Q_C$ = C, and $Q_D$ = D.

**54192 (J,W)**
**54L192 (J,W)**
**54LS192 (J,W)**
**54193 (J,W)**
**54L193 (J,W)**
**54LS193 (J,W)**

**74192 (N)**
**74L192 (N)**
**74LS192 (N)**
**74193 (N)**
**74L193 (N)**
**74LS193 (N)**

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 192, 193 | | | DM54/74 L192, L193 | | | DM54/74 LS192, LS193 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.7 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.7 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | N/A | | | | V |
| | | | $I_I$ = −18 mA | | | | | | | N/A | | | −1.5 | |
| $I_{OH}$ | High Level Output Current | | | | | | −400 | | | −200 | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | DM54 | 2.4 | | | 2.4 | | | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.4 | | | 2.4 | | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | | | 2 | | | 4 | mA |
| | | | | DM74 | | | 16 | | | 3.6 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | | 0.4 | | 0.15 | 0.3 | | 0.25 | 0.4 | V |
| | | | | DM74 | | | 0.4 | | 0.2 | 0.4 | | 0.35 | 0.5 | |
| | | | $I_{OL}$ = 4 mA | DM74 | | | | | | | | 0.25 | 0.4 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | 0.1 | | | | mA |
| | | | $V_I$ = 7 V | | | | | | | | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | <1 | 10 | | | | μA |
| | | | $V_I$ = 2.7 V | | | | | | | | | | 20 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | | −0.10 | −0.18 | | | | mA |
| | | | $V_I$ = 0.4 V | | | | −1.6 | | | | | | −0.4 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −20 | | −55 | −3 | −9 | −15 | −20 | | −100 | mA |
| | | | | DM74 | −18 | | −55 | −3 | −9 | −15 | −20 | | −100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | DM54 | | 65 | 89 | | 8 | 13 | | 19 | 34 | mA |
| | | | | DM74 | | 65 | 102 | | 8 | 13 | | 19 | 34 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

**Note 3:** $I_{CC}$ is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | DM54/74 192, 193 | | | | DM54/74 L192, L193 | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | | $C_L$ = 15 pF, $R_L$ = 400 Ω | 20 | 25 | | $C_L$ = 50 pF, $R_L$ = 4 kΩ | 6 | 8 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Count up | Carry | | | 17 | 26 | | | 30 | 60 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 16 | 24 | | | 60 | 120 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Count down | Borrow | | | 16 | 24 | | | 30 | 60 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 16 | 24 | | | 50 | 100 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Either Count | Q | | | 25 | 38 | | | 45 | 90 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 31 | 47 | | | 75 | 150 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Load | Q | | | 27 | 40 | | | 55 | 110 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 29 | 40 | | | 105 | 200 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Clear | Q | | | 22 | 35 | | | 95 | 190 | ns |
| $t_W$ | Width of Any Input Pulse | | | | 25 | | | | 70 | | | ns |
| $t_{SETUP}$ | Data Setup Time | | | | 20 | | | | 30 | | | ns |
| $t_{HOLD}$ | Data Hold Time | | | | 0 | | | | 0 | | | ns |

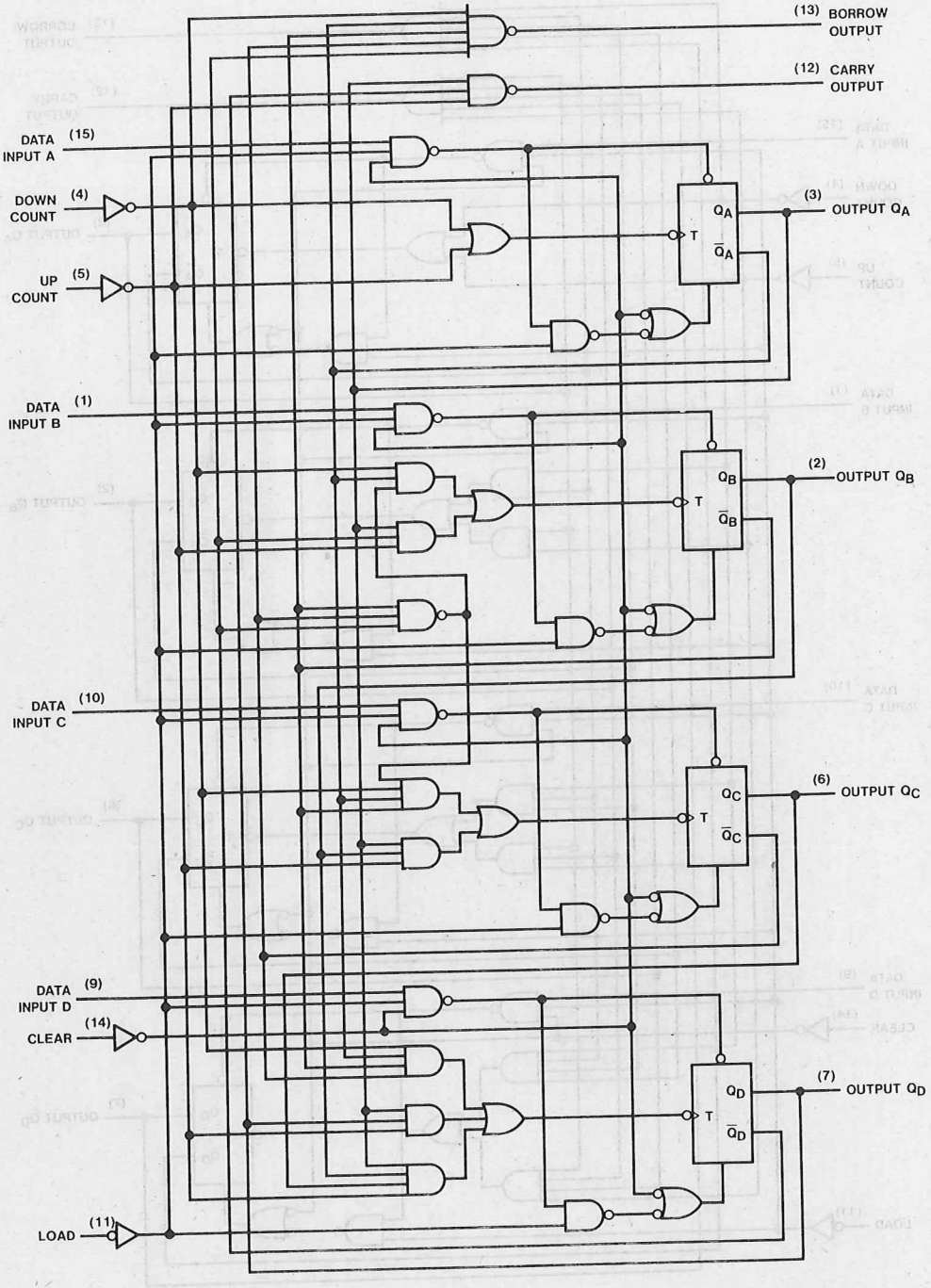
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## Switching Characteristics (Continued)

| Parameter | | From (Input) | To (Output) | DM54/74 LS192, LS193 | | | | DM54/74 LS192, LS193 | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 25 | 32 | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 20 | 25 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Count up | Carry | | | 17 | 26 | | | 20 | 30 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 18 | 24 | | | 24 | 36 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Count down | Borrow | | | 16 | 24 | | | 19 | 29 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 15 | 24 | | | 21 | 32 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Either Count | Q | | | 27 | 38 | | | 30 | 45 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 30 | 47 | | | 36 | 54 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Load | Q | | | 24 | 40 | | | 27 | 41 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 25 | 40 | | | 31 | 47 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Clear | Q | | | 23 | 35 | | | 29 | 44 | ns |
| $t_W$ | Width of Any Input Pulse | | | | 20 | | | | 20 | | | ns |
| $t_{SETUP}$ | Data Setup Time | | | | 20 | | | | 20 | | | ns |
| $t_{HOLD}$ | Data Hold Time | | | | 0 | | | | 0 | | | ns |
| | Clear Inactive Setup Time | | | | 40 | | | | 40 | | | ns |

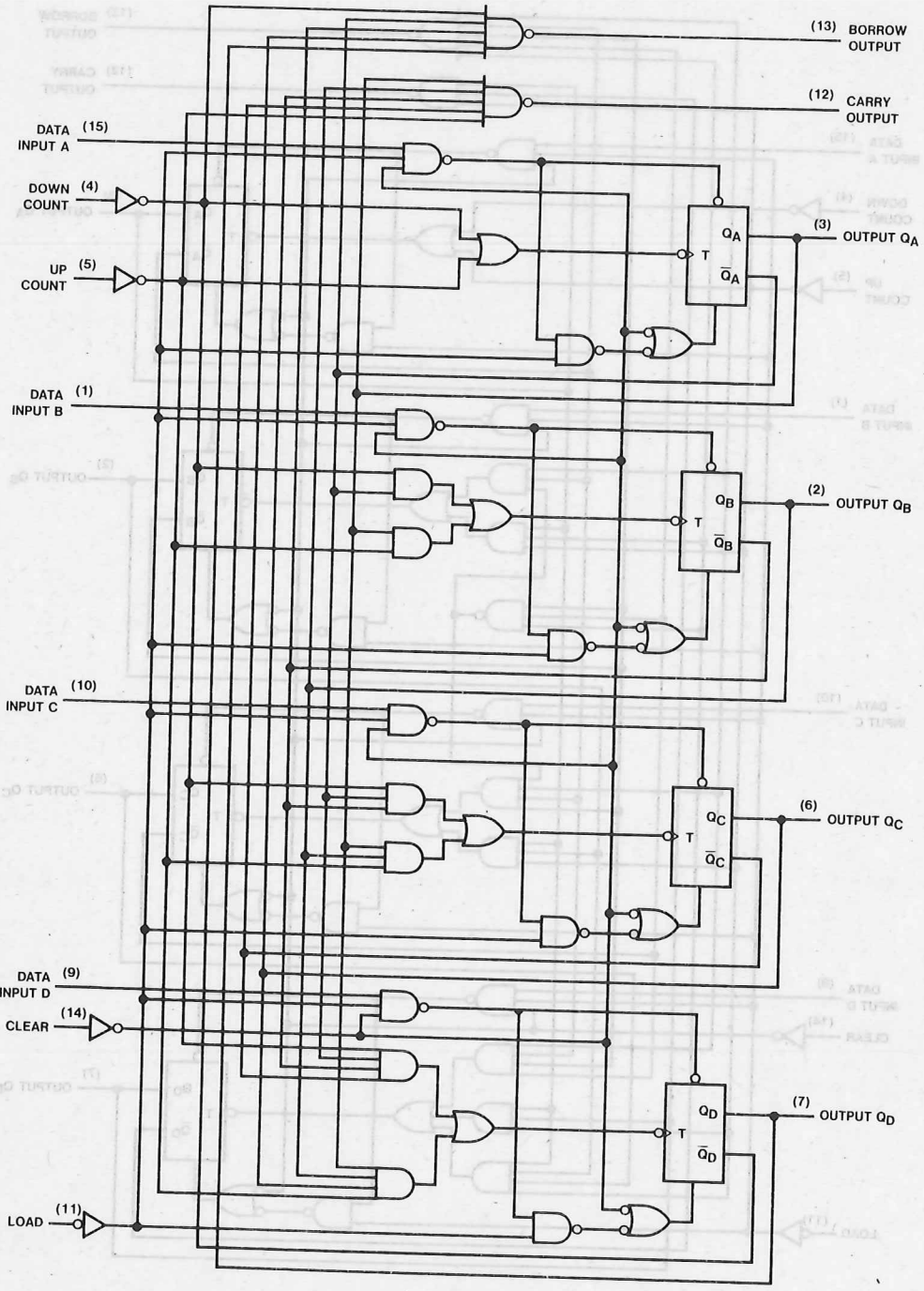
## Logic Diagrams

192, L192, LS192



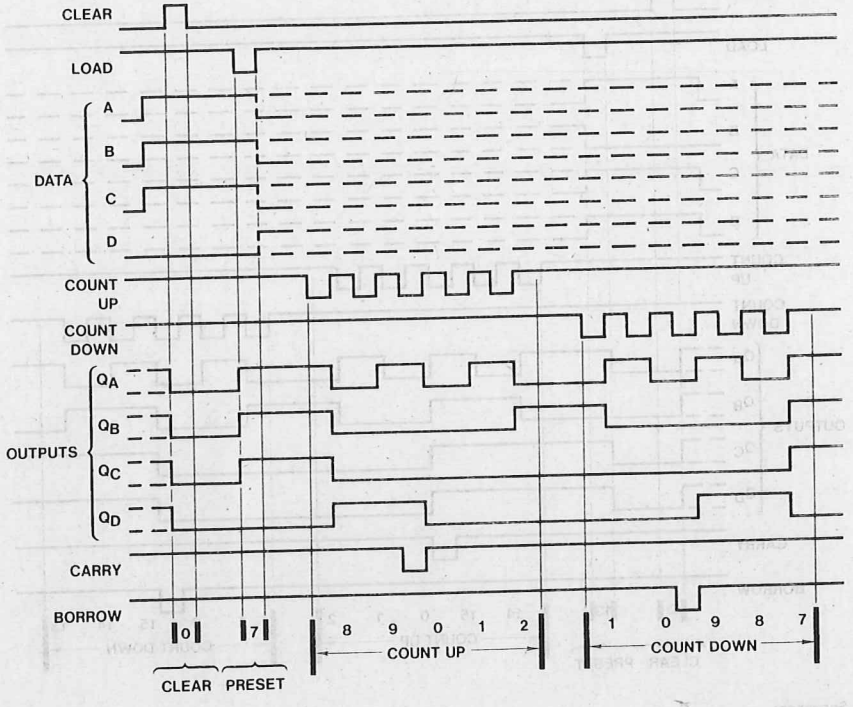
## Logic Diagrams (Continued)

193, L193, LS193



## Timing Diagrams

192, L192, LS192 DECADE COUNTERS
TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

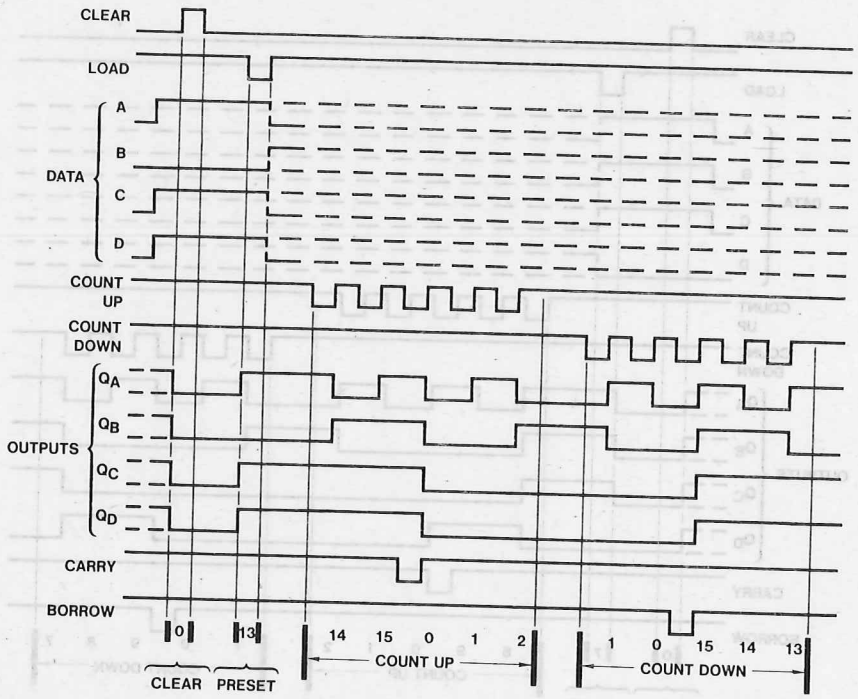



**Sequence:**
(1) Clear outputs to zero.
(2) Load (preset) to BCD seven.
(3) Count up to eight, nine, carry, zero, one, and two.
(4) Count down to one, zero, borrow, nine, eight, and seven.

**Note A:** Clear overrides load, data, and count inputs.
**Note B:** When counting up, count-down input must be high; when counting down, count-up input must be high.

## Timing Diagrams (Continued)

193, L193, LS193 BINARY COUNTERS
TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES




**Sequence:**
(1) Clear outputs to zero.
(2) Load (preset) to binary thirteen.
(3) Count up to fourteen, fifteen, carry, zero, one, and two.
(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

**Note A:** Clear overrides load, data, and count inputs.

**Note B:** When counting up, count-down input must be high; when counting down, count-up input must be high.

# 4-Bit Bidirectional Universal Shift Registers

## General Description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction $Q_A$ toward $Q_D$)
Shift left (in the direction $Q_D$ toward $Q_A$)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

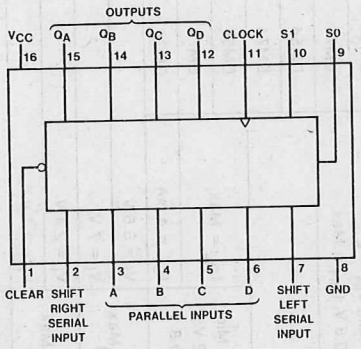
Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls of the of the DM54194/DM74194 should be changed only while the clock input is high.

## Features

- Parallel inputs and outputs
- Four operating modes:
  - Synchronous parallel load
  - Right shift
  - Left shift
  - Do nothing
- Positive edge-triggered clocking
- Direct overriding clear

| Type | Typical Clock Frequency | Typical Power Dissipation |
|---|---|---|
| 194 | 36 MHz | 195 mW |
| LS194A | 36 MHz | 75 mW |
| S194 | 105 MHz | 425 mW |

## Connection Diagram




**54194 (J,W)** **54LS194A (J,W)** **54S194 (J,W)**
**74194 (N)** **74LS194A (N)** **74S194 (N)**

## Truth Table

| Inputs | | | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clear | Mode | | Clock | Serial | | Parallel | | | | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| | S1 | S0 | | Left | Right | A | B | C | D | | | | |
| L | X | X | X | X | X | X | X | X | X | L | L | L | L |
| H | X | X | ↓ | X | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| H | H | H | ↑ | X | X | a | b | c | d | a | b | c | d |
| H | L | H | ↑ | X | H | X | X | X | X | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| H | L | H | ↑ | X | L | X | X | X | X | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| H | H | L | ↑ | H | X | X | X | X | X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | H |
| H | H | L | ↑ | L | X | X | X | X | X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | L |
| H | L | L | X | X | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)
↑ = Transition from low to high level
a, b, c, d = The level of steady state input at inputs A, B, C, or D, respectively.
$Q_{A0}$, $Q_{B0}$, $Q_{C0}$, $Q_{D0}$ = The level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the indicated steady state input conditions were established.
$Q_{An}$, $Q_{Bn}$, $Q_{Cn}$, $Q_{Dn}$ = The level of $Q_A$, $Q_B$, $Q_C$, respectively, before the most-recent ↑ transition of the clock.

## Electrical Characteristics over recommmended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 194 | | | DM54/74 LS194A | | | DM54/74 S194 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | | | | | V |
| | | | $I_I$ = −18 mA | | | | | | | −1.5 | | | −1.2 | |
| $I_{OH}$ | High Level Output Current | | | | | | −800 | | | −400 | | | −1000 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | DM54 | 2.4 | 3.4 | | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.4 | 3.4 | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | | | 4 | | | 20 | mA |
| | | | | DM74 | | | 16 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | DM74 | | 0.2 | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 4 mA | DM74 | | | | | 0.25 | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | | | | 1 | mA |
| | | | $V_I$ = 7 V | | | | | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | | | | 50 | μA |
| | | | $V_I$ = 2.7 V | | | | | | | 20 | | | | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.4 V | | | | −1.6 | | | −0.4 | | | −2 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −20 | | −57 | −20 | | −100 | −40 | | −100 | mA |
| | | | | DM74 | −18 | | −57 | −20 | | −100 | −40 | | −100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | | | 39 | 63 | | 15 | 23 | | 85 | 135 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS or DM54S/74S duration of short circuit should not exceed one second.

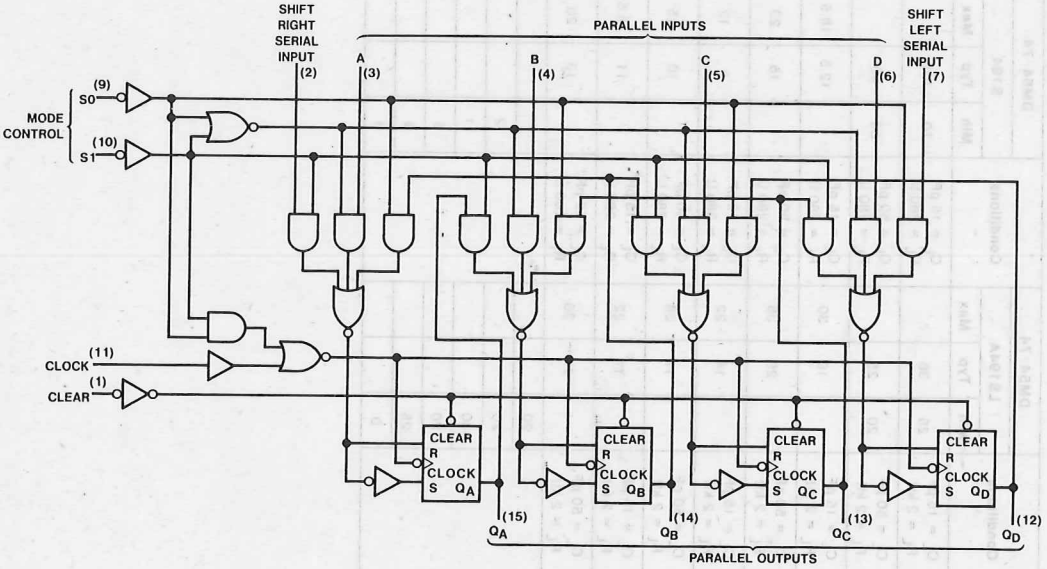
**Note 3:** With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, $I_{CC}$ is tested with a momentary GND, then 4.5 V applied to clock.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

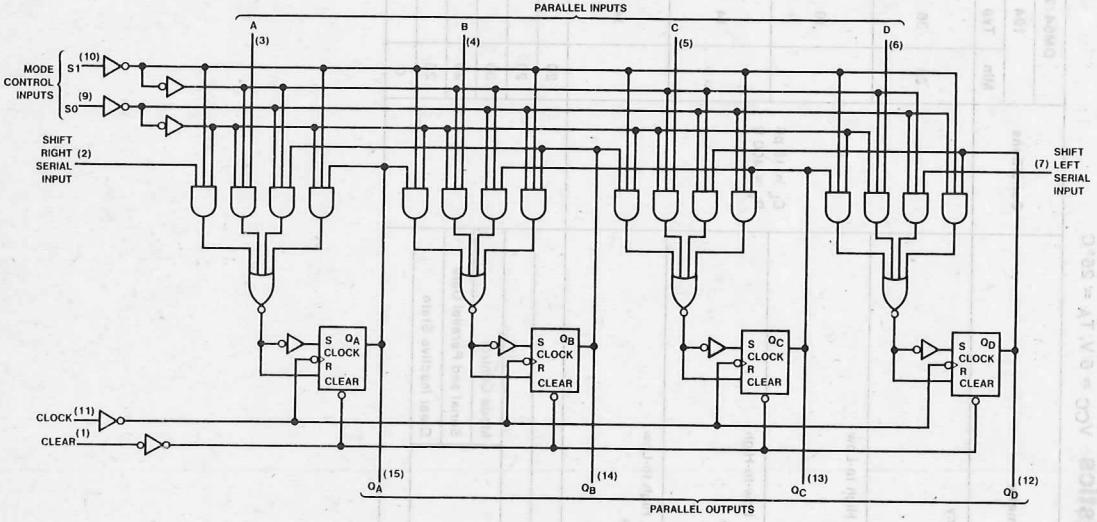
| Parameter | | | Conditions | DM54/74 194 Min | DM54/74 194 Typ | DM54/74 194 Max | Conditions | DM54/74 LS194A Min | DM54/74 LS194A Typ | DM54/74 LS194A Max | Conditions | DM54/74 S194 Min | DM54/74 S194 Typ | DM54/74 S194 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | | $C_L$ = 15 pF, $R_L$ = 400 Ω | 25 | 36 | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 25 | 36 | | $C_L$ = 15 pF, $R_L$ = 280 Ω | 70 | 105 | | ns |
| | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 20 | 25 | | $C_L$ = 50 pF, $R_L$ = 280 Ω | 60 | 90 | | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Clear | | | | 19 | 30 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 19 | 30 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 12.5 | 18.5 | ns |
| | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 25 | 38 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 15 | 23 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output From Clock | | | | 14 | 22 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 14 | 22 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 8 | 12 | ns |
| | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 17 | 26 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 10 | 15 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Clock | | | | 14 | 22 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 17 | 22 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 11 | 16.5 | ns |
| | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 23 | 35 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 13 | 20 | |
| $t_{W(CLOCK)}$ | Width of Clock Pulse | | | 20 | | | | 20 | | | | 7 | | | ns |
| $t_{W(CLEAR)}$ | Width of Clear Pulse | | | 20 | | | | 20 | | | | 12 | | | ns |
| $t_{SETUP}$ | Setup Time | Mode Control | | 30 | | | | 30 | | | | 11 | | | ns |
| | | Serial and Parallel Data | | 20 | | | | 20 | | | | 5 | | | |
| | | Clear Inactive State | | 25 | | | | 25 | | | | 9 | | | |
| $t_{HOLD}$ | Hold Time at Any Input | | | 0 | | | | 0 | | | | 3 | | | ns |

## Logic Diagrams

194

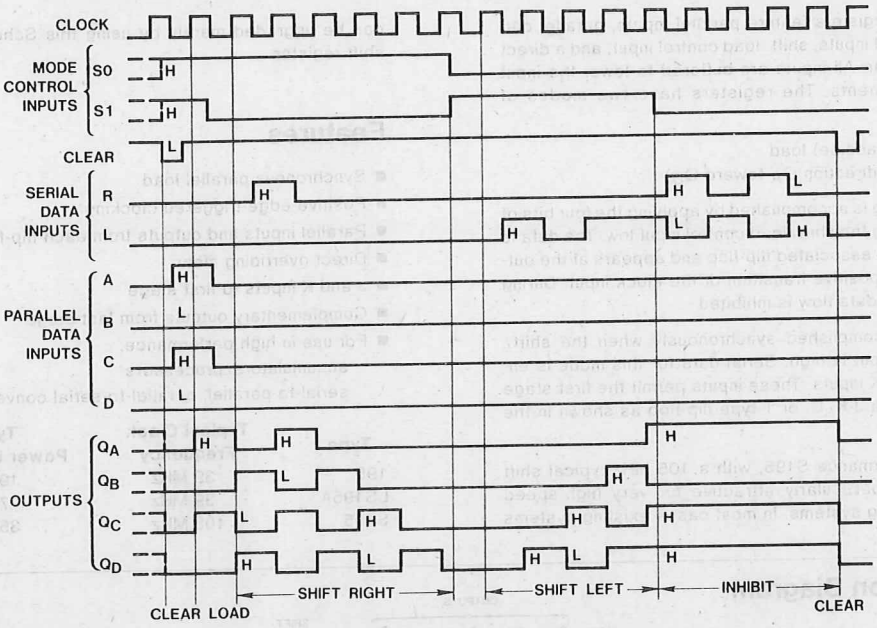



LS194A, S194



## Timing Diagram

TYPICAL CLEAR, LOAD , RIGHT-SHIFT, LEFT-SHIFT, INHIBIT, AND CLEAR SEQUENCES



# 4-Bit Parallel Access Shift Registers

## General Description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load
Shift (in the direction $Q_A$ toward $Q_D$)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D, or T-type flip-flop as shown in the truth table.

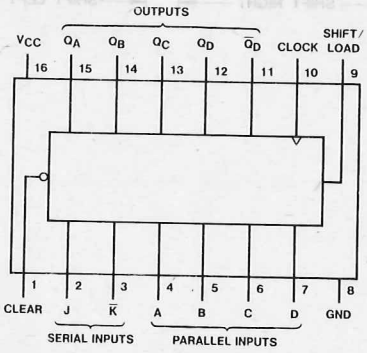
The high-performance S195, with a 105 MHz typical shift frequency, is particularly attractive for very high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky-clamped shift register.

## Features

- Synchronous parallel load
- Positive-edge-triggered clocking
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and $\overline{K}$ inputs to first stage
- Complementary outputs from last stage
- For use in high-performance:
  accumulators/processors
  serial-to-parallel, parallel-to-serial converters

| Type | Typical Clock Frequency | Typical Power Dissipation |
|---|---|---|
| 195 | 39 MHz | 195 mW |
| LS195A | 39 MHz | 70 mW |
| S195 | 105 MHz | 350 mW |

## Connection Diagram




**54195 (J,W)** **54S195 (J,W)** **74LS195A (N)**
**54LS195A (J,W)** **74195 (N)** **74S195 (N)**

## Truth Table

| Inputs | | | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clear | Shift/ Load | Clock | Serial | | Parallel | | | | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $\overline{Q}_D$ |
| | | | J | $\overline{K}$ | A | B | C | D | | | | | |
| L | X | X | X | X | X | X | X | X | L | L | L | L | H |
| H | L | ↑ | X | X | a | b | c | d | a | b | c | d | $\overline{d}$ |
| H | H | L | X | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $\overline{Q}_{D0}$ |
| H | H | ↑ | L | H | X | X | X | X | $Q_{A0}$ | $Q_{A0}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |
| H | H | ↑ | L | L | X | X | X | X | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |
| H | H | ↑ | H | H | X | X | X | X | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |
| H | H | ↑ | H | L | X | X | X | X | $\overline{Q}_{An}$ | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)
↑ = Transition from low to high level
a,b,c,d = The level of steady state input at A, B, C, or D, respectively.
$Q_{A0}$, $Q_{B0}$, $Q_{C0}$, $Q_{D0}$ = The level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the indicated steady state input conditions were established.
$Q_{An}$, $Q_{Bn}$, $Q_{Cn}$ = The level of $Q_A$, $Q_B$, $Q_C$, respectively, before the most recent transition of the clock.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 195 | | | DM54/74 LS195A | | | DM54/74 S195 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | | | | | V |
| | | | $I_I$ = −18 mA | | | | | | | −1.5 | | | −1.2 | |
| $I_{OH}$ | High Level Output Current | | | | | | −800 | | | −400 | | | −1000 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V | | DM54 | 2.4 | 3.4 | | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | DM74 | 2.4 | 3.4 | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | | | 4 | | | 20 | mA |
| | | | | DM74 | | | 16 | | | 8 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min | $I_{OL}$ = Max | DM54 | | 0.2 | 0.4 | | 0.25 | 0.4 | | | 0.5 | V |
| | | $V_{IH}$ = 2 V | | DM74 | | 0.2 | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| | | $V_{IL}$ = 0.8 V | $I_{OL}$ = 4 mA | DM74 | | | | | 0.25 | 0.4 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | | | | 1 | mA |
| | | | $V_I$ = 7 V | | | | | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | | | | | μA |
| | | | $V_I$ = 2.7 V | | | | | | | 20 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.4 V | | | | −1.6 | | | −0.4 | | | | mA |
| | | | $V_I$ = 0.5 V | | | | | | | | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −20 | | −57 | −20 | | −100 | −40 | | −100 | mA |
| | | | | DM74 | −18 | | −57 | −20 | | −100 | −40 | | −100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | | | 39 | 63 | | 14 | 21 | | 70 | 109 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

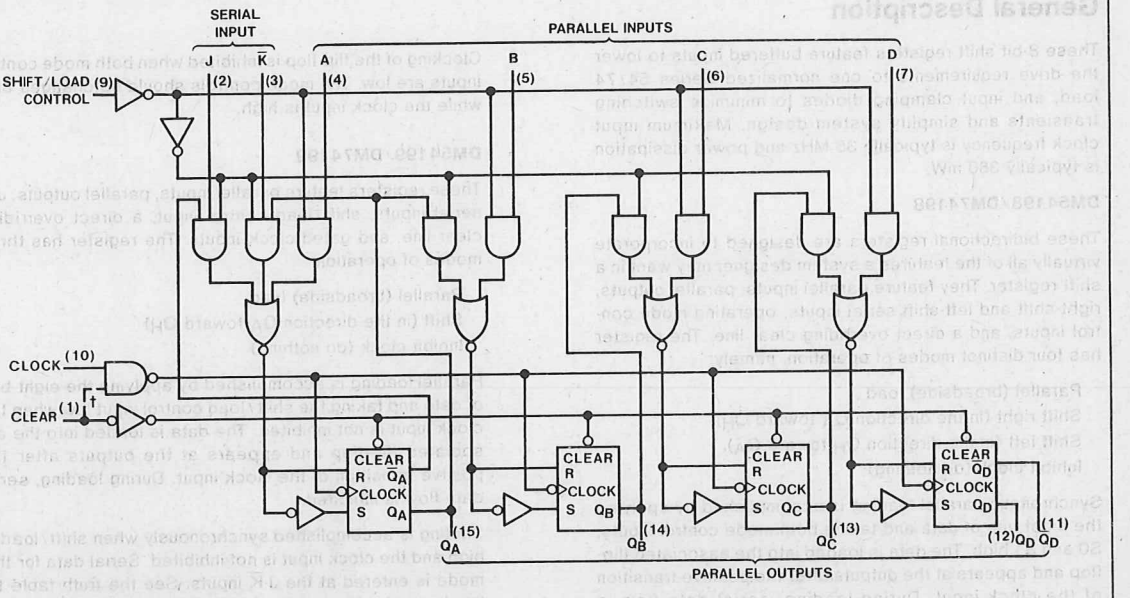
**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS or DM54S/74S duration of short circuit should not exceed one second.

**Note 3:** With all outputs open, shift/load grounded, and 4.5 V applied to the J, $\overline{K}$, and data inputs, $I_{CC}$ is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

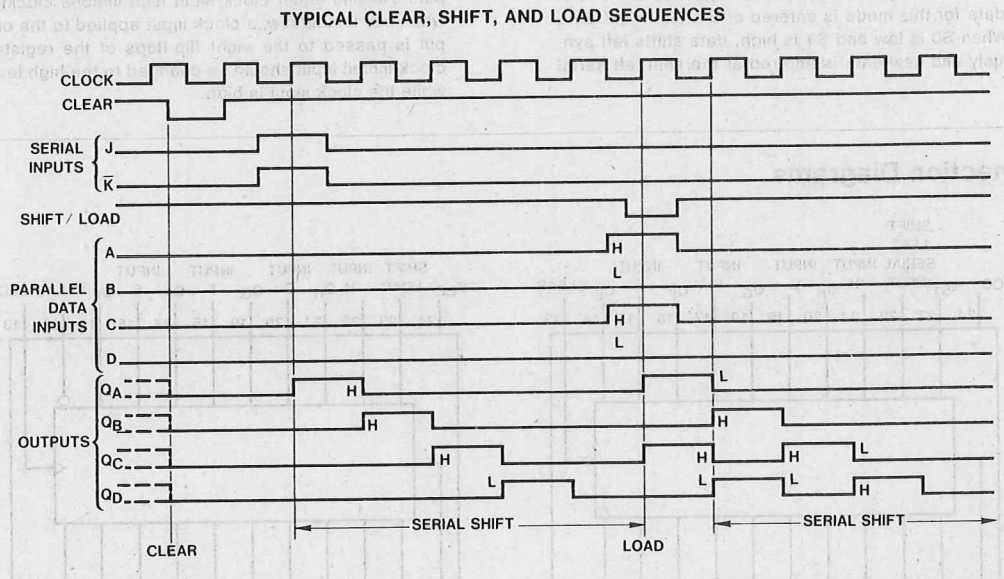
| Parameter | | | Conditions | DM54/74 195 Min | DM54/74 195 Typ | DM54/74 195 Max | Conditions | DM54/74 LS195A Min | DM54/74 LS195A Typ | DM54/74 LS195A Max | Conditions | DM54/74 S195 Min | DM54/74 S195 Typ | DM54/74 S195 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | | $C_L$ = 15 pF, $R_L$ = 400 Ω | 30 | 39 | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 30 | 39 | | $C_L$ = 15 pF, $R_L$ = 280 Ω | 70 | 105 | | MHz |
| | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 25 | 30 | | $C_L$ = 50 pF, $R_L$ = 280 Ω | 60 | 90 | | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Clear | | | | 19 | 30 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 19 | 30 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 12.5 | 18.5 | ns |
| | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 25 | 38 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 15 | 23 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output From Clock | | | | 14 | 22 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 14 | 22 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 8 | 12 | ns |
| | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 17 | 26 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 10 | 15 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Clock | | | | 17 | 26 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 17 | 26 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 11 | 16.5 | ns |
| | | | | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 23 | 35 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 13 | 20 | |
| $t_{W(CLOCK)}$ | Width of Clock Input Pulse | | | 16 | | | | 16 | | | | 7 | | | ns |
| $t_{W(CLEAR)}$ | Width of Clear Input Pulse | | | 12 | | | | 12 | | | | 12 | | | ns |
| $t_{SETUP}$ | Setup Time | Shift/Load | | 25 | | | | 25 | | | | 11 | | | ns |
| | | Serial and Parallel Data | | 15 | | | | 15 | | | | 5 | | | |
| | | Clear Inactive State | | 25 | | | | 25 | | | | 9 | | | |
| $t_{RELEASE}$ | Shift/Load Release Time | | | | | 10 | | | | 10 | | | | 6 | ns |
| $t_{HOLD}$ | Serial and Parallel Data Hold Time | | | 0 | | | | 0 | | | | 3 | | | ns |

## Logic Diagram




†This connection is made on 195 only.

## Timing Diagram



# 8-Bit Shift Registers

## General Description

These 8-bit shift registers feature buffered inputs to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes to minimize switching transients and simplify system design. Maximum input clock frequency is typically 35 MHz and power dissipation is typically 360 mW.

**DM54198/DM74198**

These bidirectional registers are designed to incorporate virtually all of the features a system designer may want in a shift register. They feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating mode control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction $Q_A$ toward $Q_H$)
Shift left (in the direction $Q_H$ toward $Q_A$)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the eight bits of data and taking both mode control inputs, S0 and S1 high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls should be changed only while the clock input is high.

**DM54199/DM74199**

These registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, a direct overriding clear line, and gated clock inputs. The register has three modes of operation:

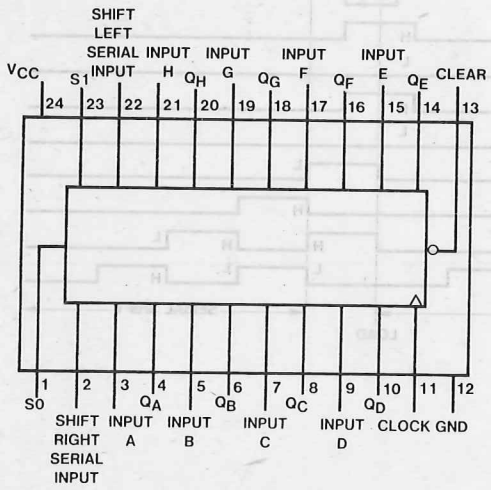
Parallel (broadside) load
Shift (in the direction $Q_A$ toward $Q_H$)
Inhibit clock (do nothing)

Parallel loading is accomplished by applying the eight bits of data and taking the shift/load control input low when the clock input is not inhibited. The data is loaded into the associated flip-flop and appears at the outputs after the positve transition of the clock input. During loading, serial data flow is inhibited.

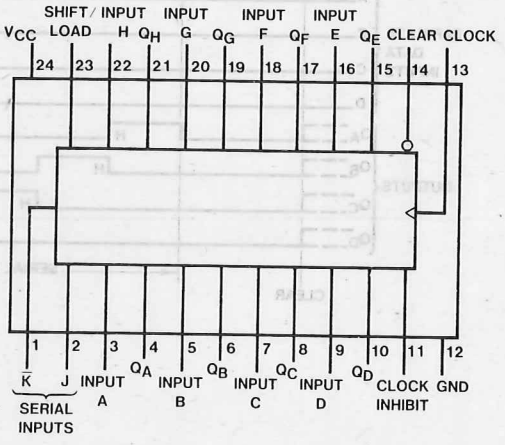
Shifting is accomplished synchronously when shift/load is high and the clock input is not inhibited. Serial data for this mode is entered at the J-$\overline{K}$ inputs. See the truth table for levels required to enter serial data into the first flip-flop.

Both of the clock inputs are identical in function and may be used interchangeably to serve as clock or clock-inhibit inputs. Holding either clock input high inhibits clocking; but when one is held low, a clock input applied to the other input is passed to the eight flip-flops of the register. The clock-inhibit input should be changed to the high level only while the clock input is high.

## Connection Diagrams




54198 (J,W)/74198 (N)




54199 (J,W)/74199 (N)

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM54/74 198, 199 | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −800 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OH}$ = −800 μA | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | DM54 | −20 | | −57 | mA |
| | | | DM74 | −18 | | −57 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max<br>(See Conditions for $I_{CC}$ Table) | DM54 | | 72 | 104 | mA |
| | | | DM74 | | 72 | 116 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | DM54/74 198,199 | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Input Count Frequency | $C_L$ = 15 pF, $R_L$ = 400 Ω | 25 | 35 | | MHz |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Clear | | | 23 | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output From Clock | | | 20 | 30 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output From Clock | | | 17 | 26 | ns |
| $t_W$ | Width of Clock or Clear Pulse | | 20 | | | ns |
| $t_{SETUP}$ | Mode-Control Setup Time | | 30 | | | ns |
| $t_{SETUP}$ | Data Setup Time | | 20 | | | ns |
| $t_{HOLD}$ | Hold Time at Any Input | | 0 | | | ns |

## Conditions for $I_{CC}$ (All outputs are open)

| Type | Apply 4.5 V | First Ground, Then Apply 4.5 V | Ground |
|---|---|---|---|
| 198 | Serial Input, S0, S1 | Clock | Clear, Inputs A thru H |
| 199 | J, $\overline{K}$, Inputs A thru H | Clock | Clock Inhibit, Clear, Shift/Load |

6

## Truth Tables

198

| Inputs | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Clear | Mode S1 | Mode S0 | Clock | Serial Left | Serial Right | Parallel A...H | $Q_A$ | $Q_B$ | ... | $Q_G$ | $Q_H$ |
| L | X | X | X | X | X | X | L | L | ... | L | L |
| H | X | X | L | X | X | X | $Q_{A0}$ | $Q_{B0}$ | ... | $Q_{G0}$ | $Q_{H0}$ |
| H | H | H | ↑ | X | X | a...h | a | b | ... | g | h |
| H | L | H | ↑ | X | H | X | H | $Q_{An}$ | ... | $Q_{Fn}$ | $Q_{Gn}$ |
| H | L | H | ↑ | X | L | X | L | $Q_{An}$ | ... | $Q_{Fn}$ | $Q_{Gn}$ |
| H | H | L | ↑ | H | X | X | $Q_{Bn}$ | $Q_{Cn}$ | ... | $Q_{Hn}$ | H |
| H | H | L | ↑ | L | X | X | $Q_{Bn}$ | $Q_{Cn}$ | ... | $Q_{Hn}$ | L |
| H | L | L | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | ... | $Q_{G0}$ | $Q_{H0}$ |

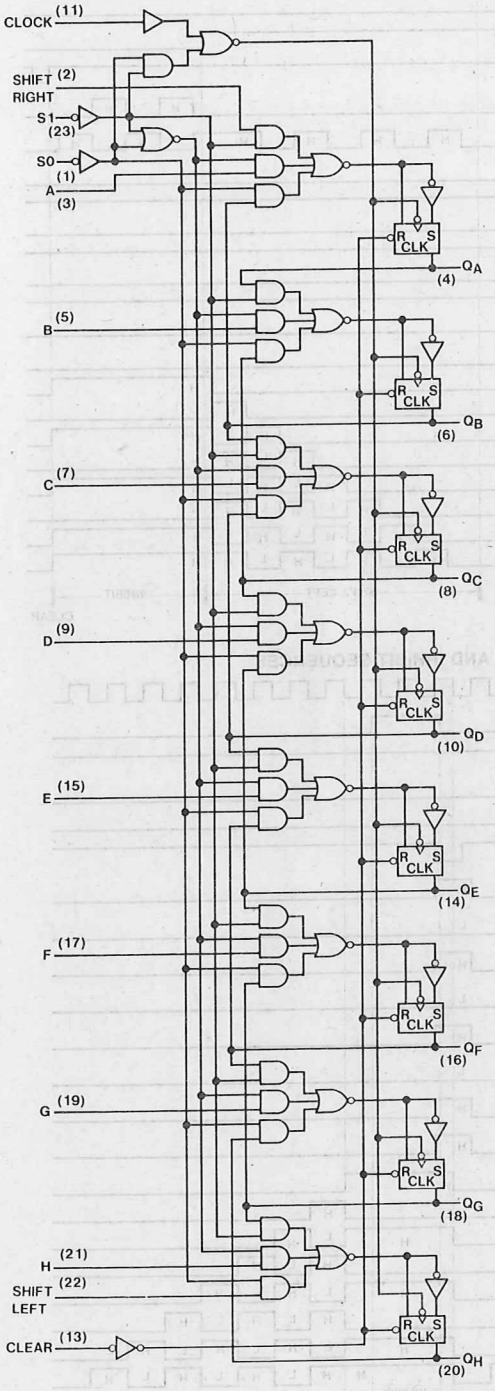
H = High Level (steady state), L = Low Level (steady state)
X = Don't care (any input, including transitions)
↑ = Transition from low to high level
a...h = The level of steady state input at inputs A thru H, respectively.
$Q_{A0}$, $Q_{B0}$, $Q_{G0}$, $Q_{H0}$ = The level of $Q_A$, $Q_B$, $Q_G$, or $Q_H$, respectively, before the indicated steady-state input conditions were established.
$Q_{An}$, $Q_{Bn}$, etc. = The level of $Q_A$, $Q_B$, etc., respectively, before the most-recent ↑ transition of the clock.

199

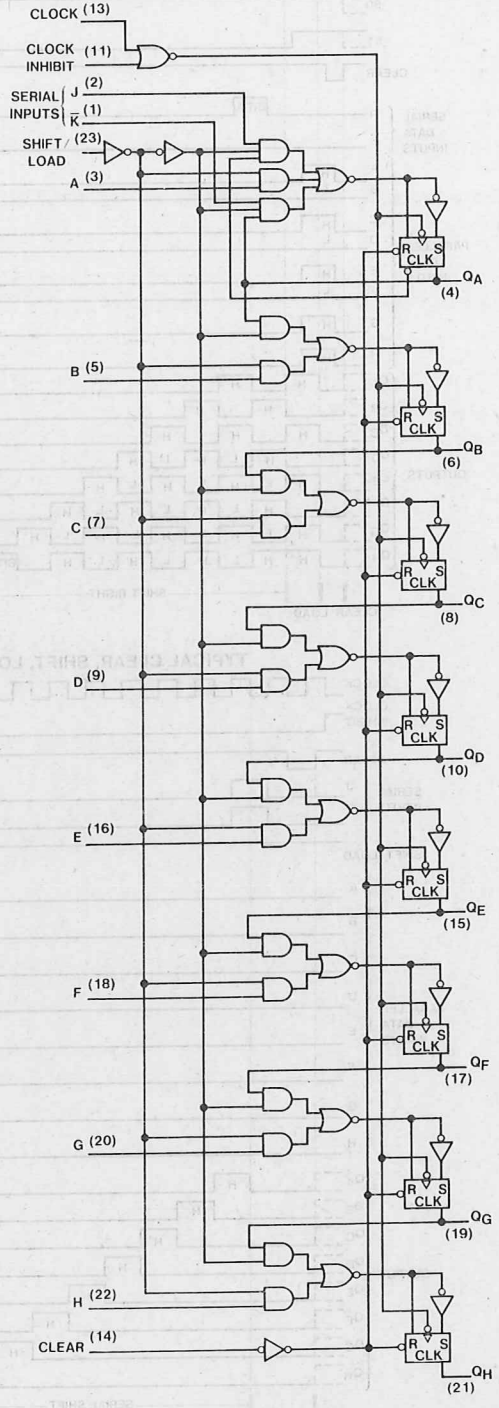
| Inputs | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Clear | Shift/Load | Clock Inhibit | Clock | Serial J | Serial $\overline{K}$ | Parallel A...H | $Q_A$ | $Q_B$ | $Q_C$ | ... | $Q_H$ |
| L | X | X | X | X | X | X | L | L | L | ... | L |
| H | X | L | L | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | ... | $Q_{H0}$ |
| H | L | L | ↑ | X | X | a...h | a | b | c | ... | h |
| H | H | L | ↑ | L | H | X | $Q_{A0}$ | $Q_{A0}$ | $Q_{B0}$ | ... | $Q_{Gn}$ |
| H | H | L | ↑ | L | L | X | L | $Q_{An}$ | $Q_{Bn}$ | ... | $Q_{Gn}$ |
| H | H | L | ↑ | H | H | X | H | $Q_{An}$ | $Q_{Bn}$ | ... | $Q_{Gn}$ |
| H | H | L | ↑ | H | L | X | $\overline{Q}_{An}$ | $Q_{An}$ | $Q_{Bn}$ | ... | $Q_{Gn}$ |
| H | X | H | ↑ | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{B0}$ | ... | $Q_{H0}$ |

## Logic Diagrams

198




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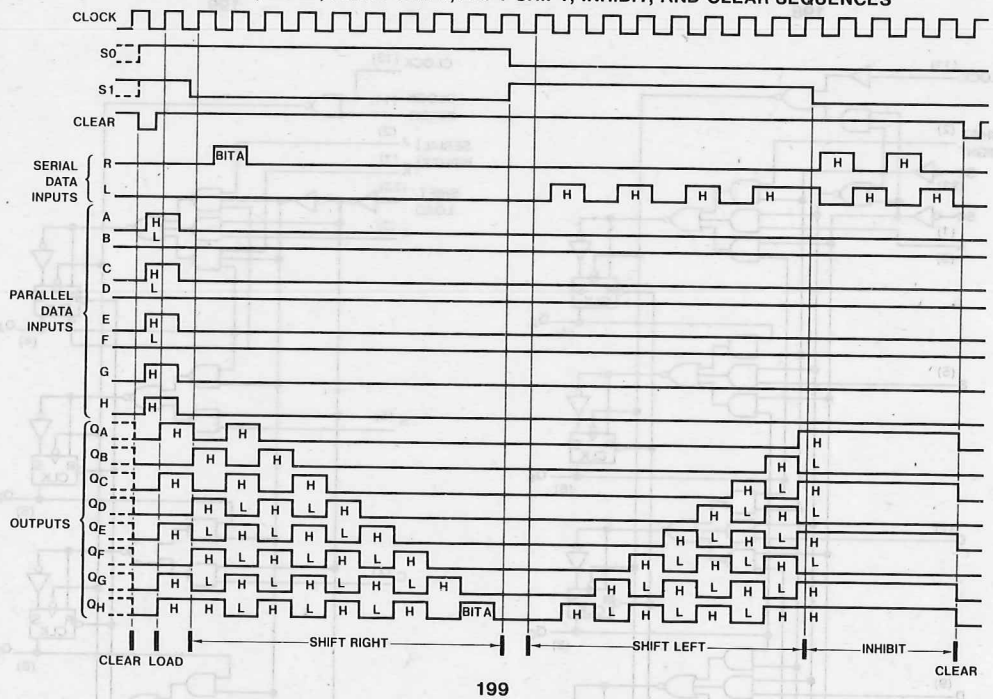



6

## Timing Diagrams

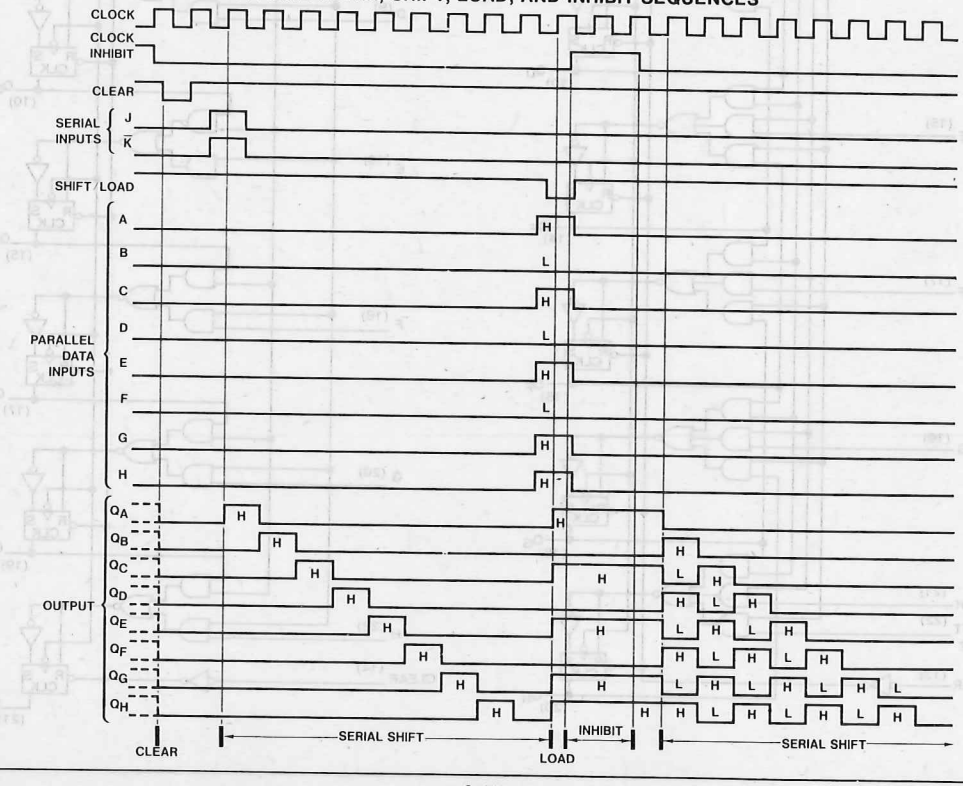
198

TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT, AND CLEAR SEQUENCES




199

TYPICAL CLEAR, SHIFT, LOAD, AND INHIBIT SEQUENCES



## Parameter Measurement Information

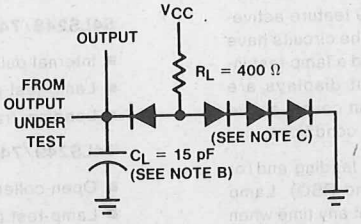
198
TEST TABLE FOR SYNCHRONOUS INPUTS

| Data Input for Test | $S_1$ | $S_0$ | Output Tested (See Note E) |
|---|---|---|---|
| A | 4.5 V | 4.5 V | $Q_A$ at $t_{n+1}$ |
| B | 4.5 V | 4.5 V | $Q_B$ at $t_{n+1}$ |
| C | 4.5 V | 4.5 V | $Q_C$ at $t_{n+1}$ |
| D | 4.5 V | 4.5 V | $Q_D$ at $t_{n+1}$ |
| E | 4.5 V | 4.5 V | $Q_E$ at $t_{n+1}$ |
| F | 4.5 V | 4.5 V | $Q_F$ at $t_{n+1}$ |
| G | 4.5 V | 4.5 V | $Q_G$ at $t_{n+1}$ |
| H | 4.5 V | 4.5 V | $Q_H$ at $t_{n+1}$ |
| L Serial Input | 4.5 V | 0 V | $Q_A$ at $t_{n+8}$ |
| R Serial Input | 0 V | 4.5 V | $Q_H$ at $t_{n+8}$ |

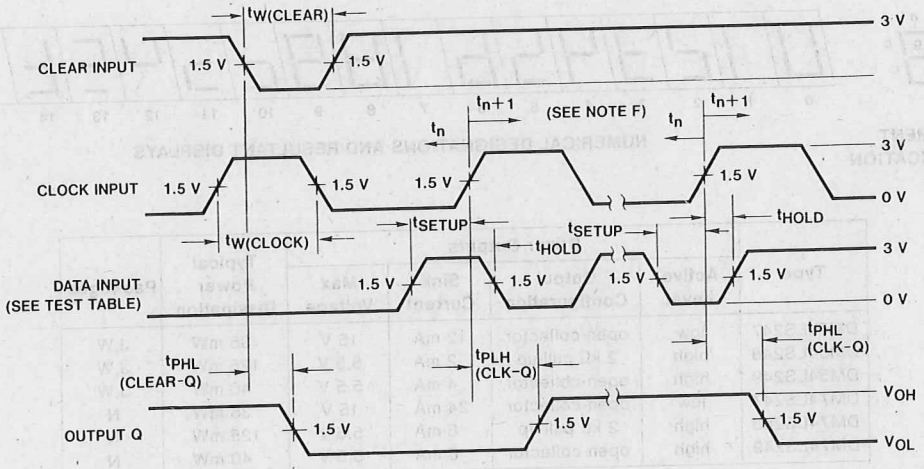
199
TEST TABLE FOR SYNCHRONOUS INPUTS

| Data Input for Test | Shift/Load | Output Tested (See Note E) |
|---|---|---|
| A | 0 V | $Q_A$ at $t_{n+1}$ |
| B | 0 V | $Q_B$ at $t_{n+1}$ |
| C | 0 V | $Q_C$ at $t_{n+1}$ |
| D | 0 V | $Q_D$ at $t_{n+1}$ |
| E | 0 V | $Q_E$ at $t_{n+1}$ |
| F | 0 V | $Q_F$ at $t_{n+1}$ |
| G | 0 V | $Q_G$ at $t_{n+1}$ |
| H | 0 V | $Q_H$ at $t_{n+1}$ |
| J and $\overline{K}$ | 4.5 V | $Q_H$ at $t_{n+8}$ |

LOAD FOR OUTPUT UNDER TEST




SWITCHING TIME WAVEFORMS




**Note A:** The clock pulse has the following characteristics: $t_{w(clock)} \geq 20$ ns and PRR = 1 MHz.
The clear pulse has the following characteristics: $t_{w(clear)} \geq 20$ ns and $t_{HOLD} = 0$ ns.
When testing $f_{MAX}$, vary the clock PRR.

**Note B:** $C_L$ includes probe and jig capacitance.

**Note C:** All diodes are 1N3064.

**Note D:** A clear pulse is applied prior to each test.

**Note E:** Propagation delay times ($t_{PLH}$ and $t_{PHL}$) are measured at $t_{n+1}$. Proper shifting of data is verified at $t_{n+8}$ with a functional test.

**Note F:** $t_n$ = bit time before clocking transition.
$t_{n+1}$ = bit time after one clocking transition
$t_{n+8}$ = bit time after clocking transitions

# BCD-to-Seven Segment Decoders/Drivers

## General Description

The DM54LS247/DM74LS247 and DM54LS248/DM74LS248 are electrically and functionally identical to the DM54LS47/DM74LS47 and DM54LS48/DM74LS48, respectively, and have the same pin assignments as their equivalents. They can be used interchangeably in present or future designs to offer designers a choice between two indicator fonts. The DM54LS249/DM74LS249 is a 16-pin version of the 14-pin DM54LS49/DM74LS49. Included in the DM54LS249/DM74LS249 circuit is the full functional capability for lamp test and ripple blanking, which is not available in the DM54LS49/DM74LS49 circuit. The DM54LS247/DM74LS247, DM54LS248/DM74LS248, and DM54LS249/DM74LS249 compose the 6 and the 9 with tails. Composition of all other characters, including display patterns for BCD inputs above nine, is identical. The DM54LS247/DM74LS247 features active-low outputs designed for driving indicators directly, and the DM54LS248/DM74LS248 and DM54LS249/DM74LS249 feature active-high outputs for driving lamp buffers. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

All of these circuits incorporate automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is at a high level. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

## Features

- All circuit types feature lamp intensity modulation capability

**54LS247/74LS247**

- Open-collector outputs drive indicators directly
- Lamp-test provision
- Leading/trailing zero suppression

**54LS248/74LS248**

- Internal pull-ups eliminate need for external resistors
- Lamp-test provision
- Leading/trailing zero suppression

**54LS249/74LS249**

- Open-collector outputs
- Lamp-test provision
- Leading/trailing zero suppression

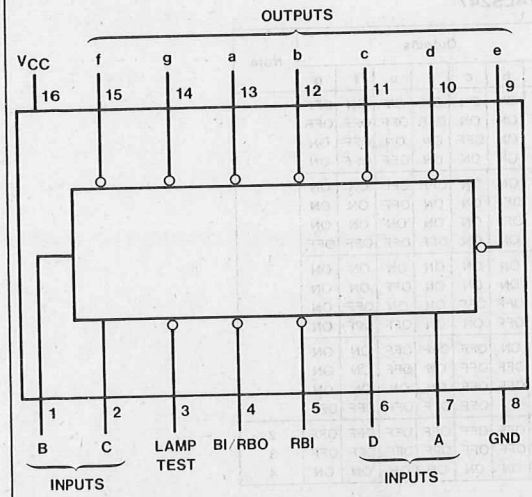



SEGMENT IDENTIFICATION

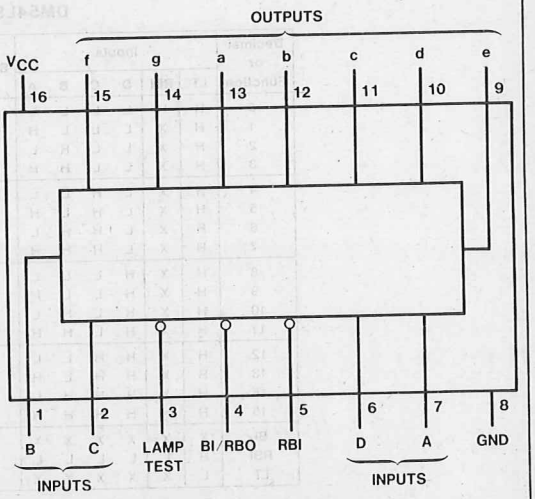
NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

| Type | Driver Outputs | | | | Typical Power Dissipation | Packages |
|---|---|---|---|---|---|---|
| | Active Level | Output Configuration | Sink Current | Max Voltage | | |
| DM54LS247 | low | open-collector | 12 mA | 15 V | 35 mW | J,W |
| DM54LS248 | high | 2 kΩ pull-up | 2 mA | 5.5 V | 125 mW | J,W |
| DM54LS249 | high | open-collector | 4 mA | 5.5 V | 40 mW | J,W |
| DM74LS247 | low | open-collector | 24 mA | 15 V | 35 mW | N |
| DM74LS248 | high | 2 kΩ pull-up | 6 mA | 5.5 V | 125 mW | N |
| DM74LS249 | high | open-collector | 8 mA | 5.5 V | 40 mW | N |

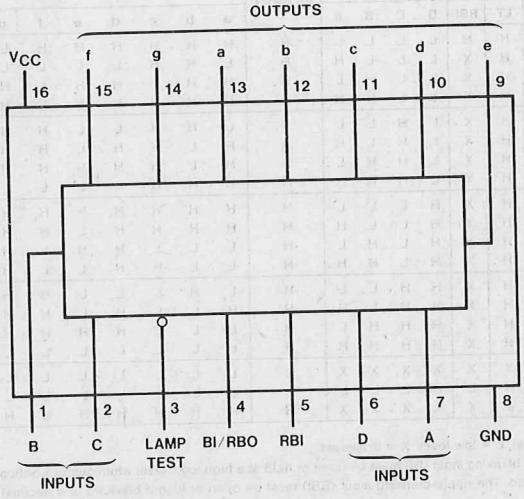
## Connection Diagrams




54LS247 (J,W); 74LS247 (N)




54LS248 (J,W); 74LS248 (N)




54LS249 (J,W); 74LS249 (N)

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## Truth Tables

### DM54LS247/DM74LS247

| Decimal or Function | Inputs | | | | | | BI/RBO† | Outputs | | | | | | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LT | RBI | D | C | B | A | | a | b | c | d | e | f | g | |
| 0 | H | H | L | L | L | L | H | ON | ON | ON | ON | ON | ON | OFF | |
| 1 | H | X | L | L | L | H | H | OFF | ON | ON | OFF | OFF | OFF | OFF | |
| 2 | H | X | L | L | H | L | H | ON | ON | OFF | ON | ON | OFF | ON | |
| 3 | H | X | L | L | H | H | H | ON | ON | ON | ON | OFF | OFF | ON | |
| 4 | H | X | L | H | L | L | H | OFF | ON | ON | OFF | OFF | ON | ON | |
| 5 | H | X | L | H | L | H | H | ON | OFF | ON | ON | OFF | ON | ON | |
| 6 | H | X | L | H | H | L | H | ON | OFF | ON | ON | ON | ON | ON | |
| 7 | H | X | L | H | H | H | H | ON | ON | ON | OFF | OFF | OFF | OFF | |
| 8 | H | X | H | L | L | L | H | ON | ON | ON | ON | ON | ON | ON | 1 |
| 9 | H | X | H | L | L | H | H | ON | ON | ON | ON | OFF | ON | ON | |
| 10 | H | X | H | L | H | L | H | OFF | OFF | OFF | ON | ON | OFF | ON | |
| 11 | H | X | H | L | H | H | H | OFF | OFF | ON | ON | OFF | OFF | ON | |
| 12 | H | X | H | H | L | L | H | OFF | ON | OFF | OFF | OFF | ON | ON | |
| 13 | H | X | H | H | L | H | H | ON | OFF | OFF | ON | OFF | ON | ON | |
| 14 | H | X | H | H | H | L | H | OFF | OFF | OFF | ON | ON | ON | ON | |
| 15 | H | X | H | H | H | H | H | OFF | OFF | OFF | OFF | OFF | OFF | OFF | |
| BI | X | X | X | X | X | X | L | OFF | OFF | OFF | OFF | OFF | OFF | OFF | 2 |
| RBI | H | L | L | L | L | L | L | OFF | OFF | OFF | OFF | OFF | OFF | OFF | 3 |
| LT | L | X | X | X | X | X | H | ON | ON | ON | ON | ON | ON | ON | 4 |

### DM54LS248/DM74LS248, DM54LS249/DM74LS249

| Decimal or Function | Inputs | | | | | | BI/RBO† | Outputs | | | | | | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LT | RBI | D | C | B | A | | a | b | c | d | e | f | g | |
| 0 | H | H | L | L | L | L | H | H | H | H | H | H | H | L | 1 |
| 1 | H | X | L | L | L | H | H | L | H | H | L | L | L | L | 1 |
| 2 | H | X | L | L | H | L | H | H | H | L | H | H | L | H | |
| 3 | H | X | L | L | H | H | H | H | H | H | H | L | L | H | |
| 4 | H | X | L | H | L | L | H | L | H | H | L | L | H | H | |
| 5 | H | X | L | H | L | H | H | H | L | H | H | L | H | H | |
| 6 | H | X | L | H | H | L | H | H | L | H | H | H | H | H | |
| 7 | H | X | L | H | H | H | H | H | H | H | L | L | L | L | |
| 8 | H | X | H | L | L | L | H | H | H | H | H | H | H | H | 1 |
| 9 | H | X | H | L | L | H | H | H | H | H | H | L | H | H | |
| 10 | H | X | H | L | H | L | H | L | L | L | H | H | L | H | |
| 11 | H | X | H | L | H | H | H | L | L | H | H | L | L | H | |
| 12 | H | X | H | H | L | L | H | L | H | L | L | L | H | H | |
| 13 | H | X | H | H | L | H | H | H | L | L | H | L | H | H | |
| 14 | H | X | H | H | H | L | H | L | L | L | H | H | H | H | |
| 15 | H | X | H | H | H | H | H | L | L | L | L | L | L | L | |
| BI | X | X | X | X | X | X | L | L | L | L | L | L | L | L | 2 |
| RBI | H | L | L | L | L | L | L | L | L | L | L | L | L | L | 3 |
| LT | L | X | X | X | X | X | H | H | H | H | H | H | H | H | 4 |

H = high level, L = low level, X = irrelevant

**Note 1:** The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

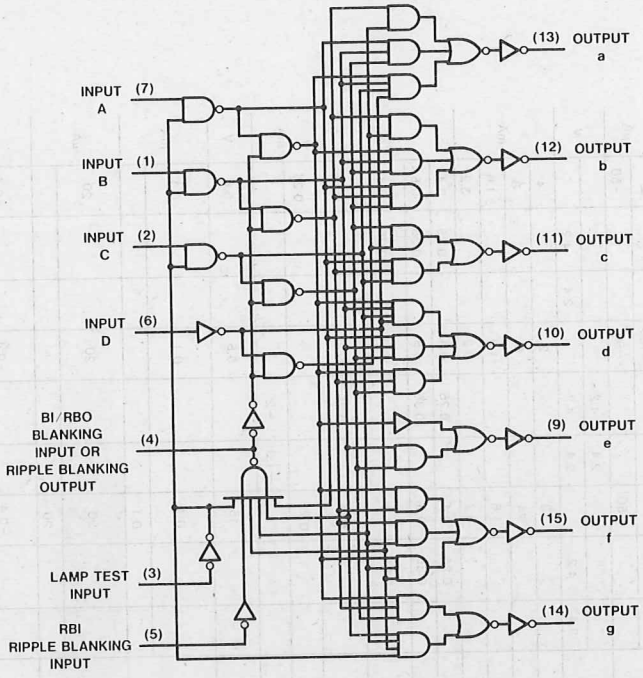
**Note 2:** When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.

**Note 3:** When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).

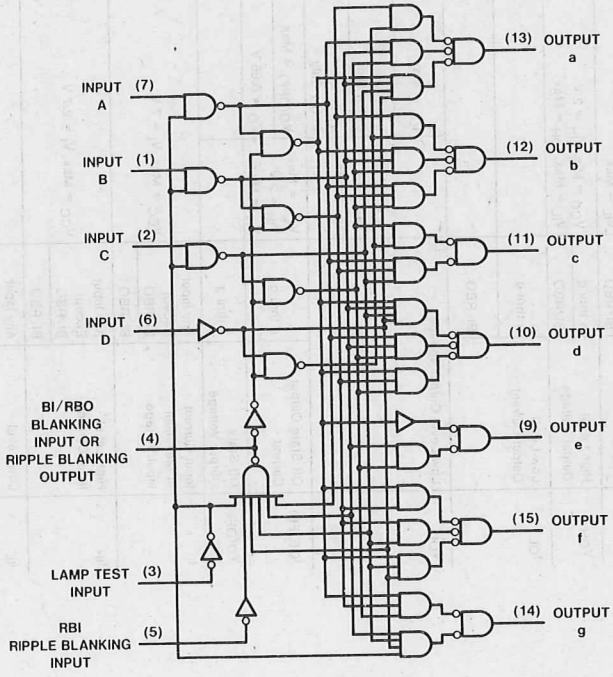
**Note 4:** When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

† BI/RBO is a wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

## DM54LS247/DM74LS247




## DM54LS248/DM74LS248, DM54LS249/DM74LS249




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## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM54/74 | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | LS247 | | | LS248 | | | LS249 | | | |
| | | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | DM54 | | | 0.8 | | | 0.8 | | | 0.8 | V |
| | | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | a thru g | $V_{CC}$ = Min, $V_{IH}$ = 2 V | | | | | | | | −100 | | | | µA |
| | | BI/RBO | $V_{IL}$ = Max | | | | | −50 | | | −50 | | | −50 | |
| $V_{OH}$ | High Level Output Voltage | a thru g | $V_{CC}$ = Min, $V_{IH}$ = 2 V | | | | | | 2.4 | 4.2 | | | | | V |
| | | BI/RBO | $V_{IL}$ = Max, $I_{OH}$ = Max | | | 2.4 | 4.2 | | 2.4 | 4.2 | | 2.4 | 4.2 | | |
| $I_{OL}$ | Low Level Output Current | a thru g | | | DM54 | | | 12 | | | 2 | | | 4 | mA |
| | | | | | DM74 | | | 24 | | | 6 | | | 8 | |
| | | BI/RBO | | | DM54 | | | 1.6 | | | 1.6 | | | 1.6 | |
| | | | | | DM74 | | | 3.2 | | | 3.2 | | | 3.2 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OL}$ = Max | DM54 | | 0.25 | 0.4 | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | | | DM74 | | 0.35 | 0.5 | | 0.35 | 0.5 | | 0.35 | 0.5 | |
| | | | | $I_{OL}$ = Max/2, DM74 Only | | | 0.25 | 0.4 | | | N/A | | 0.25 | 0.4 | |
| | | | | $I_{OL}$ = 2 mA, DM74 Only | | | | N/A | | 0.25 | 0.4 | | | N/A | |
| $I_{O(OFF)}$ | Off-State Output Current | a thru g | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $V_{O(OFF)}$ = Max | | | | 0.25 | | | | | | 0.25 | mA |
| | | | | $V_O$ = 0.85 V | | | | | −1.3 | −2 | | | | | |
| $V_{O(OFF)}$ | Off-State Output Voltage | a thru g | | | | | | 15 | | | 5.5 | | | 5.5 | V |
| $I_I$ | Input Current at Maximum Input Voltage | Any Input Except BI/RBO | $V_{CC}$ = Max, $V_I$ = 7 V | | | | | 0.1 | | | 0.1 | | | 0.1 | mA |
| | | BI/RBO | | | | | | 0.1 | | | | | | | |
| $I_{IH}$ | High Level Input Current | Any Input Except BI/RBO | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | | 20 | | | 20 | | | 20 | µA |
| | | BI/RBO | | | | | | 20 | | | | | | | |
| $I_{IL}$ | Low Level Input Current | Any Input Except BI/RBO | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | | −0.4 | | | −0.4 | | | −0.4 | mA |
| | | BI/RBO | | | | | | −1.2 | | | −1.2 | | | −1.2 | |
| $I_{OS}$ | Short Circuit Output Current | BI/RBO | $V_{CC}$ = Max | | | −0.3 | | −2 | −0.3 | | −2 | −0.3 | | −2 | mA |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (2) | | DM54 | | 7 | 13 | | 25 | 38 | | 8 | 15 | mA |
| | | | | | DM74 | | 7 | 13 | | 25 | 38 | | 8 | 15 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** $I_{CC}$ is measured with all outputs open and all inputs at 4.5 V.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Device | Conditions | $t_{PLH}$ and $t_{PHL}$ (ns) Propagation Delay Time From A Input | | | $t_{PLH}$ and $t_{PHL}$ (ns) Propagation Delay Time From RBI Input | | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max |
| LS247 | $C_L$ = 15 pF, $R_L$ = 665 Ω | | | 100 | | | 100 |
| LS248 | $C_L$ = 15 pF, $R_L$ = 4 kΩ | | | 100 | | | |
| | $C_L$ = 15 pF, $R_L$ = 6 kΩ | | | | | | 100 |
| LS249 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | | 100 | | | |
| | $C_L$ = 15 pF, $R_L$ = 6 kΩ | | | | | | 100 |

# TRI-STATE® Data Selectors/Multiplexers

## General Description

These data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources, and feature a strobe-controlled TRI-STATE output. The strobe must be at a low logic level to enable these devices. The TRI-STATE outputs permit direct connection to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

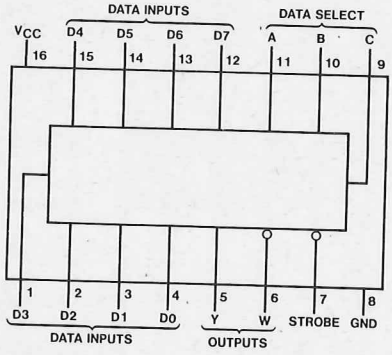
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

## Features

- TRI-STATE versions of 151, LS151, S151
- Interface directly with system bus
- Perform parallel-to-serial conversion
- Permit multiplexing from N-lines to one line
- Complementary outputs provide true and inverted data

| Type | Max No. of Common Outputs | Typical Prop Delay Time (D to Y) | Typical Power Dissipation |
|---|---|---|---|
| 54251 | 49 | 17 ns | 155 mW |
| 74251 | 129 | 17 ns | 155 mW |
| 54LS251 | 49 | 17 ns | 35 mW |
| 74LS251 | 129 | 17 ns | 35 mW |
| 54S251 | 39 | 8 ns | 275 mW |
| 74S251 | 129 | 8 ns | 275 mW |

## Connection Diagram




**54251 (J,W)**
**54LS251 (J,W)**
**54S251 (J,W)**

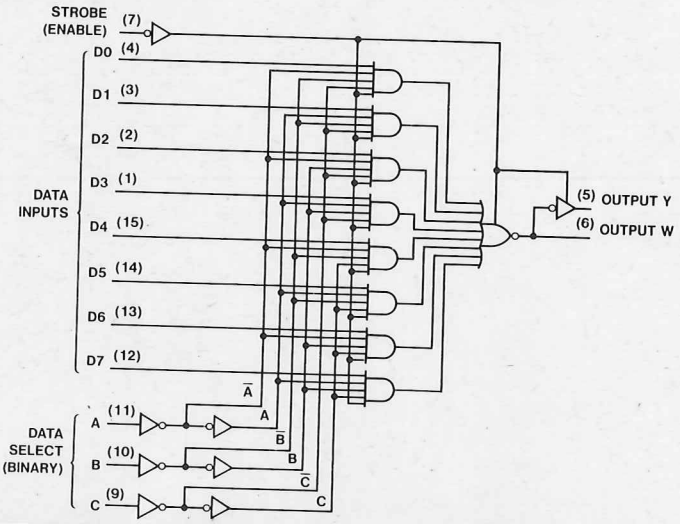
**74251 (N)**
**74LS251 (N)**
**74S251 (N)**

## Truth Table

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| Select | | | Strobe | | |
| C | B | A | S | Y | W |
| X | X | X | H | Z | Z |
| L | L | L | L | D0 | $\overline{D0}$ |
| L | L | H | L | D1 | $\overline{D1}$ |
| L | H | L | L | D2 | $\overline{D2}$ |
| L | H | H | L | D3 | $\overline{D3}$ |
| H | L | L | L | D4 | $\overline{D4}$ |
| H | L | H | L | D5 | $\overline{D5}$ |
| H | H | L | L | D6 | $\overline{D6}$ |
| H | H | H | L | D7 | $\overline{D7}$ |

H = High Logic Level, L = Low Logic Level
X = Don't Care, Z = High Impedance (Off)
D0, D1...D7 = The Level of the respective D input.

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 251 | | | DM54/74 LS251 | | | DM54/74 S251 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −12 mA | | | | −1.5 | | | | | | | V |
| | | | $I_I$ = −18 mA | | | | | | | −1.5 | | | −1.2 | |
| $I_{OH}$ | High Level Output Current | | | DM54 | | | −2 | | | −1 | | | −2 | mA |
| | | | | DM74 | | | −5.2 | | | −2.6 | | | −6.5 | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | DM54 | 2.4 | | | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| | | | | DM74 | 2.4 | | | 2.4 | 3.1 | | 2.4 | 3.2 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 16 | | | 12 | | | 20 | mA |
| | | | | DM74 | | | 16 | | | 24 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $I_{OL}$ = Max | DM54 | | | 0.4 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | DM74 | | | 0.4 | | 0.35 | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 12 mA | DM74 | | | | | 0.25 | 0.4 | | | | |
| $I_{O(OFF)}$ | Off-State (High Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $V_O$ = 0.4 V | | | | −40 | | | −20 | | | | μA |
| | | | $V_O$ = 0.5 V | | | | | | | | | | −50 | |
| | | | $V_O$ = 2.4 V (2.7 V for LS251) | | | | 40 | | | 20 | | | 50 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | | | | 1 | mA |
| | | | $V_I$ = 7 V | | | | | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | | | | | μA |
| | | | $V_I$ = 2.7 V | | | | | | | 20 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.4 V | | | | −1.6 | | | −0.4 | | | | mA |
| | | | $V_I$ = 0.5 V | | | | | | | | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | | −18 | | −70 | −20 | | −100 | −40 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | Strobe Grounded | | | 31 | 51 | | 6.1 | 10 | | 55 | 85 | mA |
| | | | Strobe at 4.5 V | | | 31 | 51 | | 7.1 | 12 | | 55 | 85 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and for DM54LS/74LS or DM54S/74S duration of short circuit should not exceed one second.

**Note 3:** All outputs open, all inputs at 4.5 V.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| | Parameter | From (Input) | To (Output) | DM54/74 LS251 | | | | DM54/74 LS251 | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A, B, or C (4 levels) | Y | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 29 | 45 | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 35 | 53 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 28 | 45 | | | 35 | 53 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A, B, or C (3 levels) | W | | | 20 | 33 | | | 25 | 38 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 21 | 33 | | | 28 | 42 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any D | Y | | | 17 | 28 | | | 23 | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 18 | 28 | | | 25 | 38 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any D | W | | | 10 | 15 | | | 16 | 25 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 9 | 15 | | | 16 | 25 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | Strobe | Y | | | 30 | 45 | | | 40 | 60 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | | | 26 | 40 | | | 34 | 51 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | Strobe | W | | | 17 | 27 | | | 26 | 40 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | | | 24 | 40 | | | 31 | 47 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | Strobe | Y | $C_L$ = 5 pF, $R_L$ = 667 Ω | | 30 | 45 | | | | | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | | | | 15 | 25 | | | | | ns |
| $t_{HZ}$ | Output Disable Time from High Level | Strobe | W | | | 37 | 55 | | | | | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | | | | 15 | 25 | | | | | ns |

## Switching Characteristics (Continued)

| Parameter | | From (Input) | To (Output) | DM54/74 251 Conditions | Min | Typ | Max | DM54/74 S251 Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A, B, or C (4 levels) | Y | $C_L$ = 50 pF, $R_L$ = 400 Ω | | 22 | 36 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 12 | 18 | ns |
| | | | | | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 14 | 21 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 23 | 36 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 13 | 19.5 | ns |
| | | | | | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 15 | 23 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A, B, or C (3 levels) | W | | | 18 | 29 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 10 | 15 | ns |
| | | | | | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 12 | 18 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 16 | 27 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 9 | 13.5 | ns |
| | | | | | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 11 | 17 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any D | Y | | | 17 | 28 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 8 | 12 | ns |
| | | | | | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 10 | 15 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 18 | 28 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 8 | 12 | ns |
| | | | | | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 10 | 15 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any D | W | | | 11 | 15 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 4.5 | 7 | ns |
| | | | | | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 6.5 | 10 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 10 | 15 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 4.5 | 7 | ns |
| | | | | | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 6.5 | 10 | |
| $t_{ZH}$ | Output Enable Time to High Level | Strobe | Y | | | 15 | 27 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 13 | 19.5 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | | | 18 | 36 | | | 14 | 21 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | Strobe | W | | | 15 | 27 | | | 13 | 19.5 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | | | 19 | 38 | | | 14 | 21 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | Strobe | Y | $C_L$ = 5 pF, $R_L$ = 400 Ω | | 4 | 8 | $C_L$ = 5 pF, $R_L$ = 280 Ω | | 5.5 | 8.5 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | | | | 14 | 23 | | | 9 | 14 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | Strobe | W | | | 4 | 8 | | | 5.5 | 8.5 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | | | | 15 | 23 | | | 9 | 14 | ns |

# TRI-STATE® Data Selectors/Multiplexers

## General Description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

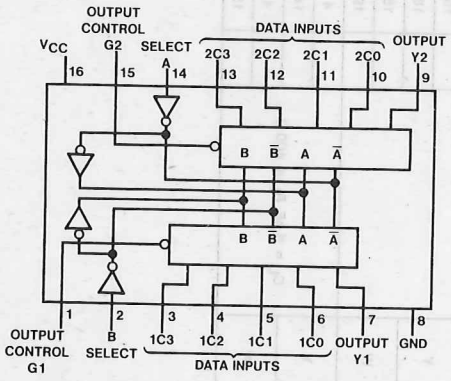
The TRI-STATE outputs can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level.

## Features

- TRI-STATE version of LS153, S153 with same pin-out
- Schottky-diode-clamped transistors
- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe/output control
- High fan-out totem-pole outputs

| Type | Typical Propagation Delay | | Typical Power Dissipation |
|---|---|---|---|
| LS253 | Data to Output | 12 ns | 35 mW |
| | Select to Output | 21 ns | |
| S253 | Data to Output | 6 ns | 275 mW |
| | Select to Output | 12 ns | |

## Connection Diagram




**54LS253 (J,W)**
**54S253 (J,W)**

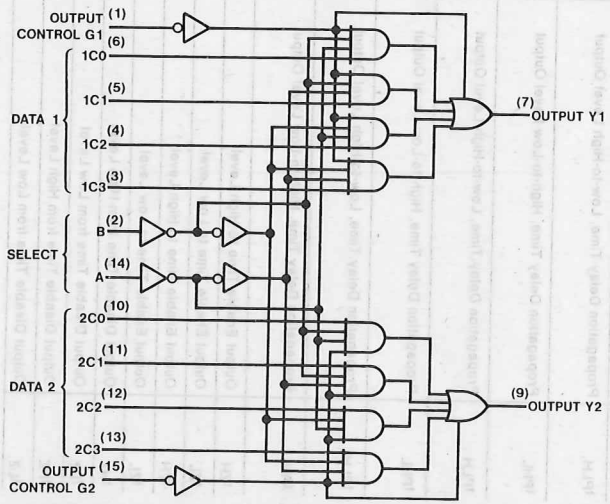
**74LS253 (N)**
**74S253 (N)**

## Truth Table

| Select Inputs | | Data Inputs | | | | Output Control | Output |
|---|---|---|---|---|---|---|---|
| B | A | C0 | C1 | C2 | C3 | G | Y |
| X | X | X | X | X | X | H | Z |
| L | L | L | X | X | X | L | L |
| L | L | H | X | X | X | L | H |
| L | H | X | L | X | X | L | L |
| L | H | X | H | X | X | L | H |
| H | L | X | X | L | X | L | L |
| H | L | X | X | H | X | L | H |
| H | H | X | X | X | L | L | L |
| H | H | X | X | X | H | L | H |

Address inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 LS253 | | | DM54/74 S253 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | | −1.5 | | | −1.2 | V |
| $I_{OH}$ | High Level Output Current | | | DM54 | | | −1 | | | −2 | mA |
| | | | | DM74 | | | −2.6 | | | −6.5 | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | DM54 | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| | | | | DM74 | 2.4 | 3.1 | | 2.7 | 3.2 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 12 | | | 20 | mA |
| | | | | DM74 | | | 24 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $I_{OL}$ = Max | DM54 | | | 0.4 | | | 0.5 | V |
| | | | | DM74 | | | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 12 mA | DM74 | | | 0.4 | | | | |
| $I_{O(OFF)}$ | Off-State (High-Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | | $V_O$ = 0.4 V | | | −20 | | | | μA |
| | | | | $V_O$ = 0.5 V | | | | | | −50 | |
| | | | | $V_O$ = 2.4 V | | | | | | 50 | |
| | | | | $V_O$ = 2.7 V | | | 20 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | | $V_I$ = 5.5 V | | | | | | 1.0 | mA |
| | | | | $V_I$ = 7 V | | | 0.1 | | | | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | | 20 | | | 50 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | | $V_I$ = 0.4 V | | | −0.4 | | | | mA |
| | | | | $V_I$ = 0.5 V | | | | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | | −20 | | −100 | −40 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | Condition A | | 7 | 12 | | | | mA |
| | | | | Condition B | | 8.5 | 14 | | | | |
| | | | | All Outputs Open | | | | | 55 | 70 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

**Note 3:** $I_{CC}$ is measured with the outputs open under the following conditions:

A. All inputs grounded.

B. Output control at 4.5 V, all inputs grounded.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | DM54/74 LS253 | | | | DM54/74 LS253 | | | | DM54/74 S253 | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Y | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 17 | 25 | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 23 | 35 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 6 | 9 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 13 | 20 | | | 20 | 30 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 8 | 12 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Select | Y | | | 30 | 45 | | | 36 | 54 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 11.5 | 18 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 21 | 32 | | | 29 | 44 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 13.5 | 21 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | Output Control | Y | | | 10 | 18 | | | 20 | 32 | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 12 | 18 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | | | 15 | 23 | | | 23 | 35 | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 14 | 21 | ns |
| $t_{HZ}$ | Output Disable Time From High Level | Output Control | Y | $C_L$ = 5 pF, $R_L$ = 667 Ω | | 27 | 41 | | | | | $C_L$ = 5 pF, $R_L$ = 280 Ω | | 13 | 19.5 | ns |
| $t_{LZ}$ | Output Disable Time From Low Level | | | | | 18 | 27 | | | | | | | 14 | 21 | ns |
| | | | | | | | | | | | | | | 5.5 | 8.5 | ns |
| | | | | | | | | | | | | | | 9 | 14 | ns |

# TRI-STATE® Quad 2-Data Selectors/Multiplexers

## General Description

These Schottky-clamped high-performance multiplexers feature TRI-STATE outputs that can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output enable circuitry is designed such that the output disable times are shorter than the output enable times.

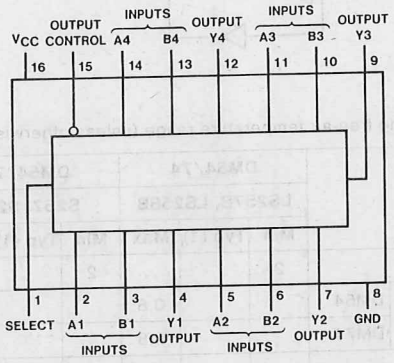
This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

## Features

- TRI-STATE versions LS157, S157, LS158, S158, with same pin-outs
- Schottky-clamped for significant improvement in A-C performance
- Provides bus interface from multiple sources in high-performance systems

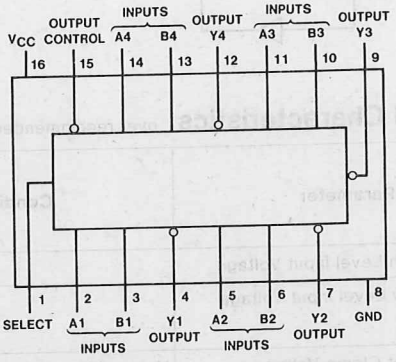
| Type | Average Propagation Delay From Data Input | Typical Power Dissipation |
|---|---|---|
| LS257B | 12 ns | 50 mW |
| LS258B | 12 ns | 35 mW |
| S257 | 4.8 ns | 320 mW |
| S258 | 4 ns | 280 mW |

## Connection Diagram




54LS257B (J,W)
54S257 (J,W)

74LS257B (N)
74S257 (N)

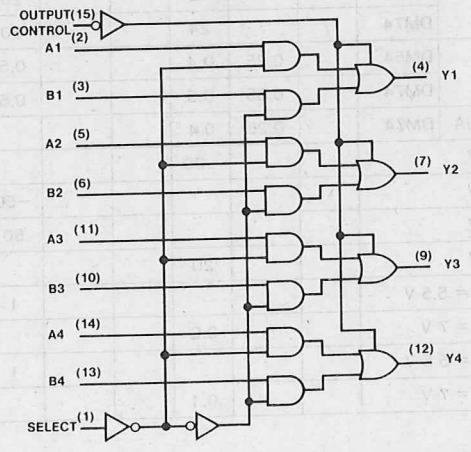



54LS258B (J,W)
54S258 (J,W)

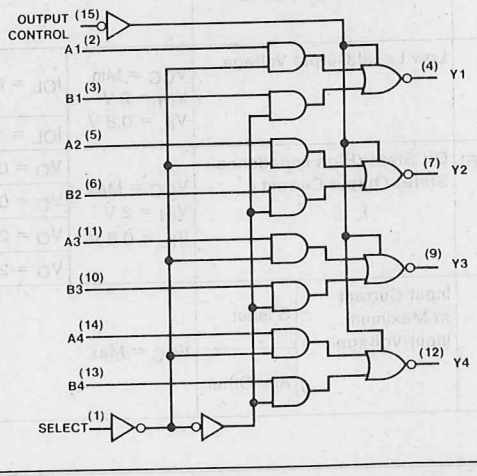
74LS258B (N)
74S258 (N)

## Logic Diagrams

LS257B

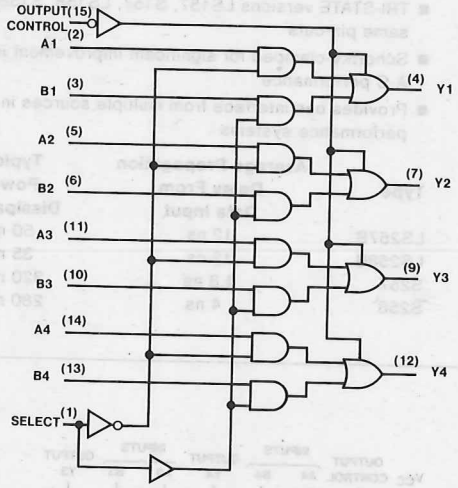



LS258B

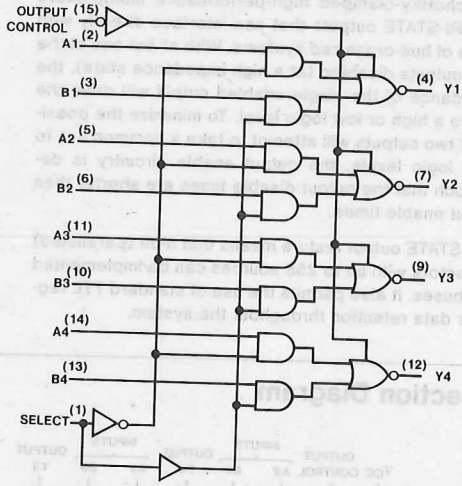


## Logic Diagrams (Continued)

S257




S258




## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 LS257B, LS258B | | | DM54/74 S257, S258 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | | −1.5 | | | −1.2 | V |
| $I_{OH}$ | High Level Output Current | | | DM54 | | | −1.0 | | | −2 | mA |
| | | | | DM74 | | | −2.6 | | | −6.5 | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | DM54 | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| | | | | DM74 | 2.4 | 3.1 | | 2.4 | 3.2 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 12 | | | 20 | mA |
| | | | | DM74 | | | 24 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $I_{OL}$ = Max | DM54 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | DM74 | | 0.35 | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 12 mA | DM74 | | 0.25 | 0.4 | | | | |
| $I_{O(OFF)}$ | Off State (High Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $V_O$ = 0.4 V | | | | −20 | | | | μA |
| | | | $V_O$ = 0.5 V | | | | | | | −50 | |
| | | | $V_O$ = 2.4 V | | | | | | | 50 | |
| | | | $V_O$ = 2.7 V | | | | 20 | | | | |
| $I_I$ | Input Current at Maximum Input Voltage | S Input | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | | | 1 | mA |
| | | | | $V_I$ = 7 V | | | 0.2 | | | | |
| | | Any Other | | $V_I$ = 5.5 V | | | | | | 1 | |
| | | | | $V_I$ = 7 V | | | 0.1 | | | | |

## Electrical Characteristics (Continued)

| Parameter | | | Conditions | | DM54/74 LS257B, LS258B | | | DM54/74 S257, S258 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $I_{IH}$ | High Level Input Current | S Input | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | 40 | | | 100 | μA |
| | | Any Other | | | | | 20 | | | 50 | |
| $I_{IL}$ | Low Level Input Current | S Input | $V_{CC}$ = Max | $V_I$ = 0.4 V | | | −0.8 | | | | mA |
| | | | | $V_I$ = 0.5 V | | | | | | −4 | |
| | | Any Other | | $V_I$ = 0.4 V | | | −0.4 | | | | |
| | | | | $V_I$ = 0.5 V | | | | | | −2 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | −20 | | −100 | −40 | | −100 | mA |
| $I_{CC}$ | Supply Current | All Outputs High | $V_{CC}$ = Max (3) | LS257B, S257 | | 5.9 | 10 | | 44 | 68 | mA |
| | | All Outputs Low | | | | 9.2 | 16 | | 60 | 93 | |
| | | All Outputs Off | | | | 12 | 19 | | 64 | 99 | |
| | | All Outputs High | | LS258B, S258 | | 4.1 | 7 | | 36 | 56 | |
| | | All Outputs Low | | | | 9 | 14 | | 52 | 81 | |
| | | All Outputs Off | | | | 12 | 19 | | 56 | 87 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

**Note 3:** $I_{CC}$ is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.

## Truth Table

| Inputs | | | | Output Y | |
|---|---|---|---|---|---|
| Output Control | Select | A | B | LS257 S257 | LS258 S258 |
| H | X | X | X | Z | Z |
| L | L | L | X | L | H |
| L | L | H | X | H | L |
| L | H | X | L | L | H |
| L | H | X | H | H | L |

H = High Level, L = Low Level, X = Don't Care
Z = High Impedance (off)

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | DM54/74 LS257B, LS258B Conditions | Min | Typ | Max | DM54/74 LS257B, LS258B Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Any | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 12 | 18 | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 18 | 27 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 12 | 18 | | | 18 | 27 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Select | Any | | | 18 | 28 | | | 23 | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 22 | 35 | | | 28 | 42 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | Output Control | Any | | | 8 | 15 | | | 18 | 27 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | | | 17 | 28 | | | 25 | 38 | ns |
| $t_{HZ}$ | Output Disable Time From High Level | Output Control | Any | $C_L$ = 5 pF, $R_L$ = 667 Ω | | 17 | 26 | | | | | ns |
| $t_{LZ}$ | Output Disable Time From Low Level | | | | | 14 | 25 | | | | | ns |

## Switching Characteristics (Continued)

| Parameter | | From (Input) | To (Output) | DM54/74 Conditions | S257 Min | S257 Typ | S257 Max | S258 Min | S258 Typ | S258 Max | Conditions | S257 Min | S257 Typ | S257 Max | S258 Min | S258 Typ | S258 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Any | $C_L$ = 50 pF $R_L$ = 280 Ω | | 7 | 11 | | 6 | 9 | $C_L$ = 15 pF $R_L$ = 280 Ω | | 5 | 7.5 | | 4 | 6 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 6.5 | 10 | | 6 | 9 | | | 4.5 | 6.5 | | 4 | 6 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Select | Any | | | 10.5 | 16 | | 10 | 15 | | | 8.5 | 15 | | 8 | 12 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 10.5 | 16 | | 9.5 | 15 | | | 8.5 | 15 | | 7.5 | 12 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | Output Control | Any | | | 15 | 23 | | 15 | 23 | | | 13 | 19.5 | | 13 | 19.5 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | | | 16 | 24 | | 16 | 24 | | | 14 | 21 | | 14 | 21 | ns |
| $t_{HZ}$ | Output Disable Time From High Level | Output Control | Any | | | | | | | | $C_L$ = 5 pF $R_L$ = 280 Ω | | 5.5 | 8.5 | | 5.5 | 8.5 | ns |
| $t_{LZ}$ | Output Disable Time From Low Level | | | | | | | | | | | | 9 | 14 | | 9 | 14 | ns |

# 8-Bit Addressable Latches

## General Description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear and enable inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possiblity of entering erroneous data in the latches, the enable should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

## Features

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion With Storage
- Asynchronous Parallel Clear
- Active High Decoder
- Enable/Disable Input Simplifies Expansion
- Direct Replacement for Fairchild 9334
- Expandable for N-Bit Applications
- Four Distinct Functional Modes
- Typical Propagation Delay Times:

| | '259 | 'LS259 |
|---|---|---|
| Enable-to-Output | 18 ns | 18 ns |
| Data-to-Output | 21 ns | 16 ns |
| Address-to-Output | 22 ns | 21 ns |
| Clear-to-Output | 21 ns | 17 ns |

- Fan-Out

$I_{OL}$ (Sink Current)

| | |
|---|---|
| '259 | 16 mA |
| 54LS259 | 4 mA |
| 74LS259 | 8 mA |

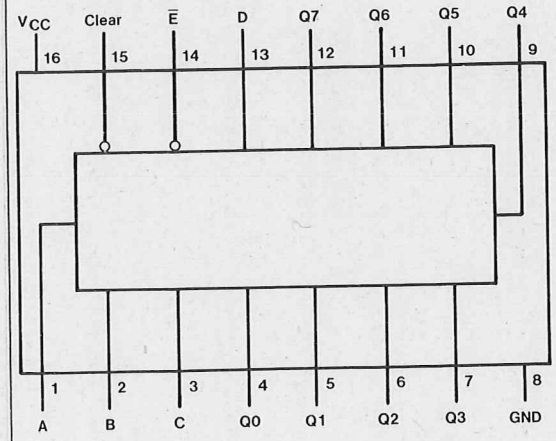
$I_{OH}$ (Source Current)

| | |
|---|---|
| '259 | −0.8 mA |
| 'LS259 | −0.4 mA |

- Typical $I_{CC}$

| | |
|---|---|
| '259 | 60 mA |
| 'LS259 | 22 mA |

## Connection Diagram




**54259 (J,W)**
**54LS259 (J,W)**

**74259 (N)**
**74LS259 (N)**

## Truth Table

| Inputs | | Output Of Addressed Latch | Each Other Output | Function |
|---|---|---|---|---|
| Clear | $\overline{E}$ | | | |
| H | L | D | $Q_{i0}$ | Addressable Latch |
| H | H | $Q_{i0}$ | $Q_{i0}$ | Memory |
| L | L | D | L | 8-Line Demultiplexer |
| L | H | L | L | Clear |

**Latch Selection Table**

| Select Inputs | | | Latch Addressed |
|---|---|---|---|
| C | B | A | |
| L | L | L | 0 |
| L | L | H | 1 |
| L | H | L | 2 |
| L | H | H | 3 |
| H | L | L | 4 |
| H | L | H | 5 |
| H | H | L | 6 |
| H | H | H | 7 |

H = high level, L = low level

D = the level of the data input

$Q_{i0}$ = the level of $Q_i$ (i = 0, 1, . . . 7, as appropriate) before the indicated steady-state input conditions were established.

6

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 259 | | | DM54/74 LS259 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −18 mA | | | | | | | −1.5 | V |
| | | | $I_I$ = −12 mA | | | | −1.5 | | | | |
| $I_{OH}$ | High Level Output Current | | | | | | −800 | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| $I_{OL}$ | Low Level Output Current | | DM54 | | | | 16 | | | 4 | mA |
| | | | DM74 | | | | 16 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = Max | | DM54 | | 0.2 | 0.4 | | 0.25 | 0.4 | V |
| | | | | DM74 | | 0.2 | 0.4 | | 0.35 | 0.5 | |
| | | | | $I_{OL}$ = 4 mA | | | | | 0.25 | 0.4 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 5.5 V | | | | 1 | | | | mA |
| | | | $V_I$ = 7 V | | | | | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.4 V | | | | 40 | | | | μA |
| | | | $V_I$ = 2.7 V | | | | | | | 20 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | | −1.6 | | | −0.4 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | | −20 | | −55 | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | | | 30 | 48 | | 22 | 36 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time and for the DM54LS/74LS duration of short should not exceed one second.

**Note 3:** $I_{CC}$ is measured with 4.5 V applied to all inputs and all outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From | To | DM54/74 259 | | | | DM54/74 LS259 | | | | DM54/74 LS259 | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Enable | Output | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 19 | 28 | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 22 | 35 | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 25 | 38 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 18 | 27 | | | 15 | 24 | | | 21 | 32 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Output | | | 24 | 35 | | | 20 | 32 | | | 23 | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 19 | 28 | | | 13 | 21 | | | 20 | 30 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Output | Address | Output | | | 23 | 35 | | | 24 | 38 | | | 27 | 41 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 21 | 35 | | | 18 | 29 | | | 25 | 38 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Clear | Output | | | 21 | 31 | | | 17 | 27 | | | 24 | 36 | ns |
| $t_W$ | Enable and Clear Pulse Width | | | | 19 | 13 | | | 15 | | | | 15 | | | ns |
| $t_{SETUP}$ | Data to Enable (4) | | | | 20 | 13 | | | 15↑ | | | | 15↑ | | | ns |
| | Address to Enable (3)(4) | | | | 10 | 5 | | | 15↓ | | | | 15↓ | | | ns |
| $t_{HOLD}$ | Data to Enable (4) | | | | 0 | −10 | | | 0↑ | | | | 0↑ | | | ns |
| | Address to Enable (4) | | | | 0 | −13 | | | 0↑ | | | | 0↑ | | | ns |

**Note 3:** The Address to Enable Set-Up Time is the time before the High-to-Low Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

**Note 4:** ↑ The arrow indicates that the rising edge of the Enable Pulse is used for reference. ↓ The arrow indicates that the falling edge of the Enable Pulse is used for reference.

# 9-Bit Parity Generators/Checkers

## General Description

These universal, nine-bit parity generators/checkers utilize Schottky-clamped TTL high-performance circuitry, and feature odd/even outputs to facilitate operation of either odd or even parity applications. The word-length capability is easily expanded by cascading.

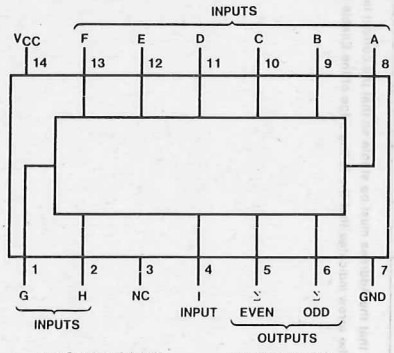
The S280 can be used to upgrade the performance of most systems utilizing the DM74180 parity generator/checker. Although the S280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4, and no internal connection at pin 3. This permits the S280 to be substituted for the 180 in existing designs to produce an identical function, even if S280's are mixed with existing 180's.

Input buffers are provided so that each input represents only one normal 74S load, and full fan-out to 10 normal Series 74S loads is available from each of the outputs at low logic levels. A fan-out to 20 normal Series 74S loads is provided at high logic levels, to facilitate connection of unused inputs to used inputs.

## Features

- Generates either odd or even parity for nine data lines
- Cascadable for n-bits
- Can be used to upgrade existing systems using MSI parity circuits
- Typical data-to-output delay—14 ns

## Connection Diagram

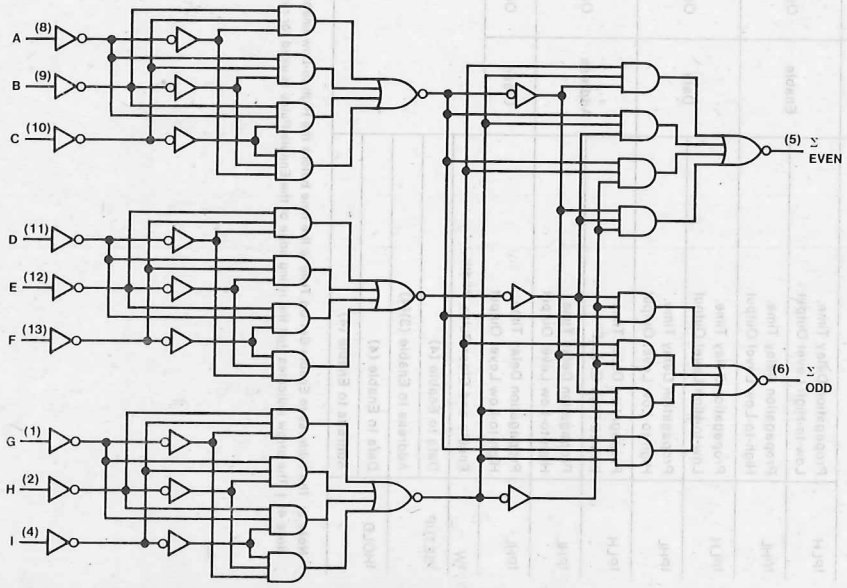



54S280 (J,W) 74S280 (N)

## Truth Table

| Number of Inputs (A Thru I) that are High | Outputs | |
|---|---|---|
| | Σ Even | Σ Odd |
| 0, 2, 4, 6, 8 | H | L |
| 1, 3, 5, 7, 9 | L | H |

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | DM54/74 S280 | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ(1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | −1.2 | V |
| $I_{OH}$ | High Level Output Current | | | | −1 | mA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OH}$ = −1 mA | 2.7 | 3.4 | | V |
| $I_{OL}$ | Low Level Output Current | | | | 20 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 20 mA | | | 0.5 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | 50 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.5 V | | | −2 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | −40 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | 67 | 105 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
**Note 3:** $I_{CC}$ is measured with all inputs grounded and all outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Conditions | DM54/74 S280 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Σ Even | $C_L$ = 15 pF, $R_L$ = 180 Ω | | 14 | 21 | ns |
| | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 16 | 24 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 15 pF, $R_L$ = 180 Ω | | 11.5 | 18 | |
| | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 13.5 | 21 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Σ Odd | $C_L$ = 15 pF, $R_L$ = 180 Ω | | 14 | 21 | ns |
| | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 16 | 24 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 15 pF, $R_L$ = 180 Ω | | 11.5 | 18 | |
| | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 13.5 | 21 | |

## Typical Applications

Three S280's can be used to implement a 25-line parity generator/checker. This arrangement will provide parity in typically 25 ns. (See *Figure 1.*)

As an alternative, the outputs of two or three parity generators/checkers can be decoded with a 2-input (S86) or 3-input (S135) exclusive-OR gate for 18 or 27-line parity applications.

Longer word lengths can be implemented by cascading S280's. As shown in *Figure 2*, parity can be generated for word lengths up to 81 bits in typically 25 ns.

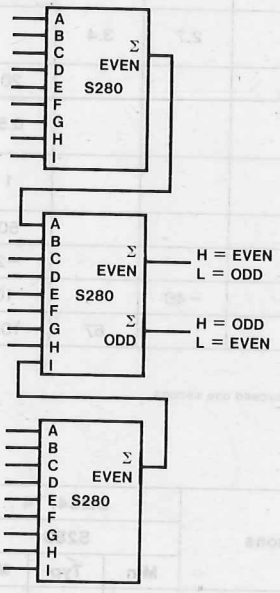



FIGURE 1. 25-Line Parity/Generator Checker

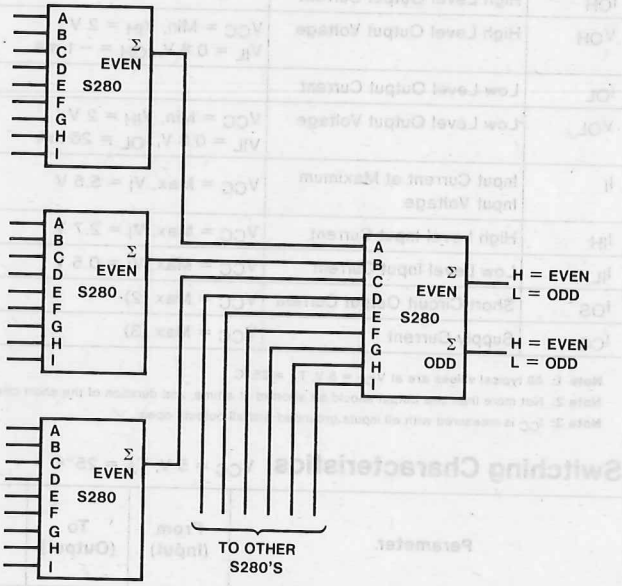



FIGURE 2. 81-Line Parity/Generator Checker

# Decade and 4-Bit Binary Counters

## General Description

The DM54LS290/DM74LS290 and 54LS293/74LS293 counters are electrically and functionally identical to the 54LS90/74LS90 and 54LS93/74LS93, respectively. Only the arrangement of the terminals has been changed for the 'LS290 and 'LS293.

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 'LS290 and divide-by-eight for the 'LS293.

All of these counters have a gated zero reset and the 'LS290 also has gated set-to-nine inputs for use in BCD nine's complement applications.

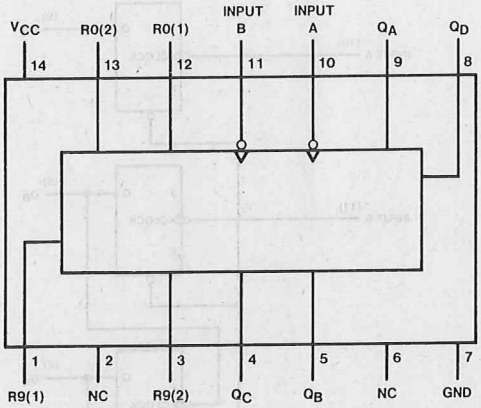
To use the maximum count length (decade or four-bit binary) of these counters, the B input is connected to the $Q_A$ output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the 'LS290 counter by connecting the $Q_D$ output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output $Q_A$.

## Features

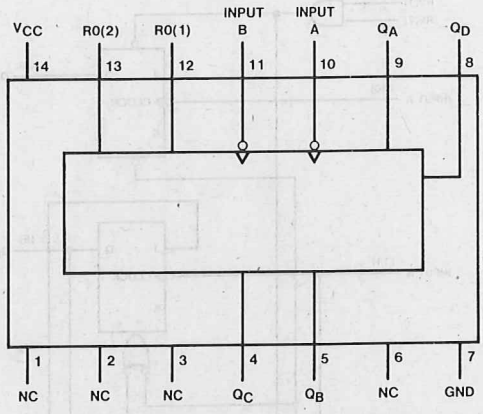
- GND and $V_{CC}$ on Corner Pins (Pins 7 and 14 respectively)

| Type | Typical Power Dissipation | Count Frequency |
|---|---|---|
| LS290 | 45 mW | 42 MHz |
| LS293 | 45 mW | 42 MHz |

## Connection Diagrams




54LS290 (J,W) 74LS290 (N)




54LS293 (J,W) 74LS293 (N)

## Truth Tables

LS290
BCD COUNT SEQUENCE
(See Note A)

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

Note A: Output $Q_A$ is connected to input B for BCD count.

LS290
BI-QUINARY (5-2)
(See Note B)

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_A$ | $Q_D$ | $Q_C$ | $Q_B$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

Note B: Output $Q_D$ is connected to input A for bi-quinary count.

6

## Truth Tables (Continued)

**LS293**
**COUNT SEQUENCE**
**(See Note C)**

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

**Note C:** Output $Q_A$ is connected to input B.

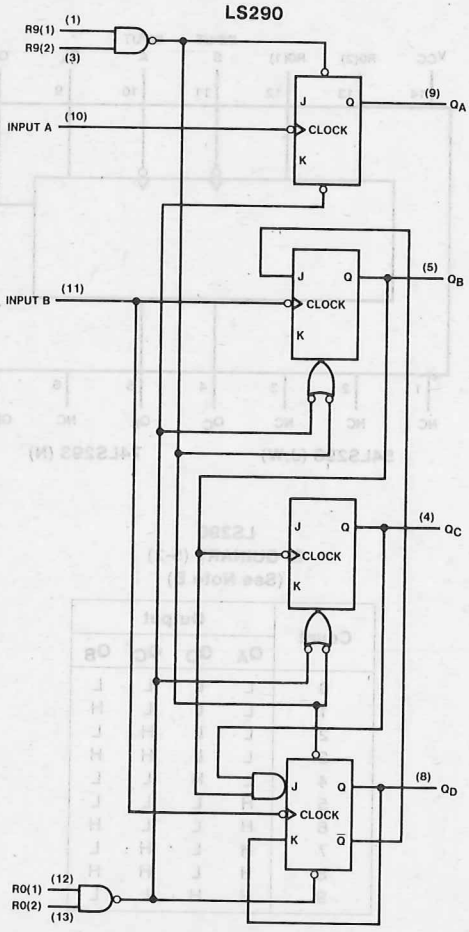
**LS293**
**RESET/COUNT TRUTH TABLE**

| Reset Inputs | | Output | | | |
|---|---|---|---|---|---|
| R0(1) | R0(2) | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | L | L | L |
| L | X | COUNT | | | |
| X | L | COUNT | | | |

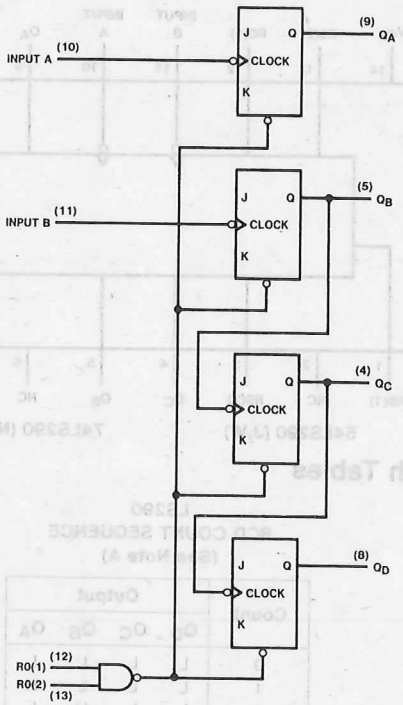
**Note D:** H = High Level, L = Low Level, X = Don't Care.

## Logic Diagrams

**LS290**




**LS293**




The J and K inputs shown without connection are for reference only and are functionally at a high level.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM54/74 LS290, LS293 Min | Typ (1) | Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | DM54 | | | 0.8 | V |
| | | | | | DM74 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min | $I_I$ = −18 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | DM54 | 2.5 | 3.4 | | V |
| | | | | | DM74 | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 4 | mA |
| | | | | | DM74 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $I_{OL}$ = Max | DM54 | | 0.25 | 0.4 | V |
| | | | | | DM74 | | 0.35 | 0.5 | |
| | | | | $I_{OL}$ = 4 mA | DM74 | | 0.25 | 0.4 | |
| $I_I$ | Input Current at Maximum Input Voltage | Any Reset | $V_{CC}$ = Max, $V_I$ = 7 V | | | | | 0.1 | mA |
| | | A Input | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | | 0.2 | |
| | | B Input | | | LS290 | | | 0.4 | |
| | | | | | LS293 | | | 0.2 | |
| $I_{IH}$ | High Level Input Current | Any Reset | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | | 20 | μA |
| | | A Input | | | | | | 40 | |
| | | B Input | | | LS290 | | | 80 | |
| | | | | | LS293 | | | 40 | |
| $I_{IL}$ | Low Level Input Current | Any Reset | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | | −0.4 | mA |
| | | A Input | | | | | | −2.4 | |
| | | B Input | | | LS290 | | | −3.2 | |
| | | | | | LS293 | | | −1.6 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | DM54 | −20 | | −100 | mA |
| | | | | | DM74 | −20 | | −100 | |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (3) | | LS290 | | 9 | 15 | mA |
| | | | | | LS293 | | 9 | 15 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.

**Note 2:** Not more than one output to be shorted at a time and duration not to exceed one second.

**Note 3:** $I_{CC}$ is measured with all outputs open, both $R_O$ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | To (Output) | DM54/74 Conditions | DM54/74 LS290 Min | DM54/74 LS290 Typ | DM54/74 LS290 Max | DM54/74 LS293 Min | DM54/74 LS293 Typ | DM54/74 LS293 Max | DM54/74 Conditions | DM74 LS290 Min | DM74 LS290 Typ | DM74 LS290 Max | DM74 LS293 Min | DM74 LS293 Typ | DM74 LS293 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Count Frequency | | A | $Q_A$ | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 32 | 42 | | 32 | 42 | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 20 | 30 | | 20 | 30 | | MHz |
| | | | B | $Q_B$ | | 16 | | | 16 | | | | 10 | | | 10 | | | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | A | $Q_A$ | | | 10 | 16 | | 10 | 16 | | | 15 | 23 | | 15 | 23 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 12 | 18 | | 12 | 18 | | | 20 | 30 | | 20 | 30 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | A | $Q_D$ | | | 32 | 48 | | 46 | 70 | | | 40 | 60 | | 58 | 87 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 34 | 50 | | 46 | 70 | | | 45 | 68 | | 62 | 93 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | B | $Q_B$ | | | 10 | 16 | | 10 | 16 | | | 15 | 23 | | 15 | 23 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 14 | 21 | | 14 | 21 | | | 23 | 35 | | 23 | 35 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | B | $Q_C$ | | | 21 | 32 | | 21 | 32 | | | 32 | 48 | | 32 | 48 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 23 | 35 | | 23 | 35 | | | 35 | 53 | | 35 | 53 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | B | $Q_D$ | | | 21 | 32 | | 34 | 51 | | | 32 | 48 | | 47 | 71 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 23 | 35 | | 34 | 51 | | | 35 | 53 | | 47 | 71 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Set-to-0 | Any | | | 26 | 40 | | 26 | 40 | | | 35 | 53 | | 35 | 53 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Set-to-9 | $Q_A$, $Q_D$ | | | 20 | 30 | | | | | | 25 | 38 | | | | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $Q_B$, $Q_C$ | | | 26 | 40 | | | | | | 35 | 53 | | | | |
| $t_W$ | Pulse Width | A Input | | | | 15 | | | 15 | | | | 15 | | | 15 | | | ns |
| | | B Input | | | | 30 | | | 30 | | | | 30 | | | 30 | | | |
| | | Reset Input | | | | 15 | | | 15 | | | | 15 | | | 15 | | | |
| $t_{SETUP}$ | Reset Inactive State Setup Time | | | | | 25 | | | 25 | | | | 25 | | | 25 | | | ns |

# Quad 2-Multiplexers with Storage

## General Description

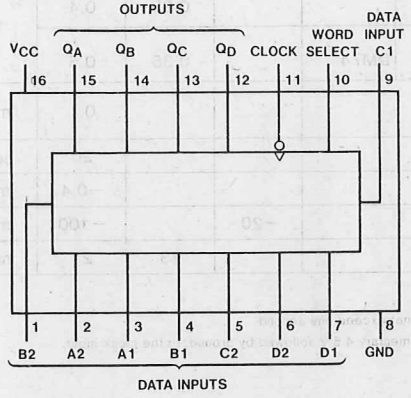
These integrated circuits provide essentially the equivalent functional capabilities of two separate MSI functions (DM54157/DM74157 or DM54LS157/DM74LS157 and DM54175/DM74175 or DM54LS175/DM74LS175) in a single 16-pin package.

When the word-select input is low, word 1 (A1, B1, C1, D1) is entered into the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is then clocked to the output terminals on the negative-going edge of the clock pulse.

## Features

- Selects one of two 4-bit data sources and stores data synchronously with system clock
- Applications:
  - Dual source for operands and constants in arithmetic processor; can release processor register files for acquiring new data
  - Implement separate registers capable of parallel exchange of contents, yet retain external load capability
  - Universal type register for implementing various shift patterns; even has compound left-right capabilities

## Connection Diagram



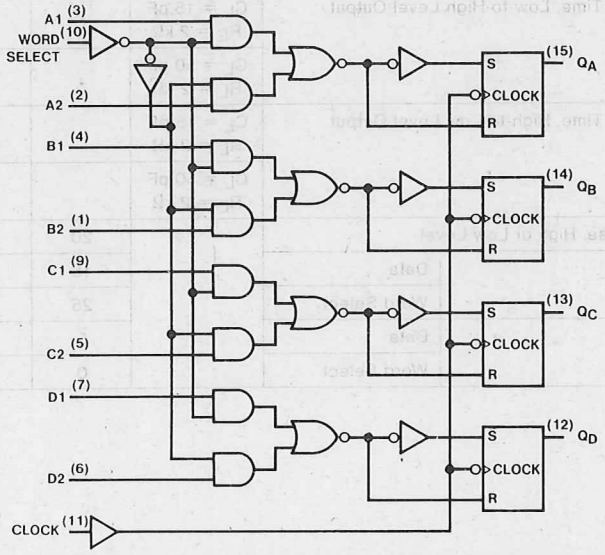

54LS298 (J,W)/74LS298 (N)

## Truth Table

| Inputs | | Outputs | | | |
|---|---|---|---|---|---|
| Word Select | Clock | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| L | ↓ | a1 | b1 | c1 | d1 |
| H | ↓ | a2 | b2 | c2 | d2 |
| X | H | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↓ = Transition from high to low level
a1,a2, etc. = The level of steady-state input at A1, A2, etc.
$Q_{A0}$, $Q_{B0}$, etc. = The level of $Q_A$, $Q_B$, etc. entered on the most recent ↓ transition of the clock input.

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM54/74 LS298 Min | Typ (1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | DM54 | | | 0.8 | V |
| | | | DM74 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −400 μA | DM54 | 2.5 | 3.4 | | V |
| | | | DM74 | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | DM54 | | | 4 | mA |
| | | | DM74 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 4 mA | | | 0.25 | 0.4 | V |
| | | $I_{OL}$ = 8 mA | DM74 | | 0.35 | 0.5 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 7 V | | | | 0.1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | 20 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −0.4 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | | 13 | 21 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

**Note 3:** With all outputs open and all inputs except clock low, $I_{CC}$ is measured after applying a momentary 4.5 V, followed by ground, to the clock input.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | DM54/DM74 LS298 Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 18 | 27 | ns |
| | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 21 | 32 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 21 | 32 | ns |
| | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 27 | 41 | ns |
| $t_W$ | Width of Clock Pulse, High or Low Level | | | 20 | | | ns |
| $t_{SETUP}$ | Setup Time | Data | | 15 | | | ns |
| | | Word Select | | 25 | | | |
| $t_{HOLD}$ | Hold Time | Data | | 5 | | | |
| | | Word Select | | 0 | | | |

## Typical Applications

*Figure 1* illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.

When the word select input is high and the registers are clocked, the contents of register 1 is transferred (shifted) to register 2, etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered into the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

Another function that can be implemented with the LS298 is a register that can be designed specifically for supporting multiplier or division operations. *Figure 2* is an example of a one place/two place shift register.

When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALU's) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.

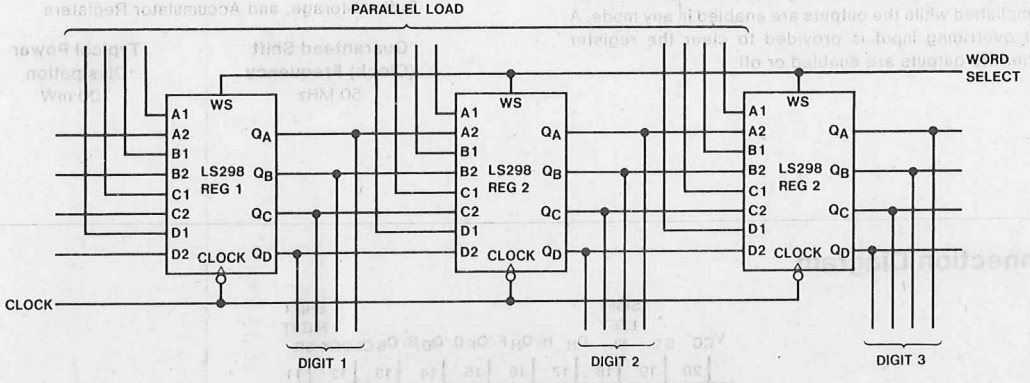



FIGURE 1

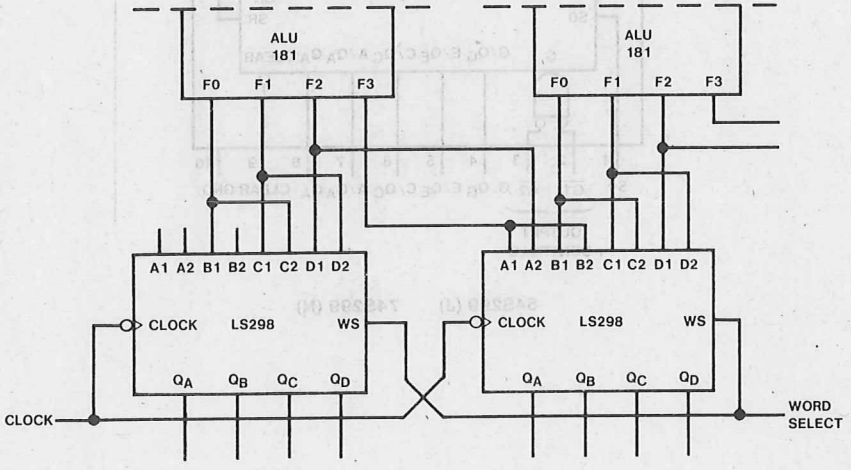



FIGURE 2

# TRI-STATE® 8-Bit Universal Shift/Storage Registers

## Description

This Schottky TTL eight-bit universal register features multiplexed inputs/outputs to achieve full eight bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

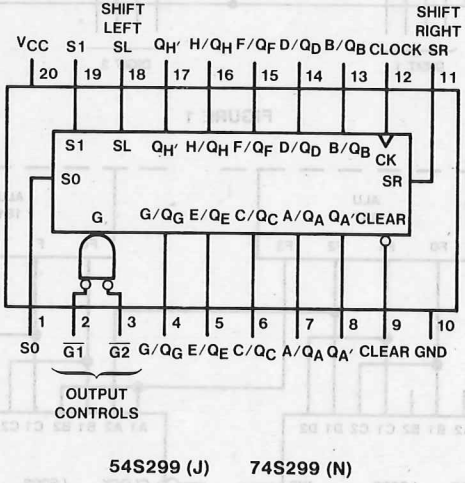
Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the TRI-STATE outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

## Features

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operation:
  Hold (Store) Shift Left
  Shift Right Load Data
- Operates with Outputs Enabled or at High Z
- TRI-STATE Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- Applications:
  Stacked or Push-Down Registers.
  Buffer Storage, and Accumulator Registers

| Guaranteed Shift (Clock) Frequency | Typical Power Dissipation |
|---|---|
| 50 MHz | 700 mW |

## Connection Diagram



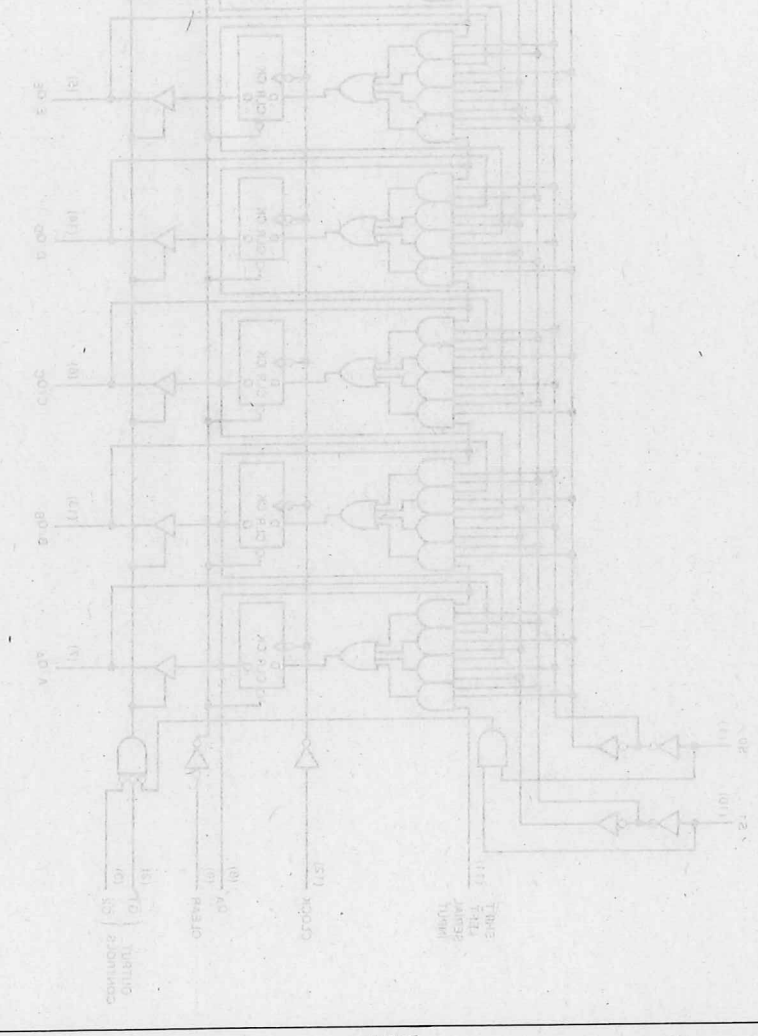

**54S299 (J)** **74S299 (N)**

## Truth Table

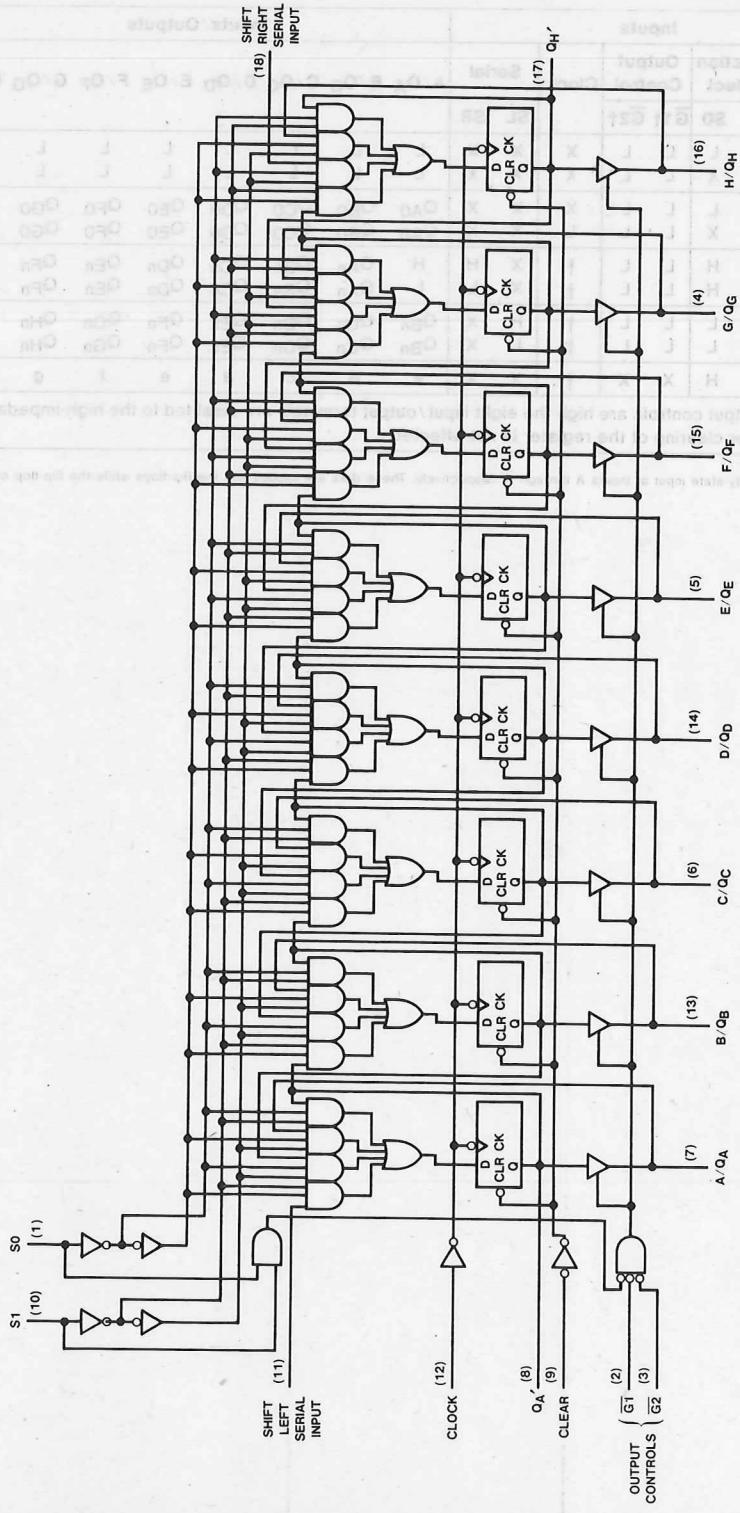
| Mode | Inputs | | | | | | | Inputs/Outputs | | | | | | | | Outputs | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Clear | Function Select | | Output Control | | Clock | Serial | $A/Q_A$ | $B/Q_B$ | $C/Q_C$ | $D/Q_D$ | $E/Q_E$ | $F/Q_F$ | $G/Q_G$ | $H/Q_H$ | $Q_{A'}$ | $Q_{H'}$ |
| | | S1 | S0 | $\overline{G}1$† | $\overline{G}2$† | | SL SR | | | | | | | | | | |
| Clear | L | X | L | L | L | X | X X | L | L | L | L | L | L | L | L | L | L |
| | L | L | X | L | L | X | X X | L | L | L | L | L | L | L | L | L | L |
| Hold | H | L | L | L | L | X | X X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $Q_{E0}$ | $Q_{F0}$ | $Q_{G0}$ | $Q_{H0}$ | $Q_{A0}$ | $Q_{H0}$ |
| | H | X | X | L | L | L | X X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $Q_{E0}$ | $Q_{F0}$ | $Q_{G0}$ | $Q_{H0}$ | $Q_{A0}$ | $Q_{H0}$ |
| Shift Right | H | L | H | L | L | ↑ | X H | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | H | $Q_{Gn}$ |
| | H | L | H | L | L | ↑ | X L | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | L | $Q_{Gn}$ |
| Shift Left | H | H | L | L | L | ↑ | H X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | $Q_{Hn}$ | H | $Q_{Bn}$ | H |
| | H | H | L | L | L | ↑ | L X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | $Q_{Hn}$ | L | $Q_{Bn}$ | L |
| Load | H | H | H | X | X | ↑ | X X | a | b | c | d | e | f | g | h | a | h |

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a...h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.



## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | DM54/74 S299 Min | DM54/74 S299 Typ (1) | DM54/74 S299 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | −1.2 | V |
| $I_{OH}$ | High Level Output Current | $Q_{A'}$ or $Q_{H'}$ | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | | | | −0.5 | mA |
| | | $Q_A$ thru $Q_H$ | | DM54 | | | −2 | |
| | | | | DM74 | | | −6.5 | |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | $Q_A$ thru $Q_H$ | 2.4 | 3.2 | | V |
| | | | | $Q_{A'}$ or $Q_{H'}$ | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | $Q_A$ thru $Q_H$ | | | 20 | mA |
| | | | | $Q_{A'}$ or $Q_{H'}$ | | | 6 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = Max | | | | 0.5 | V |
| $I_{O(OFF)}$ | Off-State (High Impedance State) Output Current | $Q_A$ thru $Q_H$ | $V_{CC}$ = Max, $V_{IH}$ = 2 V | $V_O$ = 0.5 V | | | −250 | μA |
| | | | | $V_O$ = 2.4 V | | | 100 | |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | | $V_{CC}$ = Max, $V_I$ = 2.7 V | A thru H, S0, S1 | | | 100 | μA |
| | | | | Any Other | | | 50 | |
| $I_{IL}$ | Low Level Input Current | | $V_{CC}$ = Max, $V_I$ = 0.5 V | Clock or Clear | | | −2 | mA |
| | | | | Any Other | | | −250 | μA |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | $Q_A$ thru $Q_H$ | −40 | | −100 | mA |
| | | | | $Q_{A'}$ or $Q_{H'}$ | −20 | | −100 | |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max | | | 140 | 225 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time not to exceed one second duraiton.

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## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | To (Output) | Conditions | DM54/74 S299 Min | DM54/74 S299 Typ | DM54/74 S299 Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | | | | See note (3) | 50 | 70 | | MHz |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | | Clock | $Q_{A'}$ or $Q_{H'}$ | $C_L$ = 15 pF, $R_L$ = 1 kΩ | | 12 | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | Clock | $Q_{A'}$ or $Q_{H'}$ | $C_L$ = 15 pF, $R_L$ = 1 kΩ | | 13 | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | Clear | $Q_{A'}$ or $Q_{H'}$ | $C_L$ = 15 pF, $R_L$ = 1 kΩ | | 14 | 21 | ns |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | | Clock | $Q_A$ thru $Q_H$ | $C_L$ = 45 pF, $R_L$ = 280 Ω | | 15 | 21 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | Clock | $Q_A$ thru $Q_H$ | $C_L$ = 45 pF, $R_L$ = 280 Ω | | 15 | 21 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | Clear | $Q_A$ thru $Q_H$ | $C_L$ = 45 pF, $R_L$ = 280 Ω | | 16 | 24 | ns |
| $t_{PZH}$ | Output Enable Time to High Level | | $\overline{G}_1$, $\overline{G}_2$ | $Q_A$ thru $Q_H$ | $C_L$ = 45 pF, $R_L$ = 280 Ω | | 10 | 18 | ns |
| $t_{PZL}$ | Output Enable Time to Low Level | | $\overline{G}_1$, $\overline{G}_2$ | $Q_A$ thru $Q_H$ | $C_L$ = 45 pF, $R_L$ = 280 Ω | | 12 | 18 | ns |
| $t_{PHZ}$ | Output Disable Time From High Level | | $\overline{G}_1$, $\overline{G}_2$ | $Q_A$ thru $Q_H$ | $C_L$ = 5 pF, $R_L$ = 280 Ω | | 7 | 12 | ns |
| $t_{PLZ}$ | Output Disable Time From Low Level | | $\overline{G}_1$, $\overline{G}_2$ | $Q_A$ thru $Q_H$ | $C_L$ = 5 pF, $R_L$ = 280 Ω | | 7 | 12 | ns |
| $t_W$ | Pulse Width | Clock High<br>Clock Low<br>Clear Low | | | | 10<br>10<br>10 | | | ns |
| $t_{SU}$ | Setup Time | Select<br>High Level<br>Data (4)<br>Low Level<br>Data (4)<br>Clear Inactive<br>State | | | | 15↑<br>7↑<br>5↑<br>10↑ | | | ns |
| $t_n$ | Hold Time | Select<br>Data (4) | | | | 5↑<br>5↑ | | | ns |

**Note 3:** For testing $f_{MAX}$ all outputs are loaded simultaneously.

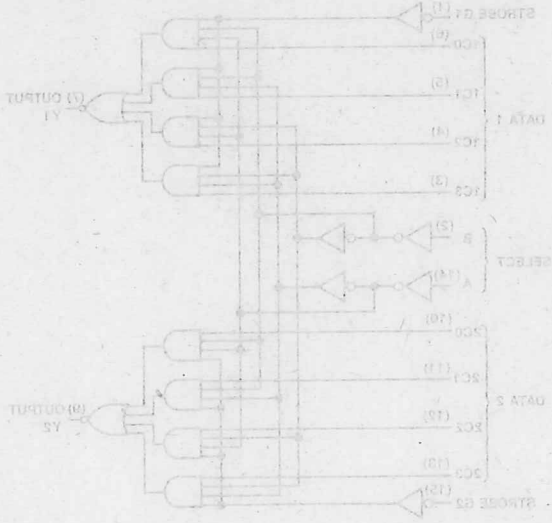
**Note 4:** Data includes the two serial inputs and the eight input/output data lines.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | To (Output) | Conditions | DM54/74 S299 | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | | | See note (3) | 40 | 60 | | MHz |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | | Clock | $Q_{A'}$ or $Q_{H'}$ | $C_L$ = 50 pF, $R_L$ = 1 kΩ | | 15 | 23 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | Clock | $Q_{A'}$ or $Q_{H'}$ | $C_L$ = 50 pF, $R_L$ = 1 kΩ | | 19 | 29 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | Clear | $Q_{A'}$ or $Q_{H'}$ | $C_L$ = 50 pF, $R_L$ = 1 kΩ | | 20 | 30 | ns |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | | Clock | $Q_A$ thru $Q_H$ | $C_L$ = 150 pF, $R_L$ = 280 Ω | | 18 | 27 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | Clock | $Q_A$ thru $Q_H$ | $C_L$ = 150 pF, $R_L$ = 280 Ω | | 18 | 27 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | Clear | $Q_A$ thru $Q_H$ | $C_L$ = 150 pF, $R_L$ = 280 Ω | | 19 | 29 | ns |
| $t_{PZH}$ | Output Enable Time to High Level | | $\overline{G}_1$, $\overline{G}_2$ | $Q_A$ thru $Q_H$ | $C_L$ = 150 pF, $R_L$ = 280 Ω | | 13 | 20 | ns |
| $t_{PZL}$ | Output Enable Time to Low Level | | $\overline{G}_1$, $\overline{G}_2$ | $Q_A$ thru $Q_H$ | $C_L$ = 150 pF, $R_L$ = 280 Ω | | 16 | 24 | ns |
| $t_W$ | Pulse Width | Clock High | | | | 10 | | | ns |
| | | Clock Low | | | | 10 | | | |
| | | Clear Low | | | | 10 | | | |
| $t_{SU}$ | Setup Time | Select | | | | 15↑ | | | ns |
| | | High Level Data (4) | | | | 7↑ | | | |
| | | Low Level Data (4) | | | | 5↑ | | | |
| | | Clear Inactive State | | | | 10↑ | | | |
| $t_n$ | Hold Time | Select | | | | 5↑ | | | ns |
| | | Data (4) | | | | 5↑ | | | |

**Note 3:** For testing $f_{MAX}$ all outputs are loaded simultaneously.

**Note 4:** Data includes the two serial inputs and the eight input/output data lines.



# Dual 4-Line to 1-Line Data Selectors/Multiplexers

## General Description

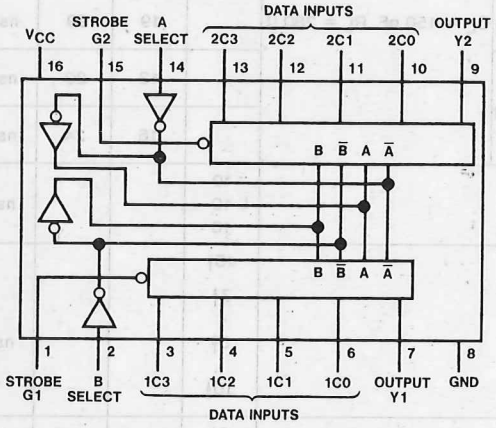
Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

## Features

- Inverting version of 54/74LS153
- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low-impedance, totem-pole outputs

| Typical Average Propagation Delay Times | | | Typical Power Dissipation |
|---|---|---|---|
| From Data | From Strobe | From Select | |
| 15 ns | 19 ns | 22 ns | 31 mW |

## Connection Diagram



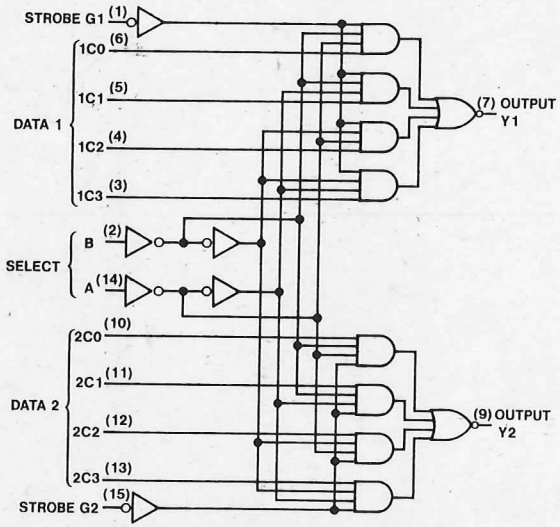

54LS352 (J,N,W) 74LS352 (J,N,W)

## Truth Table

| Select Inputs | | Data Inputs | | | | Strobe | Output |
|---|---|---|---|---|---|---|---|
| B | A | C0 | C1 | C2 | C3 | G | Y |
| X | X | X | X | X | X | H | H |
| L | L | L | X | X | X | L | H |
| L | L | H | X | X | X | L | L |
| L | H | X | L | X | X | L | H |
| L | H | X | H | X | X | L | L |
| H | L | X | X | L | X | L | H |
| H | L | X | X | H | X | L | L |
| H | H | X | X | X | L | L | H |
| H | H | X | X | X | H | L | L |

Select inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 LS352 Min | DM54/74 LS352 Typ (1) | DM54/74 LS352 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min | $I_I$ = −18 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | DM54 | 2.5 | 3.4 | | V |
| | | | | DM74 | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 4 | mA |
| | | | | DM74 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $I_{OL}$ = Max | DM54 | | 0.25 | 0.4 | V |
| | | | | DM74 | | 0.35 | 0.5 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 7 V | | | | 0.1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max | $V_I$ = 2.7 V | | | | 20 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.4 V | | | | −0.4 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | DM54 | −20 | | −100 | mA |
| | | | | DM74 | −20 | | −100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | DM54 | | 6.2 | 10 | mA |
| | | | | DM74 | | 6.2 | 10 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

**Note 3:** $I_{CCL}$ is measured with the outputs open and all inputs grounded.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Conditions | DM54/74 LS352 Min | DM54/74 LS352 Typ | DM54/74 LS352 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Y | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 13 | 20 | ns |
| | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 16 | 24 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 17 | 26 | |
| | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 23 | 35 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Select | Y | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 19 | 29 | ns |
| | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 22 | 33 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 25 | 38 | |
| | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 31 | 47 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Strobe | Y | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 16 | 24 | ns |
| | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 19 | 29 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 21 | 32 | |
| | | | | $C_L$ = 50 pF, $R_L$ = 2 kΩ | | 27 | 41 | |

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# TRI-STATE® Data Selectors/Multiplexers

## General Description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply full complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

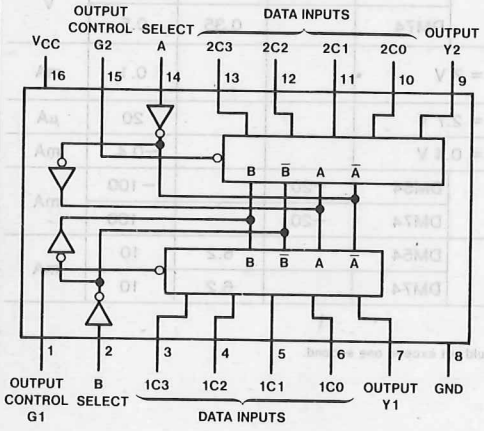
The TRI-STATE outputs can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level.

## Features

- Inverting version of 54/74LS253
- Schottky-diode-clamped transistors
- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe/output control
- High fan-out totem-pole outputs

| Typical Propagation Delay | | Typical Power Dissipation |
|---|---|---|
| Data to Output | 12 ns | 35 mW |
| Select to Output | 21 ns | |

## Connection Diagram



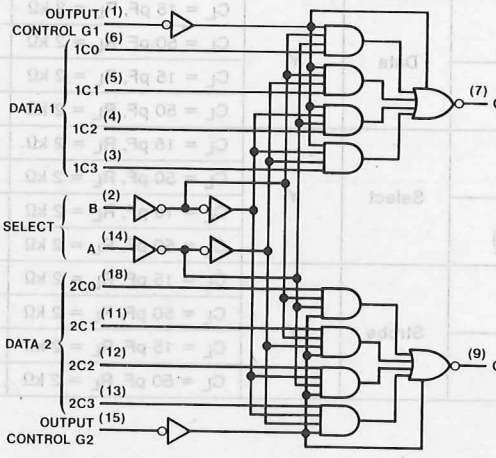

54LS353 (J,N,W) 74LS353 (J,N,W)

## Truth Table

| Select Inputs | | Data Inputs | | | | Output Control | Output |
|---|---|---|---|---|---|---|---|
| B | A | C0 | C1 | C2 | C3 | G | Y |
| X | X | X | X | X | X | H | Z |
| L | L | L | X | X | X | L | H |
| L | L | H | X | X | X | L | L |
| L | H | X | L | X | X | L | H |
| L | H | X | H | X | X | L | L |
| H | L | X | X | L | X | L | H |
| H | L | X | X | H | X | L | L |
| H | H | X | X | X | L | L | H |
| H | H | X | X | X | H | L | L |

Address inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 LS353 Min | DM54/74 LS353 Typ(1) | DM54/74 LS353 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | DM54 | | | −1 | mA |
| | | | | DM74 | | | −2.6 | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | DM54 | 2.4 | 3.4 | | V |
| | | | | DM74 | 2.4 | 3.1 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 12 | mA |
| | | | | DM74 | | | 24 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V | $I_{OL}$ = Max | DM54 | | | 0.4 | V |
| | | | | DM74 | | | 0.5 | |
| | | $V_{IL}$ = 0.8 V | $I_{OL}$ = 12 mA | DM74 | | | 0.4 | |
| $I_{O(OFF)}$ | Off-State (High-Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | | $V_O$ = 0.4 V | | | −20 | μA |
| | | | | $V_O$ = 2.7 V | | | 20 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | | 20 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | | −0.4 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | Condition A | | 7 | 12 | mA |
| | | | | Condition B | | 8.5 | 14 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

**Note 3:** $I_{CC}$ is measured with the outputs open under the following conditions:

A. All inputs grounded.

B. Output control at 4.5 V, all inputs grounded.

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## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Conditions | DM54/74 LS353 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Y | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 17 | 25 | ns |
| | | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 23 | 35 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 13 | 20 | |
| | | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 20 | 30 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Select | Y | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 30 | 45 | ns |
| | | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 36 | 54 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 21 | 32 | |
| | | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 29 | 44 | |
| $t_{ZH}$ | Output Enable Time To High Level | Output Control | Y | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 15 | 23 | ns |
| | | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 25 | 38 | |
| $t_{ZL}$ | Output Enable Time To Low Level | | | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 15 | 23 | |
| | | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 23 | 35 | |
| $t_{HZ}$ | Output Disable Time From High Level | Output Control | Y | $C_L$ = 5 pF, $R_L$ = 667 Ω | | 27 | 41 | ns |
| $t_{LZ}$ | Output Disable Time From Low Level | | | $C_L$ = 5 pF, $R_L$ = 667 Ω | | 18 | 27 | |

# TRI-STATE® Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

## General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

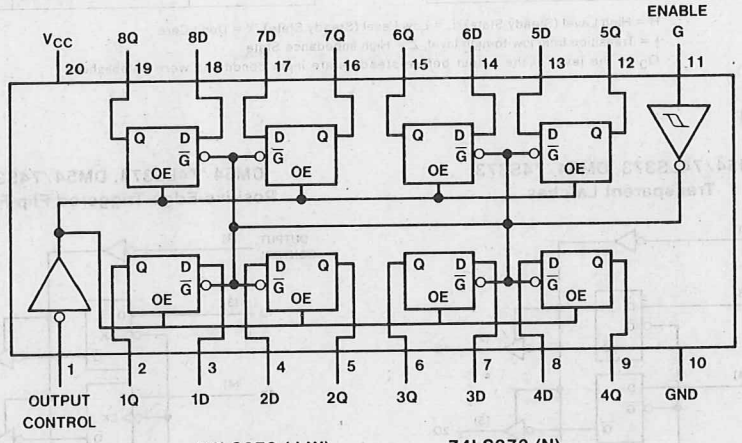
The eight latches of the DM54/74LS373 and DM54/74S373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

(Continued next page)

## Features

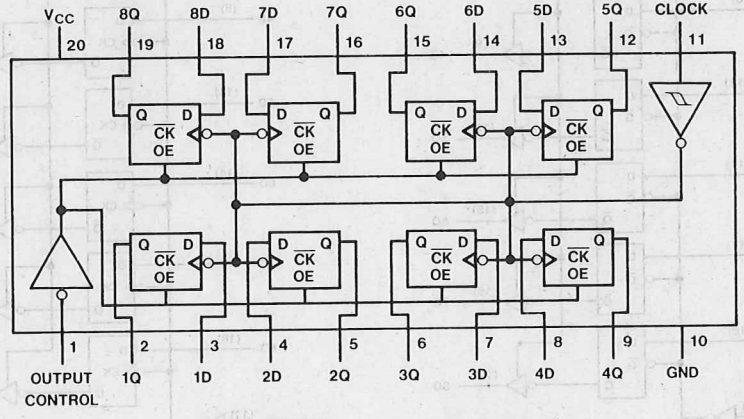
- Choice of 8 Latches or 8 D-Type Flip-Flops in a Single Package
- TRI-STATE Bus-Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Clock/Enable Input Has Hysteresis to Improve Noise Rejection
- P-N-P Inputs Reduce D-C Loading on Data Lines (DM54/74S373 and DM54/74S374)

## Connection Diagrams




54LS373 (J,W)
54S373 (J,W)

74LS373 (N)
74S373 (N)




54LS374 (J,W)
54S374 (J,W)

74LS374 (N)
74S374 (N)

## General Description (continued)

The eight flip-flops of the DM54/74LS374 and DM54/74S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

## Truth Tables

**DM54/74LS373, DM54/74S373**
**Truth Table**

| Output Control | Enable G | D | Output |
|---|---|---|---|
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

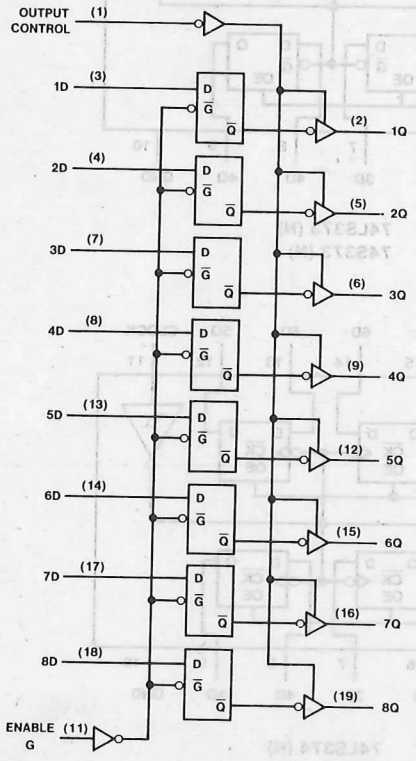
**DM54/74LS374, DM54/74S374**
**Truth Table**

| Output Control | Clock | D | Output |
|---|---|---|---|
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

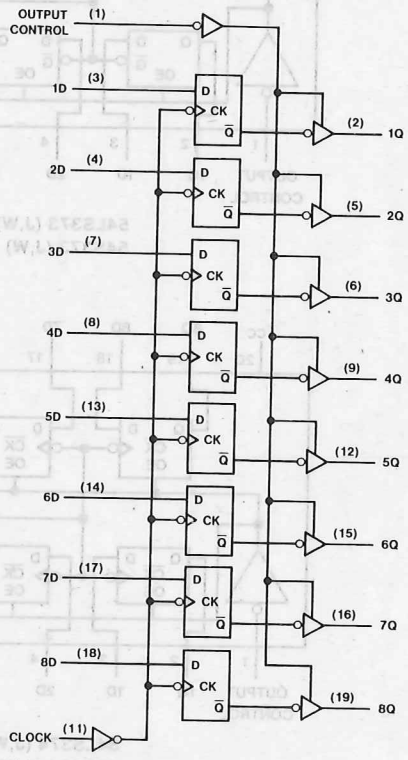
H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care
↑ = Transition from low-to-high level, Z = High Impedance State
$Q_0$ = The level of the output before steady-state input conditions were established.

## Logic Diagram

**DM54/74LS373, DM54/74S373**
**Transparent Latches**




**DM54/74LS374, DM54/74S374**
**Positive-Edge-Triggered Flip-Flops**



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | | DM54/74 LS373, LS374 | | | DM54/74 S373, S374 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High-Level Input Voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-Level Input Voltage | | | DM54 | | | 0.8 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | | −1.5 | | | −1.2 | V |
| $I_{OH}$ | High Level Output Current | | | DM54 | | | −1.0 | | | −2 | mA |
| | | | | DM74 | | | −2.6 | | | −6.5 | |
| $V_{OH}$ | High-Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | DM54 | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| | | | | DM74 | 2.4 | 3.1 | | 2.4 | 3.2 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 12 | | | 20 | mA |
| | | | | DM74 | | | 24 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $I_{OL}$ = Max | DM54 | | 0.25 | 0.4 | | | 0.5 | V |
| | | | | DM74 | | 0.35 | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 12 mA | DM74 | | | 0.4 | | | | |
| $I_{O(OFF)}$ | Off State (High Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $V_O$ = 0.4 V | | | | −20 | | | | μA |
| | | | $V_O$ = 0.5 V | | | | | | | −50 | |
| | | | $V_O$ = 2.7 V | | | | 20 | | | | |
| | | | $V_O$ = 2.4 V | | | | | | | 50 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max | $V_I$ = 7 V | | | | 0.1 | | | | mA |
| | | | $V_I$ = 5.5 V | | | | | | | 1 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | | 20 | | | 50 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.4 V | | | | −400 | | | | μA |
| | | | $V_I$ = 0.5 V | | | | | | | −250 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | | −20 | | −100 | −40 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | LS373 | | | 24 | 40 | | | | mA |
| | | | LS374 | | | 27 | 45 | | | | |
| | | | S373 | | | | | | 105 | 160 | |
| | | | S374 | | | | | | 90 | 140 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.
**Note 2:** Only one output should be shorted at a time and duration should not exced one second.

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## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Conditions | DM54/74 | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | LS373 | | | LS374 | | | |
| | | | | | Min | Typ | Max | Min | Typ | Max | |
| $f_{max}$ | Maximum Clock Frequency | | | $C_L$ = 45 pF, $R_L$ = 667 Ω | | | | 35 | 50 | | MHz |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | Data | Any Q | | | 12 | 18 | | | | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | 12 | 18 | | | | |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | Clock or Enable | Any Q | | | 20 | 30 | | 15 | 28 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | 18 | 30 | | 19 | 28 | |
| $t_{PZH}$ | Output Enable Time to High Level | Output Control | Any Q | | | 15 | 28 | | 20 | 28 | ns |
| $t_{PZL}$ | Output Enable Time to Low Level | | | | | 25 | 36 | | 21 | 28 | |
| $t_{PHZ}$ | Output Disable Time from High Level | Output Control | Any Q | $C_L$ = 5 pF, $R_L$ = 667 Ω | | 12 | 20 | | 12 | 20 | ns |
| $t_{PLZ}$ | Output Disable Time from Low Level | | | | | 15 | 25 | | 14 | 25 | |
| $t_w$ | Clock/Enable Pulse Width | | | High | 15 | | | 15 | | | ns |
| | | | | Low | 15 | | | 15 | | | |
| $t_{su}$ | Data Setup Time | | | | 0↓ | | | 20↑ | | | ns |
| $t_h$ | Data Hold Time | | | | 10↓ | | | 0↑ | | | ns |
| $f_{max}$ | Maximum Clock Frequency | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | | | | 20 | 40 | | MHz |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | Data | Any Q | | | 17 | 26 | | | | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | 18 | 27 | | | | |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | Clock or Enable | Any Q | | | 25 | 38 | | 21 | 32 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | 24 | 36 | | 25 | 38 | |
| $t_{PZH}$ | Output Enable Time to High Level | Output Control | Any Q | | | 24 | 36 | | 29 | 44 | ns |
| $t_{PZL}$ | Output Enable Time to Low Level | | | | | 33 | 50 | | 29 | 44 | |
| $t_w$ | Clock/Enable Pulse Width | | | High | 15 | | | 15 | | | ns |
| | | | | Low | 15 | | | 15 | | | |
| $t_{su}$ | Data Setup Time | | | | 0↓ | | | 20↑ | | | ns |
| $t_h$ | Data Hold Time | | | | 10↓ | | | 0↑ | | | ns |

**Note:** ↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge ↓ for the falling edge.

## Switching Characteristics (Continued)

| Parameter | | From (Input) | To (Output) | Conditions | DM54/74 | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | S373 | | | S374 | | | |
| | | | | | Min | Typ | Max | Min | Typ | Max | |
| $f_{max}$ | Maximum Clock Frequency | | | $C_L$ = 15 pF, $R_L$ = 280 Ω | | | | 75 | 100 | | MHz |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | Data | Any Q | | | 5 | 9 | | | | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | 9 | 13 | | | | |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | Clock or Enable | Any Q | | | 7 | 14 | | 8 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | 12 | 18 | | 11 | 17 | |
| $t_{PZH}$ | Output Enable Time to High Level | Output Control | Any Q | | | 8 | 15 | | 8 | 15 | ns |
| $t_{PZL}$ | Output Enable Time to Low Level | | | | | 11 | 18 | | 11 | 18 | |
| $t_{PHZ}$ | Output Disable Time from High Level | Output Control | Any Q | $C_L$ = 5 pF, $R_L$ = 280 Ω | | 6 | 9 | | 5 | 9 | ns |
| $t_{PLZ}$ | Output Disable Time from Low Level | | | | | 8 | 12 | | 7 | 12 | |
| $t_w$ | Clock/Enable Pulse Width | | | High | 6 | | | 6 | | | ns |
| | | | | Low | 7.3 | | | 7.3 | | | |
| $t_{su}$ | Data Setup Time | | | | 0↓ | | | 5↑ | | | ns |
| $t_h$ | Data Hold Time | | | | 10↓ | | | 2↑ | | | ns |
| $f_{max}$ | Maximum Clock Frequency | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | | | 75 | 100 | | MHz |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | Data | Any Q | | | 7 | 11 | | | | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | 11 | 17 | | | | |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | Clock or Enable | Any Q | | | 9 | 14 | | 10 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | 14 | 21 | | 13 | 20 | |
| $t_{PZH}$ | Output Enable Time to High Level | Output Control | Any Q | | | 11 | 17 | | 11 | 17 | ns |
| $t_{PZL}$ | Output Enable Time to Low Level | | | | | 15 | 23 | | 15 | 23 | |
| $t_w$ | Clock/Enable Pulse Width | | | High | 15 | | | 15 | | | ns |
| | | | | Low | 15 | | | 15 | | | |
| $t_{su}$ | Data Setup Time | | | | 0↓ | | | 5↑ | | | ns |
| $t_h$ | Data Hold Time | | | | 10↓ | | | 2↑ | | | ns |

**Note:** ↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge ↓ for the falling edge.

6

# Arithmetic Logic Unit/Function Generator

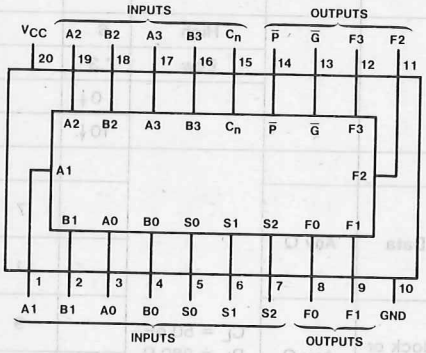
## General Description

The 'S381 is a Schottky TTL arithmetic logic unit (ALU)/function generator that performs eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. These operations are selected by the three function-select lines (S0, S1, S2). A full carry look-ahead circuit is provided for fast, simultaneous carry generation by means of two cascade outputs ($\overline{P}$ and $\overline{G}$) for the four bits in the package. The method of cascading 54S182/74S182 look-ahead carry generators with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the 'S182. The typical addition times shown illustrate the short delay time required for addition of longer words when full look-ahead is employed. The exclusive-OR, AND, or OR function of two Boolean variables is provided without the use of external circuitry. Also, the outputs can be either cleared (low) or preset (high) as desired.

## Features

- A Fully Parallel 4-Bit ALU in 20-Pin Package for 0.300-Inch Row Spacing
- Ideally Suited for High-Density Economical Processors
- Parallel Inputs and Outputs and Full Look-Ahead Provide System Flexibility
- Arithmetic and Logic Operations Selected Specifically to Simplify System Implementation:
  - A Minus B
  - B Minus A
  - A Plus B
  - and Five Other Functions
- Schottky-Clamped for High Performance
  - 16-Bit Add Time . . . 26 ns Typ Using Look-Ahead
  - 32-Bit Add Time . . . 34 ns Typ Using Look-Ahead

## Connection Diagram




54S381 (J) 74S381 (N)

## Pin Designations

| Designation | Pin Nos. | Function |
|---|---|---|
| A3, A2, A1, A0 | 17, 19, 1, 3 | WORD A INPUTS |
| B3, B2, B1, B0 | 16, 18, 2, 4 | WORD B INPUTS |
| S2, S1, S0 | 7, 6, 5 | FUNCTION-SELECT INPUTS |
| $C_n$ | 15 | CARRY INPUT FOR ADDITION, INVERTED CARRY INPUT FOR SUBTRACTION |
| F3, F2, F1, F0 | 12, 11, 9, 8 | FUNCTION OUTPUTS |
| $\overline{P}$ | 14 | INVERTED CARRY PROPAGATE OUTPUT |
| $\overline{G}$ | 13 | INVERTED CARRY GENERATE OUTPUT |
| $V_{CC}$ | 20 | SUPPLY VOLTAGE |
| GND | 10 | GROUND |

## Truth Table

| Selection | | | Arithmetic/Logic Operation |
|---|---|---|---|
| S2 | S1 | S0 | |
| L | L | L | CLEAR |
| L | L | H | B MINUS A |
| L | H | L | A MINUS B |
| L | H | H | A PLUS B |
| H | L | L | A ⊕ B |
| H | L | H | A + B |
| H | H | L | AB |
| H | H | H | PRESET |

H = high level, L = low level

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | DM54/74 S381 Min | DM54/74 S381 Typ (1) | DM54/74 S381 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | DM54 | | | 0.8 | V |
| | | | | DM74 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | −1.2 | V |
| $I_{OH}$ | High Level Output Current | | | DM54 | | | −1.0 | mA |
| | | | | DM74 | | | −1.0 | |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −1 mA | DM54 | 2.4 | 3.4 | | V |
| | | | | DM74 | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | DM54 | | | 20 | mA |
| | | | | DM74 | | | 20 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 20 mA | | | | 0.5 | V |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | Any S Input | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | 50 | μA |
| | | Cn | | | | | 250 | |
| | | Any Other | | | | | 200 | |
| $I_{IL}$ | Low Level Input Current | Any S Input | $V_{CC}$ = Max, $V_I$ = 0.5 V | | | | −2 | mA |
| | | Cn | | | | | −8 | |
| | | Any Other | | | | | −6 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | −40 | | −100 | mA |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max | | | 105 | 160 | mA |

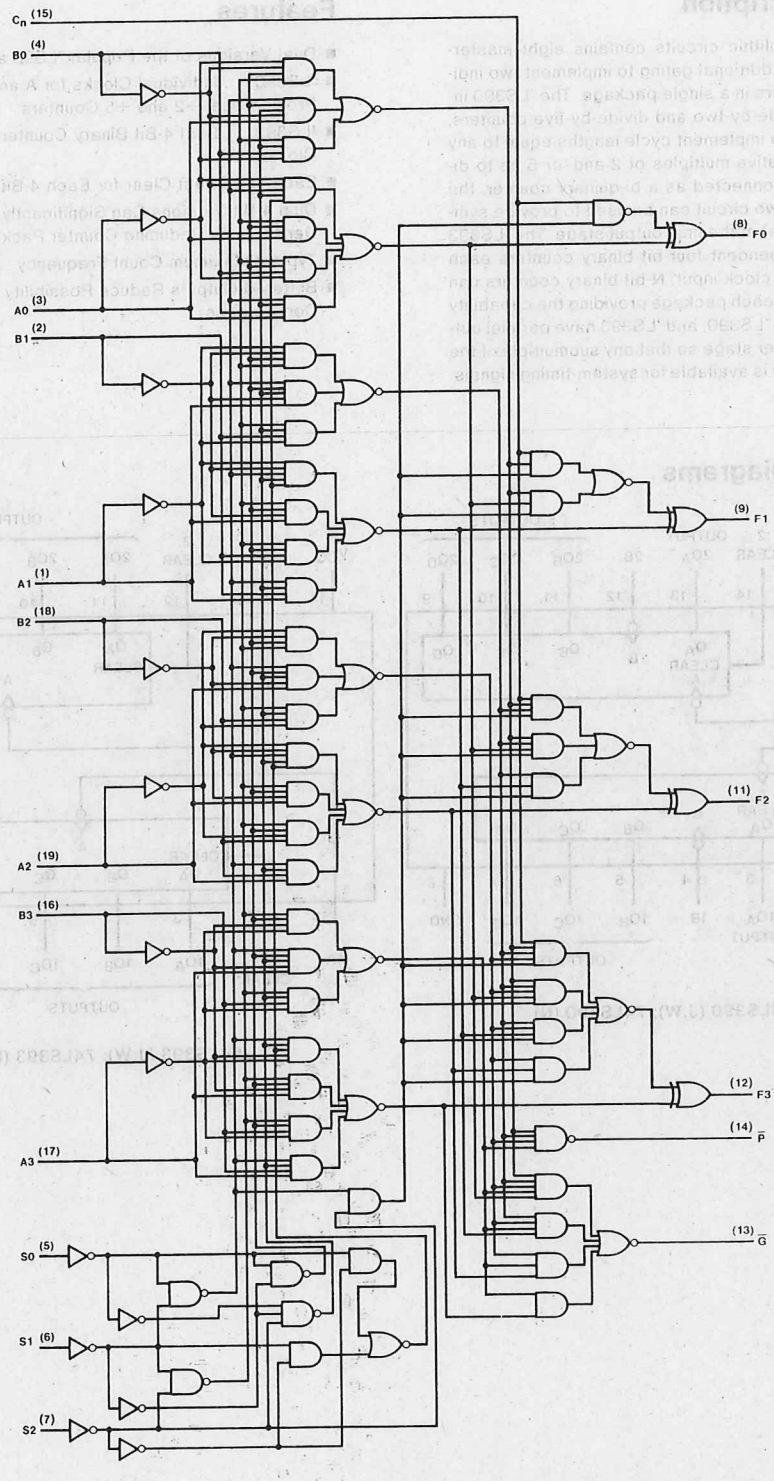
**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Only one output should be shorted at a time, duration not to exceed one second.

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## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Conditions | DM54/DM74 S381 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Cn | Any F | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 10 | 17 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 12 | 19 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 10 | 17 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 12 | 19 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any A or B | $\overline{G}$ | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 12 | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 14 | 23 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 12 | 20 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 14 | 23 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any A or B | $\overline{P}$ | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 11 | 18 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 13 | 21 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 11 | 18 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 13 | 21 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $A_i$ or $B_i$ | $F_i$ | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 18 | 27 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 20 | 30 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 16 | 25 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 18 | 27 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any S | Any | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 18 | 30 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 20 | 33 | |
| | | | | $C_L$ = 15 pF, $R_L$ = 280 Ω | | 18 | 30 | |
| | | | | $C_L$ = 50 pF, $R_L$ = 280 Ω | | 20 | 33 | |

## Logic Diagram



# Dual 4-Bit Decade and Binary Counters

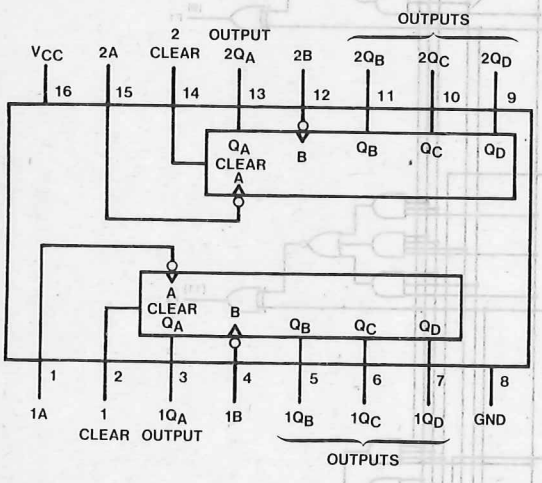
## General Description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The 'LS390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The 'LS393 comprises two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The 'LS390, and 'LS393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

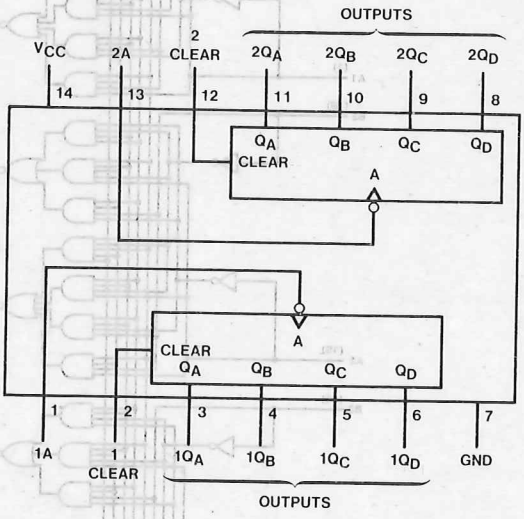
## Features

- Dual Versions of the Popular 'LS90 and 'LS93
- 'LS390 . . . Individual Clocks for A and B Flip-Flops Provide Dual ÷2 and ÷5 Counters
- 'LS393 . . . Dual 4-Bit Binary Counter with Individual Clocks
- Each has Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency . . . 35 MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

## Connection Diagrams




54LS390 (J,W); 74LS390 (N)




54LS393 (J,W); 74LS393 (N)

## Truth Tables

'LS390
BCD COUNT SEQUENCE
(EACH COUNTER)
(See Note A)

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

'LS390
BI-QUINARY (5-2)
(EACH COUNTER)
(See Note B)

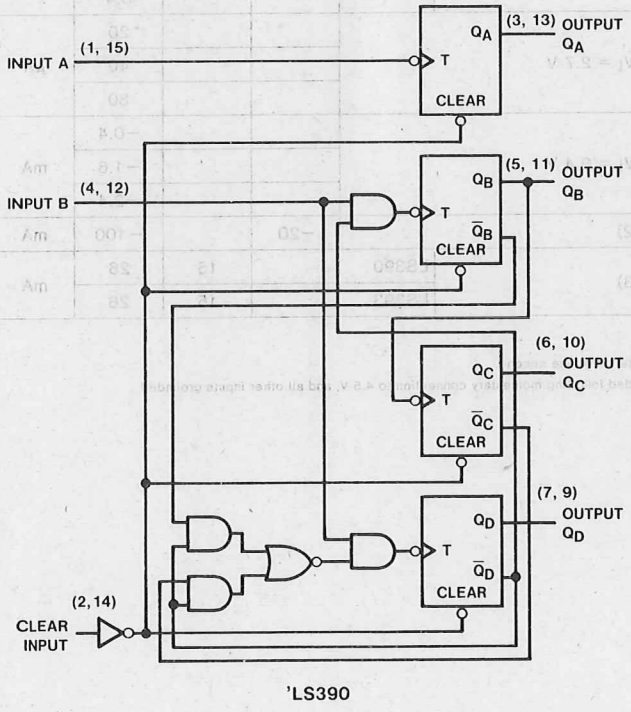
| Count | Output | | | |
|---|---|---|---|---|
| | $Q_A$ | $Q_D$ | $Q_C$ | $Q_B$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

'LS393
COUNT SEQUENCE
(EACH COUNTER)

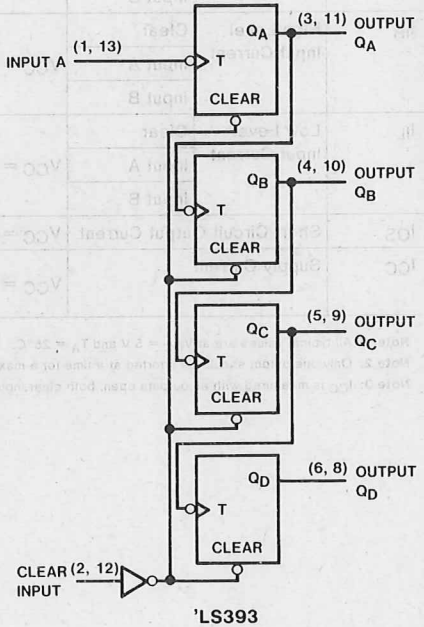
| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

A. Output $Q_A$ is connected to Input B for BCD count.
B. Output $Q_D$ is connected to Input A for Bi-quinary count.
C. H = high level, L = low level.

## Logic Diagrams




'LS390




'LS393

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM54/74 LS390, LS393 Min | Typ (1) | Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | DM54 | | | 0.8 | V |
| | | | | | DM74 | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | DM54 | | | −400 | µA |
| | | | | | DM74 | | | −400 | |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | DM54 | 2.5 | 3.4 | | V |
| | | | | | DM74 | 2.7 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | | | DM54 | | | 4 | mA |
| | | | | | DM74 | | | 8 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $I_{OL}$ = Max | DM54 | | 0.25 | 0.4 | V |
| | | | | | DM74 | | 0.35 | 0.5 | |
| | | | | $I_{OL}$ = 4 mA | DM74 | | 0.25 | 0.4 | |
| $I_I$ | Input Current at Maximum Input Voltage | Clear | $V_{CC}$ = Max | | $V_I$ = 7 V | | | 0.1 | mA |
| | | Input A | | | $V_I$ = 5.5 V | | | 0.2 | |
| | | Input B | | | | | | 0.4 | |
| $I_{IH}$ | High Level Input Current | Clear | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | | 20 | µA |
| | | Input A | | | | | | 40 | |
| | | Input B | | | | | | 80 | |
| $I_{IL}$ | Low Level Input Current | Clear | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | | −0.4 | mA |
| | | Input A | | | | | | −1.6 | |
| | | Input B | | | | | | −2.4 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (3) | | LS390 | | 15 | 26 | mA |
| | | | | | LS393 | | 15 | 26 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.

**Note 2:** Only one output should be shorted at a time for a maximum duration of one second.

**Note 3:** $I_{CC}$ is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | To (Output) | Conditions | DM54/74 | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | LS390 | | | LS393 | | | |
| | | | | | | Min | Typ | Max | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | A | $Q_A$ | $C_L$ = 15 pF, $R_L$ = 2 kΩ | 25 | 35 | | 25 | 35 | | MHz |
| | | | B | $Q_B$ | | 20 | 30 | | | | | |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | | A | $Q_A$ | | | 12 | 20 | | 12 | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | | 13 | 20 | | 13 | 20 | |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | | A | $Q_C$ of LS390 / $Q_D$ of LS393 | | | 37 | 60 | | 40 | 60 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | | 39 | 60 | | 40 | 60 | |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | | B | $Q_B$ | | | 13 | 21 | | | | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | | 14 | 21 | | | | |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | | B | $Q_C$ | | | 24 | 39 | | | | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | | 26 | 39 | | | | |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | | B | $Q_D$ | | | 13 | 21 | | | | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | | 14 | 21 | | | | |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | Clear | Any | | | 24 | 39 | | 24 | 39 | ns |
| $t_W$ | Pulse Width | A Input High or Low | | | | 20 | | | 20 | | | ns |
| | | B Input High or Low | | | | 25 | | | 25 | | | |
| | | Clear High | | | | 20 | | | 20 | | | |
| $t_{SU}$ | Clear Inactive State Setup Time | | | | | 25↓ | | | 25↓ | | | ns |

## Switching Characteristics (Continued)

| Parameter | | | From (Input) | To (Output) | Conditions | DM54/74 | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | LS390 | | | LS393 | | | |
| | | | | | | Min | Typ | Max | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | A | $Q_A$ | $C_L$ = 50 pF, $R_L$ = 2 kΩ | 20 | 30 | | 20 | 30 | | MHz |
| | | | B | $Q_B$ | | 15 | 20 | | | | | |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | | A | $Q_A$ | | | 16 | 24 | | 16 | 24 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | | 20 | 30 | | 20 | 30 | |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | | A | $Q_C$ of LS390 | | | 54 | 81 | | 58 | 87 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | $Q_D$ of LS393 | | | 54 | 81 | | 58 | 87 | |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | | B | $Q_B$ | | | 18 | 27 | | | | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | | 22 | 33 | | | | |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | | B | $Q_C$ | | | 34 | 51 | | | | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | | 36 | 54 | | | | |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level Output | | B | $Q_D$ | | | 18 | 27 | | | | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | | 22 | 33 | | | | |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | Clear | Any | | | 30 | 45 | | 30 | 45 | ns |
| $t_W$ | Pulse Width | A Input High or Low | | | | 20 | | | 20 | | | ns |
| | | B Input High or Low | | | | 25 | | | 25 | | | |
| | | Clear High | | | | 20 | | | 20 | | | |
| $t_{SU}$ | Clear Inactive State Setup Time | | | | | 25↓ | | | 25↓ | | | ns |

# TRI-STATE® 4 by 4 Register Files

## General Description

These register files are organized as 4 words of 4 bits each, and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits writing into one location, and reading from another word location, simultaneously.

Four data inputs are available to supply the word to be stored. Location of the word is determined by the write select inputs A and B, in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, $G_W$, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, $G_R$, is high, the data outputs are inhibited and go into the high impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

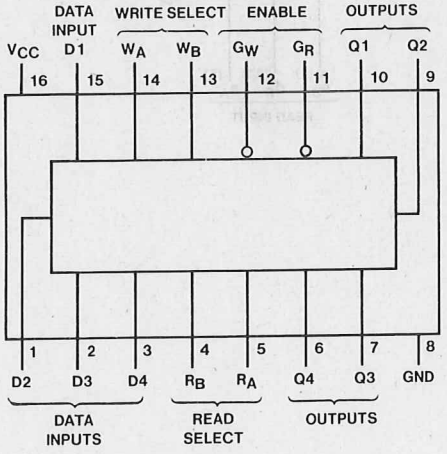
This arrangement—data entry addressing separate from data read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 ns typical) and the read time (24 ns typical). The register file has a non-volatile readout in that data is not lost when addressed.

All inputs (except read enable and write enable) are buffered to lower the drive requirements to one normal Series 54LS/74LS load, and input clamping diodes minimize switching transients to simplify system design. High speed, double ended AND-OR-INVERT gates are employed for the read-address function and have high sink current, TRI-STATE outputs. Up to 128 of these outputs may be wire-AND connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide n-bit word length.

## Features

- For use as:
  - Scratch pad memory
  - Buffer storage between processors
  - Bit storage in fast multiplication designs
- Separate read/write addressing permits simultaneous reading and writing
- Organized as 4 words of 4 bits
- Expandable to 512 words of n-bits
- TRI-STATE versions of DM54LS170/DM74LS170
- Fast access times 20 ns type

## Connection Diagram




54LS670/74LS670 (J,N,W)

## Truth Tables

WRITE TABLE (SEE NOTES A, B, AND C)

| Write Inputs | | | Word | | | |
|---|---|---|---|---|---|---|
| $W_B$ | $W_A$ | $G_W$ | 0 | 1 | 2 | 3 |
| L | L | L | Q = D | $Q_0$ | $Q_0$ | $Q_0$ |
| L | H | L | $Q_0$ | Q = D | $Q_0$ | $Q_0$ |
| H | L | L | $Q_0$ | $Q_0$ | Q = D | $Q_0$ |
| H | H | L | $Q_0$ | $Q_0$ | $Q_0$ | Q = D |
| X | X | H | $Q_0$ | $Q_0$ | $Q_0$ | $Q_0$ |

READ TABLE (SEE NOTES A AND D)

| Read Inputs | | | Outputs | | | |
|---|---|---|---|---|---|---|
| $R_B$ | $R_A$ | $G_R$ | Q1 | Q2 | Q3 | Q4 |
| L | L | L | W0B1 | W0B2 | W0B3 | W0B4 |
| L | H | L | W1B1 | W1B2 | W1B3 | W1B4 |
| H | L | L | W2B1 | W2B2 | W2B3 | W2B4 |
| H | H | L | W3B1 | W3B2 | W3B3 | W3B4 |
| X | X | H | Z | Z | Z | Z |

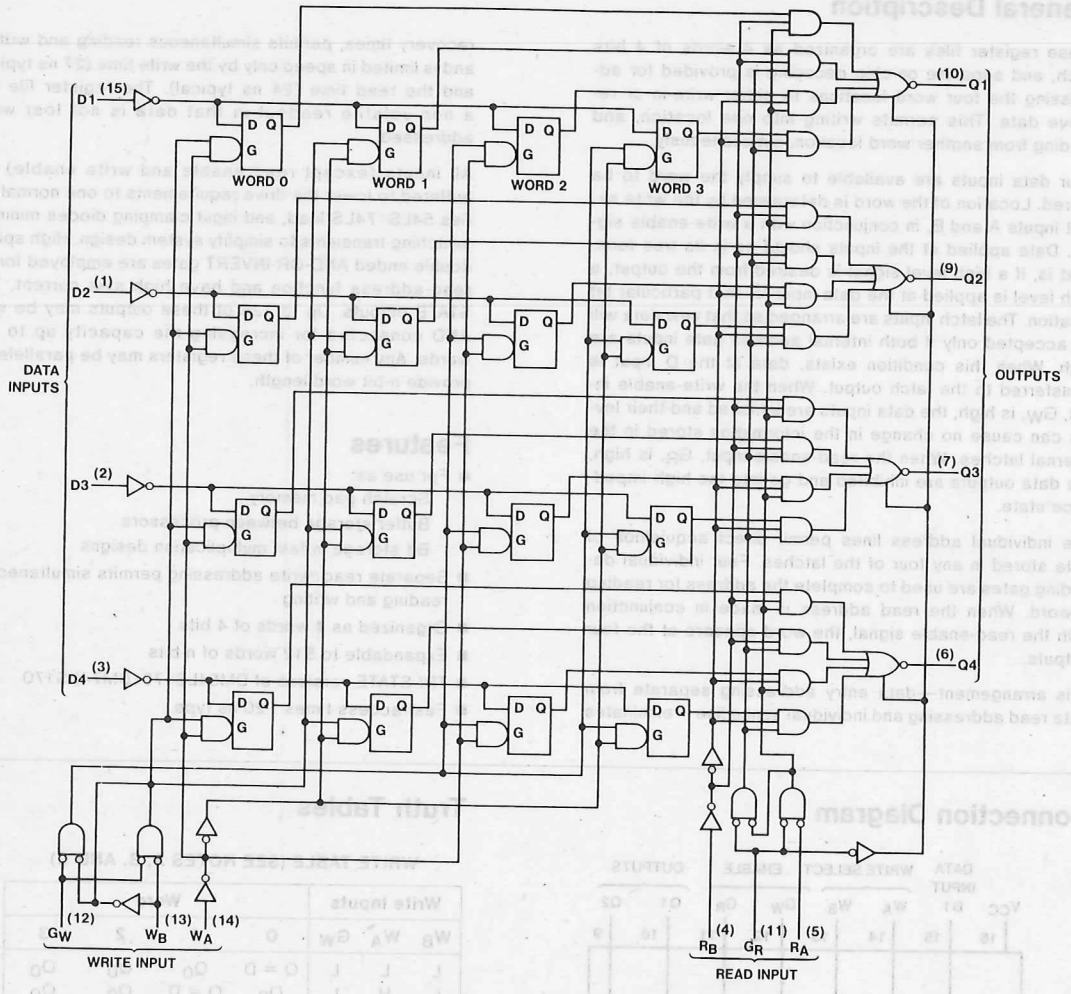
**Note A:** H = High Level, L = Low Level, X = Don't Care, Z = High Impedance (Off)

**Note B:** (Q = D) = The four selected internal flip-flop outputs will assume the states appled to the four external data inputs.

**Note C:** $Q_0$ = The level of Q before the indicated input conditions were established.

**Note D:** W0B1 = The first bit of word 0, etc.

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM54/74 LS670 | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | DM54 | | | −1 | mA |
| | | | DM74 | | | −2.6 | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | DM54 | 2.4 | 3.4 | | V |
| | | | DM74 | 2.4 | 3.4 | | |
| $I_{OL}$ | Low Level Output Current | | DM54 | | | 12 | mA |
| | | | DM74 | | | 24 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = Max | DM54 | | 0.25 | 0.4 | V |
| | | | DM74 | | 0.35 | 0.5 | |
| $I_{O(OFF)}$ | Off-State (High Impedance State)Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $V_O$ = 0.4 V | | | −20 | μA |
| | | | $V_O$ = 2.7 V | | | 20 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 7 V | Any D, R, or W | | | 0.1 | mA |
| | | | $G_W$ | | | 0.2 | |
| | | | $G_R$ | | | 0.3 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7 V | Any D, R, or W | | | 20 | μA |
| | | | $G_W$ | | | 40 | |
| | | | $G_R$ | | | 60 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | Any D, R, or W | | | −0.4 | mA |
| | | | $G_W$ | | | −0.8 | |
| | | | $G_R$ | | | −1.2 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | | 30 | 50 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

**Note 3:** Maximum $I_{CC}$ is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

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## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | To (Output) | Conditions | DM54/74 LS670 Min | DM54/74 LS670 Typ | DM54/74 LS670 Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Read Select | Any Q | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 23 | 40 | ns |
| | | | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 28 | 50 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 25 | 45 | |
| | | | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 31 | 55 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Write Enable | Any Q | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 26 | 45 | ns |
| | | | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 31 | 55 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 28 | 50 | |
| | | | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 34 | 60 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Data | Any Q | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 25 | 45 | ns |
| | | | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 30 | 55 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 23 | 40 | |
| | | | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 29 | 50 | |
| $t_{ZH}$ | Output Enable Time to High Level | | Read Enable | Any Q | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 15 | 35 | ns |
| | | | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 25 | 45 | |
| $t_{ZL}$ | Output Enable Time to Low Level | | | | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 22 | 40 | |
| | | | | | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 30 | 50 | |
| $t_{HZ}$ | Output Disable Time From High Level | | Read Enable | Any Q | $C_L$ = 5 pF, $R_L$ = 667 Ω | | 30 | 50 | ns |
| $t_{LZ}$ | Output Disable Time From Low Level | | | | $C_L$ = 5 pF, $R_L$ = 667 Ω | | 16 | 35 | |
| $t_W$ | Width of Write-Enable or Read-Enable Pulse | | | | | 25 | | | ns |
| $t_{SETUP}$ | Setup Times, High or Low Level Data (4) | Data Input With Respect to Write-Enable, $t_{SETUP(D)}$ | | | | 10 | | | ns |
| | | Write-Select With Respect to Write-Enable, $t_{SETUP(W)}$ | | | | 15 | | | |
| $t_{HOLD}$ | Hold Times, High or Low Level Data (4) | Data Input With Respect to Write-Enable, $t_{HOLD(D)}$ | | | | 15 | | | ns |
| | | Write-Select With Respect to Write-Enable, $t_{HOLD(W)}$ | | | | 5 | | | |
| $t_{LATCH}$ | Latch Time for New Data (5) | | | | | 25 | | | ns |

**Note 4:** Write-select time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{SETUP(W)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{HOLD(W)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

**Note 5:** Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.

# Dual Rank 8-Bit TRI-STATE® Shift Registers

## General Description

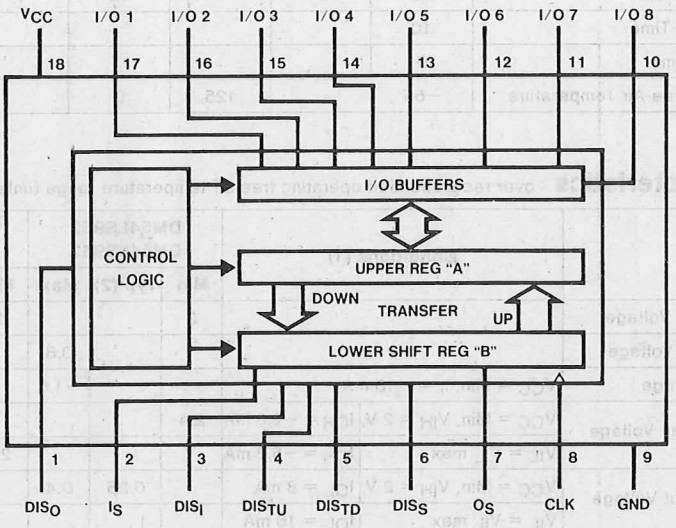
These circuits are TRI-STATE, edge-triggered, 8-bit I/O registers in parallel with 8-bit serial shift registers which are capable of operating in any of the following modes: parallel load from I/O pins to register "A", parallel transfer down from register "A" to serial shift register "B", parallel transfer up from shift register "B" to register "A", serial shift of register "B", synchronously clear (LS952 only) or exchange data between register "A" and shift register "B" (LS962 only). Since the registers are edge-triggered by the positive transition of the clock, the control lines which determine the mode or operation are completely independent of the logic level applied to the clock. Designed for bus-oriented systems, these circuits have their TRI-STATE inputs and outputs on the same pins.

## Features

- Registers are edge-triggered by the positive transition of the clock
- All inputs are PNP transistors
- Input disable dominates over output disable
- Output high impedance state does not impede any other mode of operation
- 8-bit I/O pins are TRI-STATE buffers
- Typical shift frequency is 36 MHz
- Typical power dissipation is 305 mW
- All control inputs are active when in an "L" logic state
- Devices can be cascaded into N-bit word

## Connection Diagram

**Dual-In-Line Package**




**Top View**

**Pin Description**

$DIS_O$—Output disable
$I_S$—Serial input
$DIS_I$—Input disable
$DIS_{TU}$—Transfer up disable
$DIS_{TD}$—Transfer down disable
$DIS_S$—Shift disable
$O_S$—Serial output
CLK—Clock
GND—Ground
I/O 1 . . . I/O 8—8-bit I/O pins
$V_{CC}$—Supply Voltage

## Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|---|
| Supply Voltage, $V_{CC}$ (Note 1) | 7 V |
| Input Voltage | 7 V |
| Operating Free-Air Temperature Range | |
| DM54LS952, DM54LS962 | −55°C to +125°C |
| DM74LS952, DM74LS962 | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) | 300°C |

**Note 1:** Voltage values are with respect to network ground terminal.

## Recommended Operating Conditions

| Parameter | | DM54LS952 DM54LS962 | | | DM74LS952 DM74LS962 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $V_{CC}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $I_{OH}$ | High-Level Output Current | | | −2.6 | | | −5.2 | mA |
| $I_{OL}$ | Low-Level Output Current | | | 8 | | | 16 | mA |
| $f_{CLOCK}$ | Clock Frequency | 0 | | 25 | 0 | | 25 | MHz |
| Clock Pulse | High Pulse Width | 25 | 17 | | 25 | 17 | | ns |
| | Low Pulse Width | 15 | 7 | | 15 | 7 | | ns |
| $t_{SET-UP}$ | Data Set-Up Time | 10 | | | | | | ns |
| $t_{HOLD}$ | Data Hold Time | 0 | | | | | | ns |
| $T_A$ | Operating Free-Air Temperature | −55 | | 125 | 0 | | 70 | °C |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions (1) | | DM54LS952 DM54LS962 | | | DM74LS952 DM74LS962 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (2) | Max | Min | Typ (2) | Max | |
| $V_{IH}$ | High-Level Input Voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-Level Input Voltage | | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | High-Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, | $I_{OH}$ = −2.6 mA | 2.4 | | | | | | V |
| | | $V_{IL}$ = $V_{IL}$ max | $I_{OH}$ = −5.2 mA | | | | 2.4 | | | |
| $V_{OL}$ | Low-Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, | $I_{OL}$ = 8 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | $V_{IL}$ = $V_{IL}$ max | $I_{OL}$ = 16 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | High-Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| $I_{IL}$ | Low-Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −50 | | | −50 | μA |
| $I_{OS}$ | Short-Circuit Output Current | $V_{CC}$ = Max (3) | | −20 | | −100 | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (4) | | | 61 | 99 | | 61 | 99 | mA |
| $I_{OFF}$ | TRI-STATE I/O Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V | $V_O$ = 2.4 V | | | 20 | | | 20 | μA |
| | | | $V_O$ = 0.4 V | | | −20 | | | −20 | μA |

**Note 1:** For conditions shown as min or max, use the appropriate value specified under recommended operating conditions.

**Note 2:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

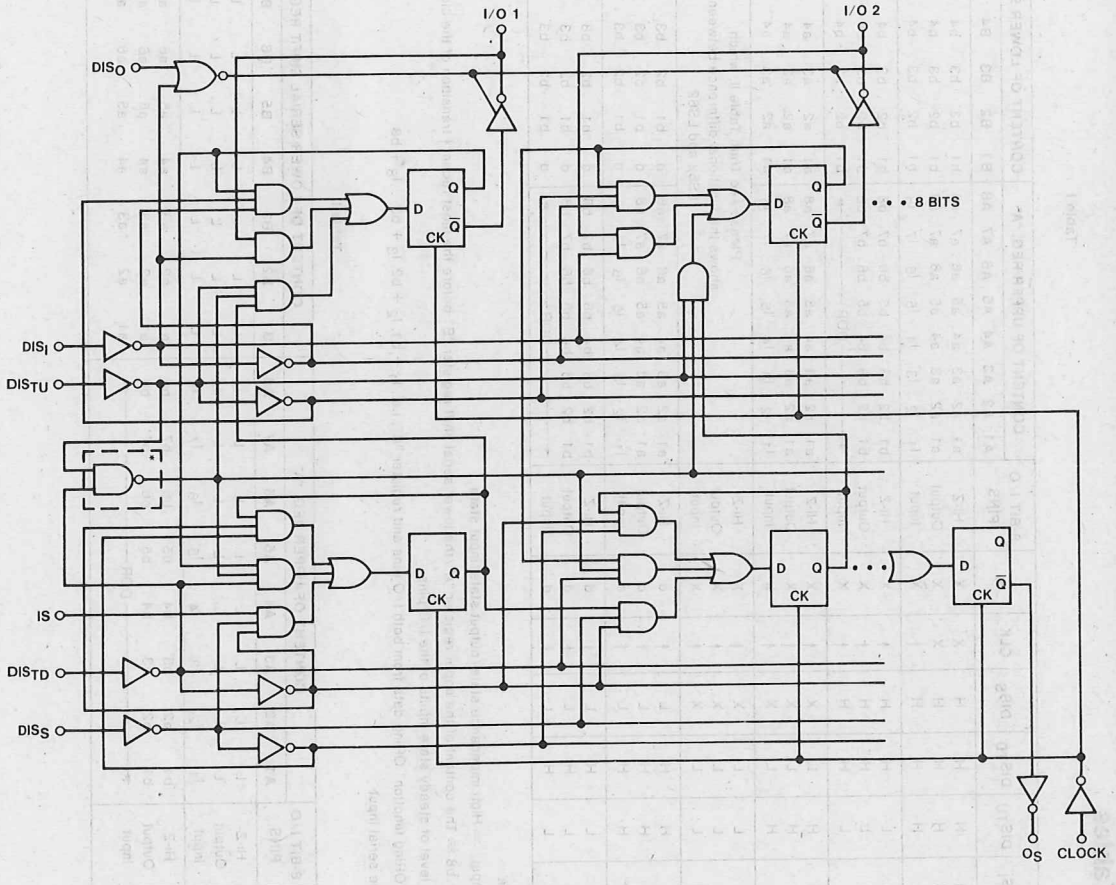
**Note 3:** Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

**Note 4:** $I_{CC}$ is measured with serial output open, the clock and shift disable input at 2.4 V. All other control inputs and I/O pins grounded.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | $C_L$ = 15 pF, $R_L$ = 1 kΩ | 25 | 36 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High-Level from Clock to Any Outputs | | 7 | 22 | 33 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level from Clock to Any Outputs | | 10 | 32 | 48 | ns |
| $t_{ENABLE}$ | Enable Time from Any Control Inputs | | 5 | 16 | 24 | ns |
| $t_{DISABLE}$ | Disable Time from Any Control Inputs | | 6 | 18 | 27 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | | 5 | 15 | 23 | ns |
| $t_{ZL}$ | Output Enable to Low Level | | 4 | 12 | 18 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | $C_L$ = 5 pF, $R_L$ = 1 kΩ | 5 | 15 | 23 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | 6 | 18 | 27 | ns |

## Logic Diagram




*Delete this NAND gate for the logic of LS962

# Truth Tables

**Table I**

| $DIS_O$ | $DIS_I$ | $DIS_{TU}$ | $DIS_{TD}$ | $DIS_S$ | CLK | $I_S$ | 8-BIT I/O PINS | CONTENT OF UPPER REG. "A" A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | CONTENT OF LOWER SERIAL SHIFT REG. "B" B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 | $O_S$ | COMMENTS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H | H | H | H | H | X | X | Hi-Z | a1 | a2 | a3 | a4 | a5 | a6 | a7 | a8 | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b8 | b8 | |
| L | H | H | H | H | X | X | Output | a1 | a2 | a3 | a4 | a5 | a6 | a7 | a8 | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b8 | b8 | Stable state |
| X | L | H | H | H | ↑ | X | Input | $I_1$ | $I_2$ | $I_3$ | $I_4$ | $I_5$ | $I_6$ | $I_7$ | $I_8$ | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b8 | b8 | Entering data from I/O to reg. "A" |
| H | H | L | H | H | ↑ | X | Hi-Z | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b8 | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b8 | b8 | |
| L | H | L | H | H | ↑ | X | Output | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b8 | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b8 | b8 | Transfer data up from reg. "B" to reg. "A" |
| X | L | L | H | H | ↑ | X | Input | ← DOR → | | | | | | | | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b8 | b8 | Reg. "A" will OR data from I/O and reg. "B" |
| H | H | H | L | X | ↑ | X | Hi-Z | a1 | a2 | a3 | a4 | a5 | a6 | a7 | a8 | a1 | a2 | a3 | a4 | a5 | a6 | a7 | a8 | a8 | |
| L | H | H | L | X | ↑ | X | Output | a1 | a2 | a3 | a4 | a5 | a6 | a7 | a8 | a1 | a2 | a3 | a4 | a5 | a6 | a7 | a8 | a8 | Transfer data down from reg. "A" to reg. "B" |
| X | L | H | L | X | ↑ | X | Input | $I_1$ | $I_2$ | $I_3$ | $I_4$ | $I_5$ | $I_6$ | $I_7$ | $I_8$ | a1 | a2 | a3 | a4 | a5 | a6 | a7 | a8 | a8 | Entering data and transfer down |
| H | H | L | L | X | ↑ | X | Hi-Z | Please see Truth Table II, which shows the functional difference between LS52 and LS62 | | | | | | | | | | | | | | | | | (1) |
| L | H | L | L | X | ↑ | X | Output | | | | | | | | | | | | | | | | | | (2) |
| X | L | L | L | X | ↑ | X | Input | | | | | | | | | | | | | | | | | | (3) |
| H | H | H | H | L | ↑ | d | Hi-Z | a1 | a2 | a3 | a4 | a5 | a6 | a7 | a8 | d | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b7 | |
| L | H | H | H | L | ↑ | d | Output | a1 | a2 | a3 | a4 | a5 | a6 | a7 | a8 | d | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b7 | Serial shifting in the lower reg. "B" |
| X | L | H | H | L | ↑ | d | Input | $I_1$ | $I_2$ | $I_3$ | $I_4$ | $I_5$ | $I_6$ | $I_7$ | $I_8$ | d | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b7 | Entering data and serial shifting |
| H | H | L | H | L | ↑ | d | Hi-Z | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b8 | d | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b7 | |
| L | H | L | H | L | ↑ | d | Output | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b8 | d | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b7 | Transfer up and serial shifting |
| X | L | L | H | L | ↑ | d | Input | ← DOR → | | | | | | | | d | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b7 | DOR function and serial shifting |

X ≡ Don't care

Hi-Z/Output/Input/ ≡ High impedance state/output state/input state

a1...a8/b1...b8 ≡ The content of the upper register "A"/the lower serial shift register "B" before the most recent ↑ transition of the clock

$I_1 \ldots I_8$ ≡ The level of steady state inputs of the I/O pins

DOR ≡ "Data ORing function" ORing data from both I/O pins and register "B", i.e., $I_1$ + b1, $I_2$ + b2, $I_3$ + b3 ... $I_8$ + b8

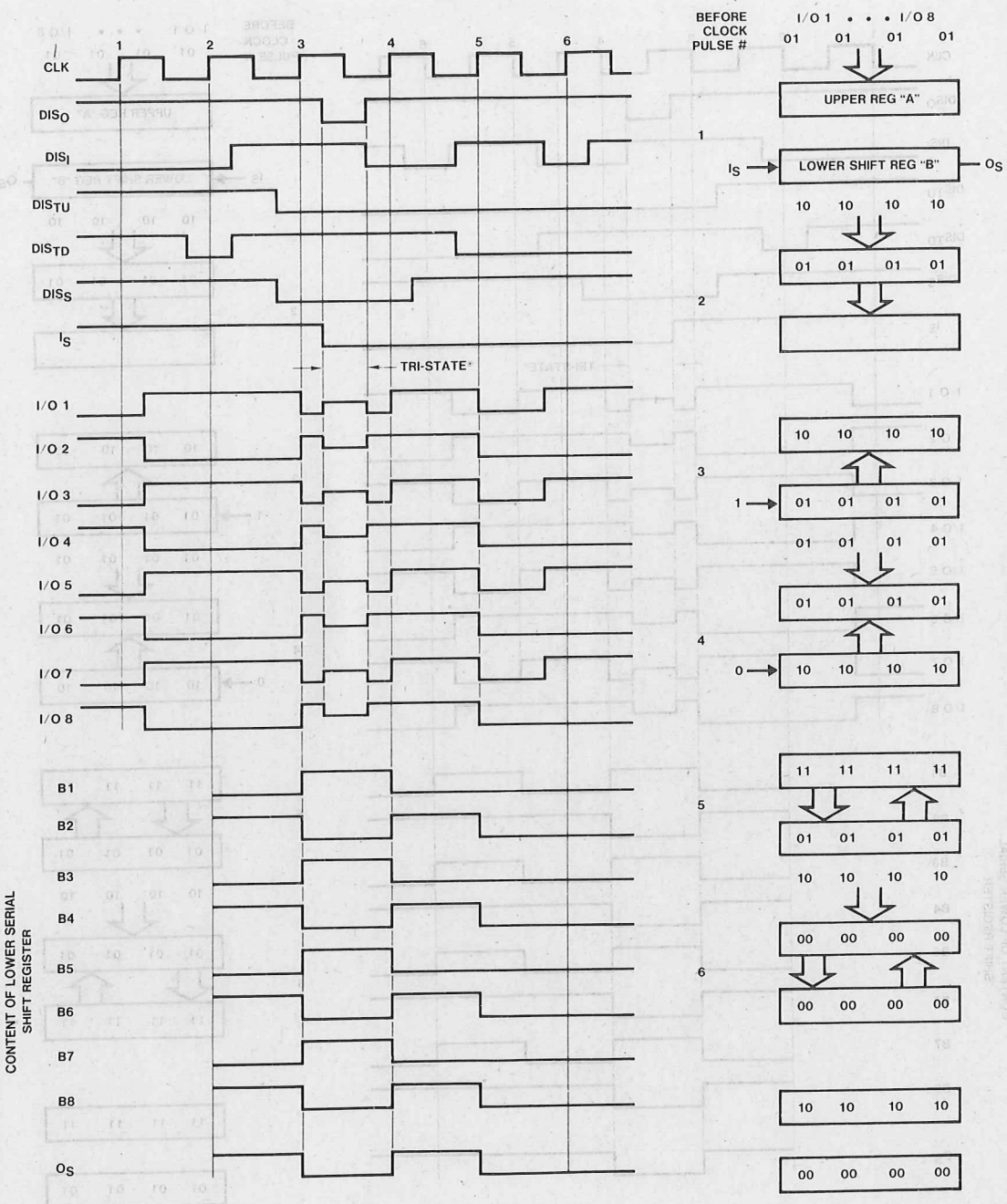
d ≡ Data of the serial input

**Table II**

| | 8-BIT I/O PINS | CONTENT OF UPPER REG. "A" A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | CONTENT OF LOWER SERIAL SHIFT REG. "B" B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 | $O_S$ | COMMENTS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DM76LS52 and DM86LS52 | Hi-Z Output Input | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | (1) Synchronously clear both registers to logic "L" level |
| | | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | (2) |
| | | $I_1$ | $I_2$ | $I_3$ | $I_4$ | $I_5$ | $I_6$ | $I_7$ | $I_8$ | L | L | L | L | L | L | L | L | L | (3) Enter data to reg. "A" clear reg. "B" |
| DM76LS62 and DM86LS62 | Hi-Z Output Input | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b8 | a1 | a2 | a3 | a4 | a5 | a6 | a7 | a8 | a8 | (1) Exchange data between registers |
| | | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b8 | a1 | a2 | a3 | a4 | a5 | a6 | a7 | a8 | a8 | (2) |
| | | ← DOR → | | | | | | | | a1 | a2 | a3 | a4 | a5 | a6 | a7 | a8 | a8 | (3) Beside data exchanging, reg. "A" will "OR" data from I/O and reg. "B" |

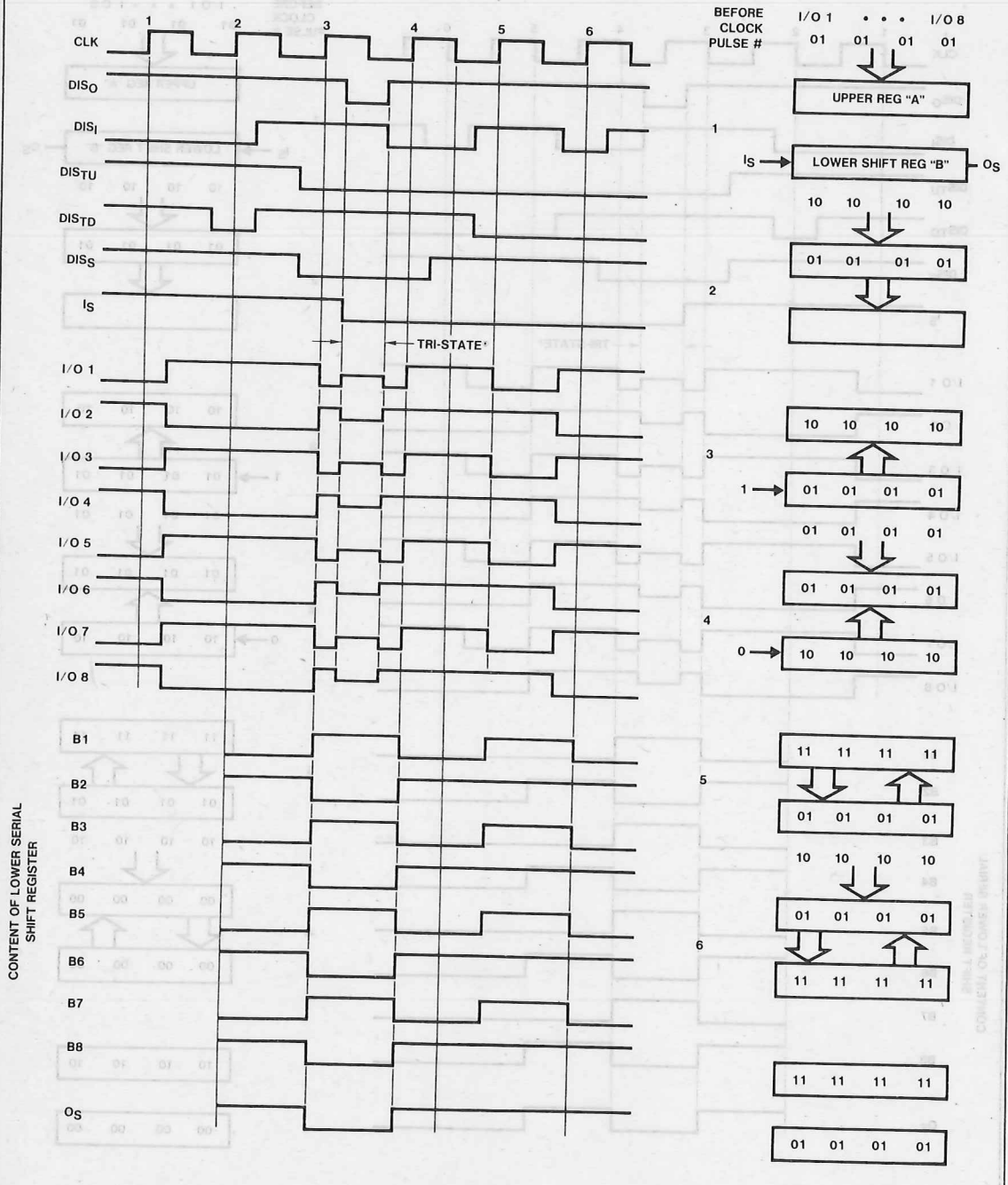
## Timing Diagrams

DM54/74LS952

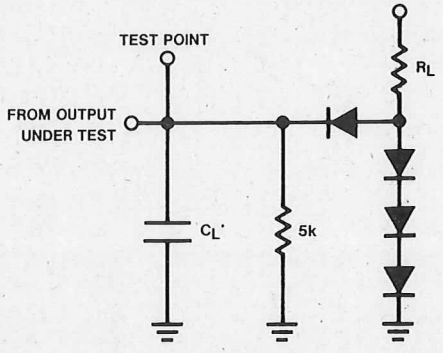


## Timing Diagrams (continued)

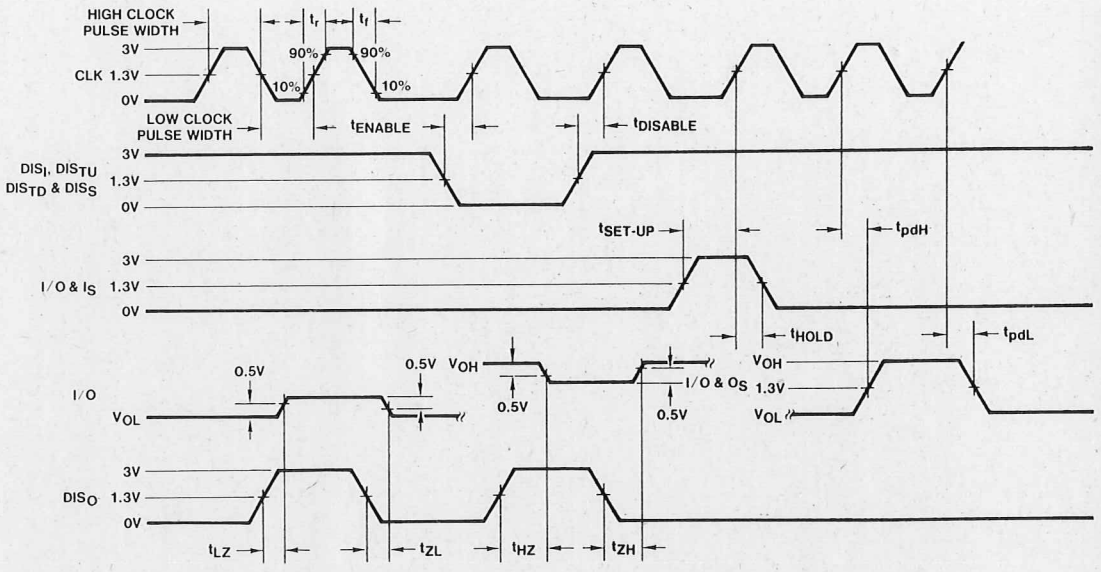
**DM54/74LS962**



## AC Test Circuit and Switching Time Waveforms



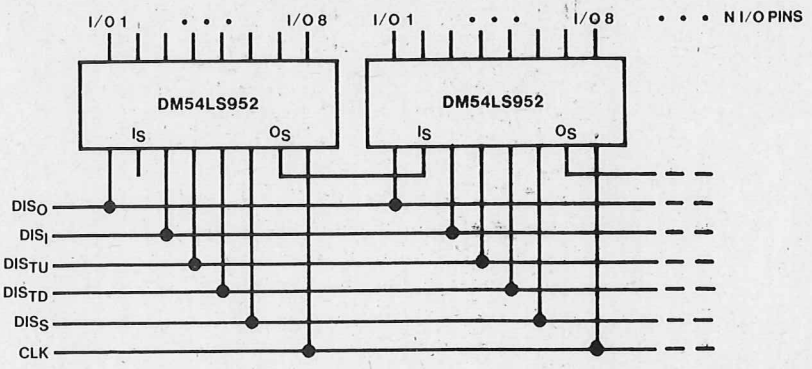

All diodes are 1N916 or 1N3064.
$C_L$ includes probe and jig capacitance.

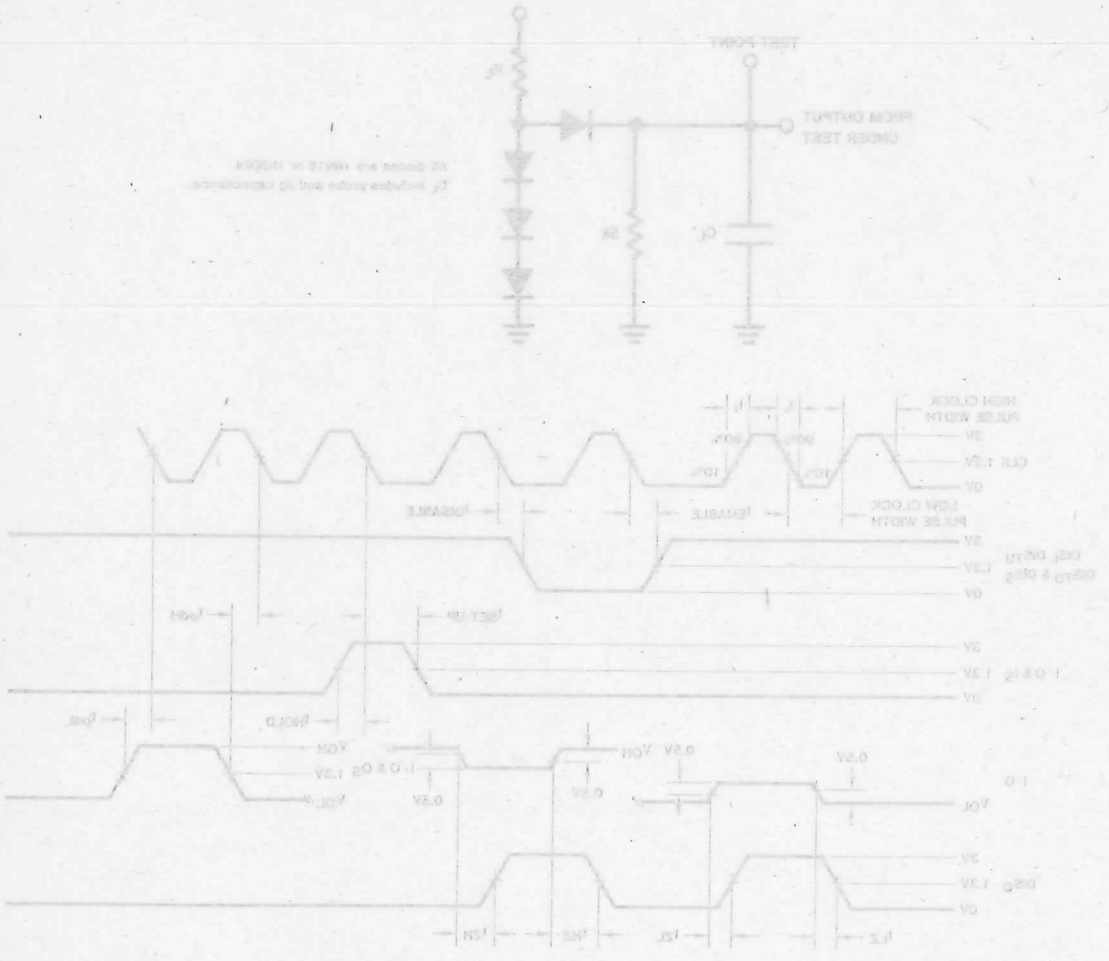



All input pulses are supplied by generators having $t_r \leq 15$ ns, $t_f \leq 6$ ns, PRR $\leq 1$ MHz, $Z_{OUT} \approx 50\ \Omega$.

## Cascading Packages

**Cascading Packages for N-Bit Word**





## Cascading Packages

# Section 7
# Additional Device Specifications

7


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| TEMPERATURE RANGE −55°C to +125°C | TEMPERATURE RANGE 0°C to +70°C | DESCRIPTION | PAGE NUMBER |
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## Successive Approximation Registers

## General Description

The DM2502, DM2503 and DM2504 are 8-bit and 12-bit TTL registers designed for use in successive approximation A/D converters. These devices contain all the logic and control circuits necessary (in combination with a D/A converter) to perform successive approximation analog-to-digital conversions.

The DM2502 has 8 bits with serial capability and is not expandable.

The DM2503 has 8 bits and is expandable without serial capability.

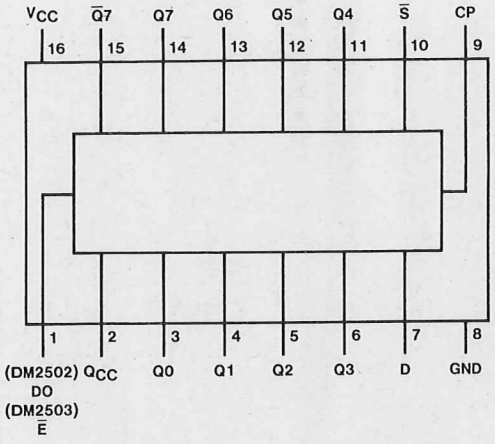
The DM2504 has 12 bits with serial capability and expandability.

All three devices are available in ceramic DIP, ceramic flatpak, and molded Epoxy-B DIPs. The DM2502, DM2503 and DM2504 operate over −55°C to +125°C; the DM2502C, DM2503C and DM2504C operate over 0°C to +70°C.

## Features

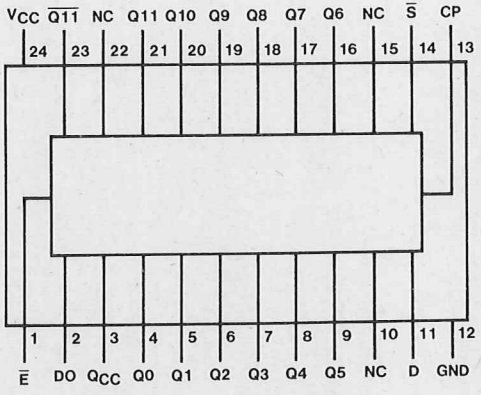
- Complete logic for successive approximation A/D converters
- 8-bit and 12-bit registers
- Capable of short cycle or expanded operation
- Continuous or start-stop operation
- Compatible with D/A converters using any logic code
- Active low or active high logic outputs
- Use as general purpose serial-to-parallel converter or ring counter

## Connection Diagrams




2502 (J,W)
2503 (J,W)

2502C (N)
2503C (N)




2504 (J,F)

2504C (N)

7

## Truth Table

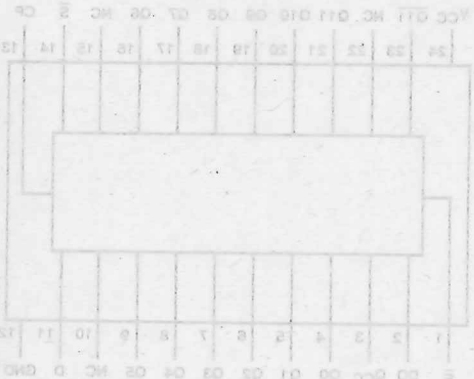
| Time | Inputs | | | Outputs (1) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_n$ | D | $\overline{S}$ | $\overline{E}$ (2) | D0 (3) | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | $Q_{CC}$ |
| 0 | X | L | L | X | X | X | X | X | X | X | X | X | X |
| 1 | D7 | H | L | X | L | H | H | H | H | H | H | H | H |
| 2 | D6 | H | L | D7 | D7 | L | H | H | H | H | H | H | H |
| 3 | D5 | H | L | D6 | D7 | D6 | L | H | H | H | H | H | H |
| 4 | D4 | H | L | D5 | D7 | D6 | D5 | L | H | H | H | H | H |
| 5 | D3 | H | L | D4 | D7 | D6 | D5 | D4 | L | H | H | H | H |
| 6 | D2 | H | L | D3 | D7 | D6 | D5 | D4 | D3 | L | H | H | H |
| 7 | D1 | H | L | D2 | D7 | D6 | D5 | D4 | D3 | D2 | L | H | H |
| 8 | D0 | H | L | D1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | L | H |
| 9 | X | H | L | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | L |
| 10 | X | X | L | X | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | L |
| | X | X | H | X | H | NC | NC | NC | NC | NC | NC | NC | NC |

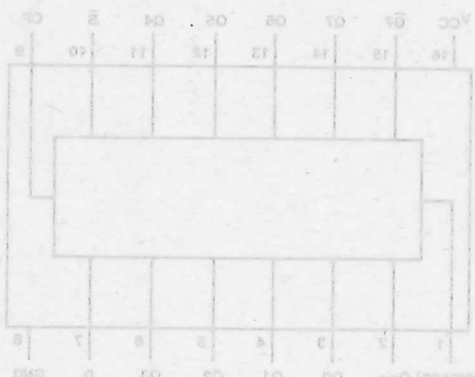
**Note 1:** Truth table for DM2504 is extended to include 12 outputs.

**Note 2:** Truth table for DM2502 does not include $\overline{E}$ column or last line in truth table shown.

**Note 3:** Truth table for DM2503 does not include D0 column.

H = High Level
L = Low Level
X = Don't Care
NC = No Change





## Application Information

### OPERATION

The registers consist of a set of master latches that act as the control elements in the device and change state on the input clock high-to-low transition and a set of slave latches that hold the register data and change on the input clock low-to-high transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the D0 output on the DM2502 and DM2504 when the clock goes from low-to-high. There are no restrictions on the data input; it can change state at any time except during a short interval centered about the clock low-to-high transition. At the same time that data enters the register bit the next less significant bit register is set to a low ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal low during the clock low-to-high transition. The register synchronously resets to the state Q7 (11) low, and all the remaining register outputs high. The $Q_{CC}$ (Conversion Complete) signal is also set high at this time. The $\overline{S}$ signal should not be brought back high until after the clock low-to-high transition in order to guarantee correct resetting. After the clock has gone high resetting the register, the $\overline{S}$ must be removed. On the next clock low-to-high transition the data on the D input is set into the Q7 (11) register bit and the Q6 (10) register bit is set to a low ready for the next clock cycle. On the next clock low-to-high transition data enters the Q6 (10) register bit and Q5 (9) is set to a low. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q0, the $Q_{CC}$ signal goes low, and the register is inhibited from further change until reset by a Start signal.

The DM2502, DM2503 and DM2504 have a specially tailored two-phase clock generator to provide non-overlapping two-phase clock pulses (i.e., the clock waveforms intersect below the thresholds of the gates they drive). Thus, even at very slow dV/dt rates at the clock input (such as from relatively weak comparator outputs), improper logic operation will not result.

### LOGIC CODES

All three registers can be operated with various logic codes. Two's complement code is used by offsetting the comparator ½ full range + ½ LSB and using the complement of the MSB ($\overline{Q7}$ or $\overline{Q11}$) with a binary D/A converter. Offset binary is used in the same manner but with the MSB (Q7 or Q11). BCD D/A converters can be used with the addition of illegal code suppression logic.

### ACTIVE HIGH OR ACTIVE LOW LOGIC

The register can be used with either D/A converters that require a low voltage level to turn on, or D/A converters that require a high voltage level to turn the switch on. If D/A converters are used which turn on with a low logic level, the resulting digital output from the register is active low. That is, a logic "1" is represented as a low voltage level. If D/A converters are used that turn on with a high logic level then the digital output is active high; a logic "1" is represented as a high voltage level.

### EXPANDED OPERATION

An active low enable input, $\overline{E}$, on the DM2503 and DM2504 allows registers to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs in parallel and connecting the $Q_{CC}$ output of one register to the $\overline{E}$ input of the next less significant register. When the start signal resets the register, the $\overline{E}$ signal goes high, forcing the Q7 (11) bit high and inhibiting the register from accepting data until the previous register is full and its $Q_{CC}$ goes low. If only one register is used the $\overline{E}$ input should be held at a low logic level.

### SHORT CYCLE

If all bits are not required, the register may be truncated and conversion time saved by using a register output going low rather than the $Q_{CC}$ signal to indicate the end of conversion. If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power turn-on. This condition can be avoided by making the start input the OR function of $Q_{CC}$ and the appropriate register output.

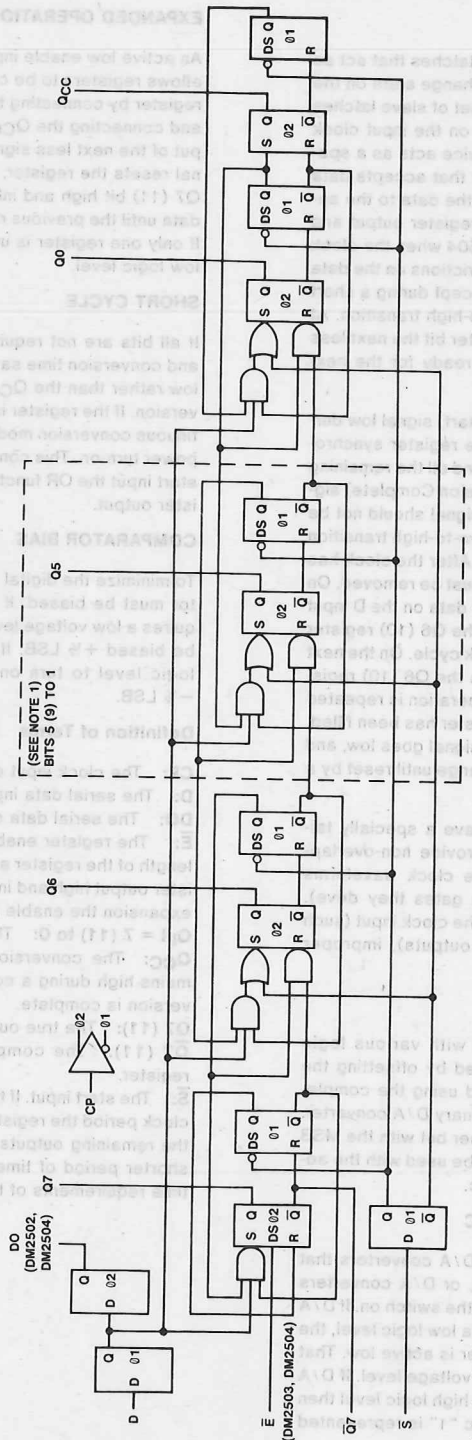
### COMPARATOR BIAS

To minimize the digital error below ± ½ LSB, the comparator must be biased. If a D/A converter is used which requires a low voltage level to turn on, the comparator should be biased +½ LSB. If the D/A converter requires a high logic level to turn on, the comparator must be biased −½ LSB.

### Definition of Terms (See Timing Diagram)

**CP:** The clock input of the register.
**D:** The serial data input of the register.
**DO:** The serial data out. (The D input delayed one bit).
**$\overline{E}$:** The register enable. This input is used to expand the length of the register and when high forces the Q7 (11) register output high and inhibits conversion. When not used for expansion the enable is held at a low logic level (ground).
**$Q_i$ i = 7 (11) to 0:** The outputs of the register.
**$Q_{CC}$:** The conversion complete output. This output remains high during a conversion and goes low when a conversion is complete.
**Q7 (11):** The true output of the MSB of the register.
**$\overline{Q7}$ (11):** The complement output of the MSB of the register.
**$\overline{S}$:** The start input. If the start input is held low for at least a clock period the register will be reset to Q7 (11) low and all the remaining outputs high. A start pulse that is low for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

## Logic Diagram




**Note 1:** Cell logic is repeated for register stages.
Q5 to Q1 DM2502, DM2503
Q9 to Q1 DM2504

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM25 | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 02, 02C | | | 03, 03C | | | 04, 04C | | | |
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −480 | | | −480 | | | −480 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OH}$ = −480 μA | | 2.4 | 3.6 | | 2.4 | 3.6 | | 2.4 | 3.6 | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 9.6 | | | 9.6 | | | 9.6 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 9.6 mA | | | 0.2 | 0.4 | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max<br>$V_I$ = 2.4 V | CP Input | | 6 | 40 | | 6 | 40 | | 6 | 40 | μA |
| | | | D, $\overline{E}$, $\overline{S}$ Inputs | | 12 | 80 | | 12 | 80 | | 12 | 80 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max<br>$V_I$ = 0.4 V | CP Input | | −1.0 | −1.6 | | −1.0 | −1.6 | | −1.0 | −1.6 | mA |
| | | | D, $\overline{E}$, $\overline{S}$ Inputs | | −2.0 | −3.2 | | −2.0 | −3.2 | | −2.0 | −3.2 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −10 | −20 | −45 | −10 | −20 | −45 | −10 | −20 | −45 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | Military | | 65 | 85 | | 60 | 80 | | 90 | 110 | mA |
| | | | Commercial | | 65 | 95 | | 60 | 90 | | 90 | 124 | |

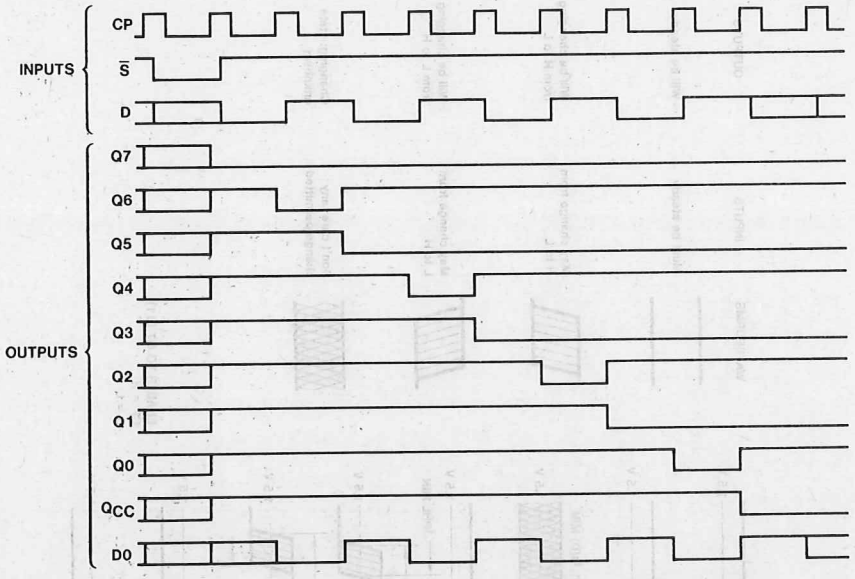
**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

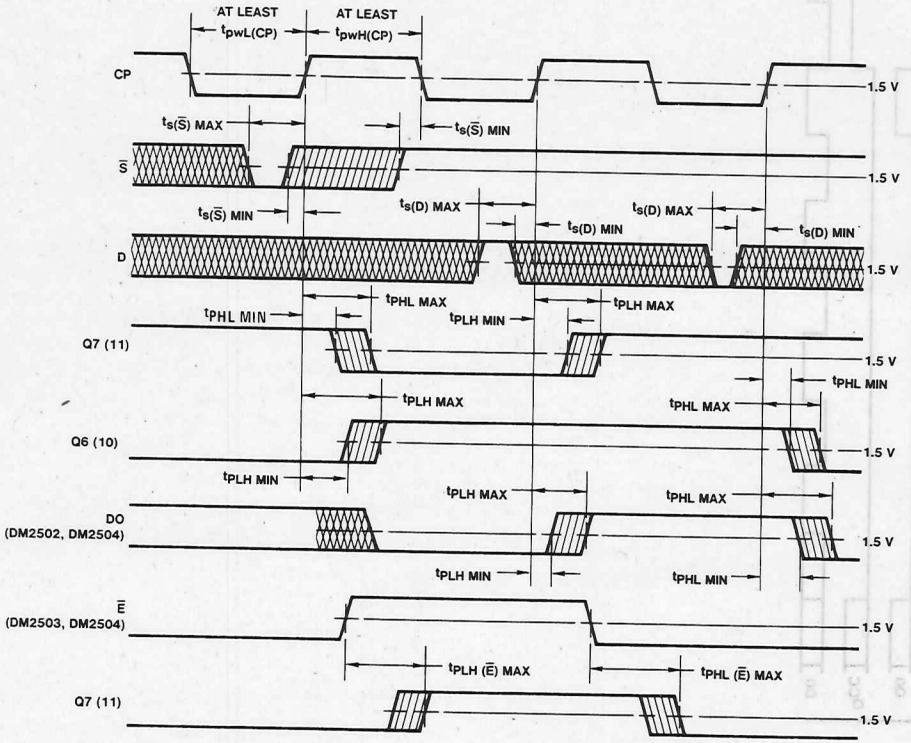
| Parameter | | | From | To | Conditions | DM25 | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 02, 02C | | | 03, 03C | | | 04, 04C | | | |
| | | | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | | | $C_L$ = 15 pF<br>$R_L$ = 400 Ω | 15 | 21 | | 15 | 21 | | 15 | 21 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | CP | Output | | 10 | 26 | 38 | 10 | 26 | 38 | 10 | 26 | 38 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 10 | 18 | 28 | 10 | 18 | 28 | 10 | 18 | 28 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | $\overline{E}$ | Q7 (Q11)<br>CP High<br>$\overline{S}$ Low | | | | N/A | | 13 | 19 | | 13 | 19 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | | N/A | | 16 | 24 | | 16 | 24 | ns |
| $t_W$ | Width of Clock Pulse | Low Level | | | | 42 | 30 | | 42 | 30 | | 42 | 30 | | ns |
| | | High Level | | | | 24 | 17 | | 24 | 17 | | 24 | 17 | | |
| $t_{SETUP}$ | Setup Time | $\overline{S}$ Input | | | | 16 | 9 | | 16 | 9 | | 16 | 9 | | ns |
| | | D Input | | | | 8 | 4 | | 8 | 4 | | 8 | 4 | | |

## Timing Diagram

02, 03



## Switching Time Waveforms



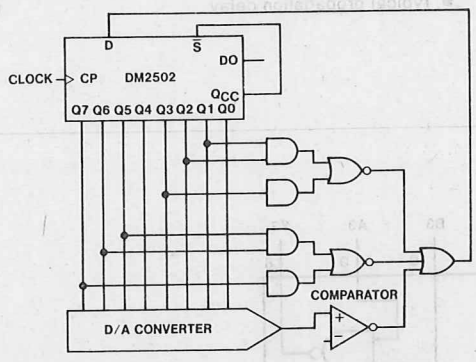

| WAVEFORMS | INPUTS | OUTPUTS |
|---|---|---|
| | Must be steady | Will be steady |
| | May change from H to L | Will be changing from H to L |
| | May change from L to H | Will be changing from L to H |
| | Don't care: any change permitted | Changing: state unknown |

ENABLE TO Q7 (11)
$\overline{CP}$ = H
$\overline{S}$ = L

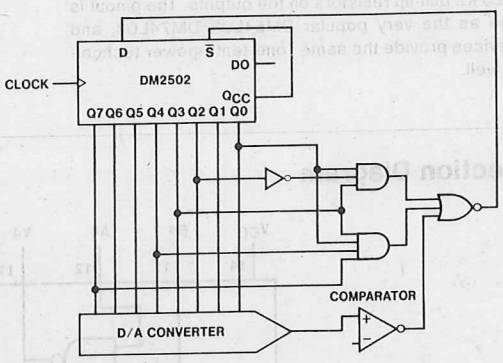
## Typical Applications

### BCD Illegal Code Suppression

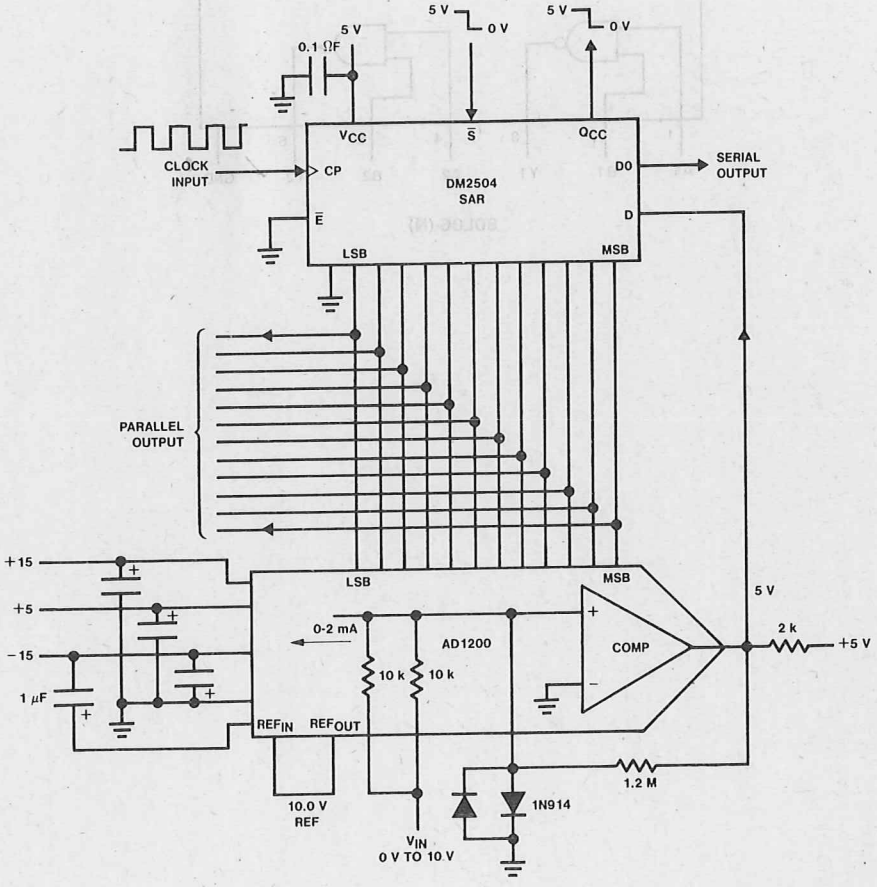
Active High




Active Low




### High Speed 12-BIT A/D Converter



# Quad 2-Input NAND Gates with Resistive Pull Up

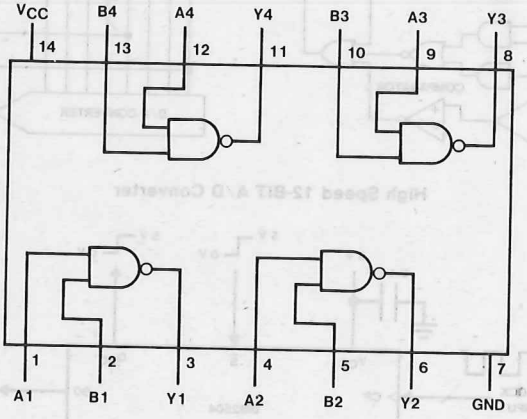
## General Description

These quad two-input NAND gates feature internally connected, 20 kΩ pull-up resistors on the outputs. The pinout is the same as the very popular DM54L03/DM74L03, and these devices provide the same "one-tenth-power technology" as well.

## Features

- Typical power dissipation 12 mW
- Typical propagation delay 115 ns

## Connection Diagram




80L06 (N)

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | DM80 L06 | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.7 | V |
| $I_{OH}$ | High Level Output Current | | | | −200 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = 5.0 V, $V_{IL}$ = 0.7 V, $I_{OH}$ = −100 μA | 2.0 | 2.5 | | V |
| $I_{OL}$ | Low Level Output Current | | | | 3.6 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max, $V_{IH}$ = 2 V | | | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | 100 | μA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | <1 | 10 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.3 V | | −0.12 | −0.18 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max | −0.17 | −0.25 | −0.33 | mA |
| $I_{CCH}$ | Supply Current (Total with Outputs High) | $V_{CC}$ = Max, $V_I$ = 0 | | 0.48 | 0.8 | mA |
| $I_{CCL}$ | Supply Current (Total with Outputs Low) | $V_{CC}$ = Max, $V_I$ = 5 V | | 2.38 | 3.68 | mA |

Note 1: All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C.

| Parameter | | From (Input) | To (Output) | Conditions | DM80 L06 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Input | Output | $C_L$ = 15 pF, $R_L$ = 4 kΩ | | 193 | 290 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 37 | 56 | ns |

# Dual 5-Input NAND Gates

## General Description

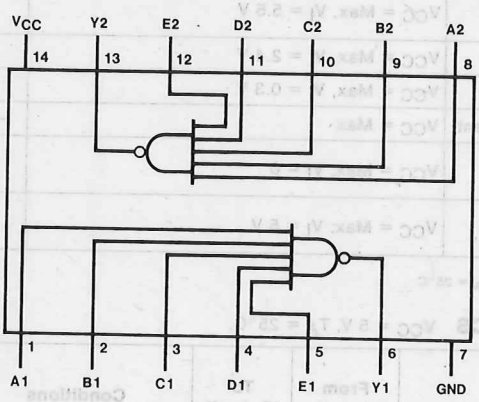
**DM7092/DM8092**

These devices provide two, 5-input NAND gates in the same package. Their primary advantage is that they fill a product void in the popular DM5400/DM7400 family. The electrical specifications are completely compatible with the series 54/74 devices.

## Features

- Typical propagation delay 11 ns
- Typical power dissipation 35 mW

## Connection Diagrams




7092 (J,W); 8092 (N)

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | DM70/80 92 | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA, $T_A$ = 25°C | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2.0 V, $I_{OL}$ = Max | | | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | −18 | | −55 | mA |
| $I_{CCH}$ | Supply Current (Total with Outputs High) | VCC = Max, $V_I$ = 0 | | | 3.6 | mA |
| $I_{CCL}$ | Supply Current (Total with Outputs Low) | $V_{CC}$ = Max, $V_I$ = 5.0 V | | | 10.2 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From | To | Conditions | DM70/80 92 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Input | Output | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 13 | 25 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Input | Output | | | 8 | 15 | ns |

# TRI-STATE® Quad Buffers

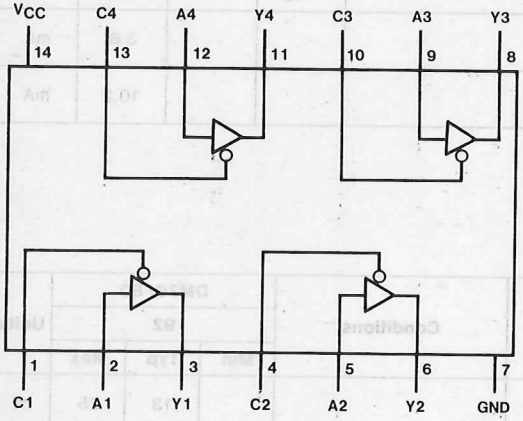
## General Description

The DM7093/DM8093 and DM7094/DM8094 are quad two-input buffers which accept normal TTL or DTL input levels; and have outputs which provide either normal low-impedance TTL characteristics, or a high-impedance third logic state. One of the two inputs to each buffer is used as a control line to gate the output into the high-impedance state. The other input simple passes the non-inverted data through the buffer. The DM7093/DM8093 provides the high-impedance state when a high logic level is applied to the control input, the DM7094/DM8094 when a low logic level is applied to the control input. The low output inpedance of these devices provides good capacitive-drive capability and rapid transition from the low to the high logic levels, thus assuring both speed and waveform integrity. It is possible to connect as many as 128 devices to a common bus line, and still have adequate drive capability.

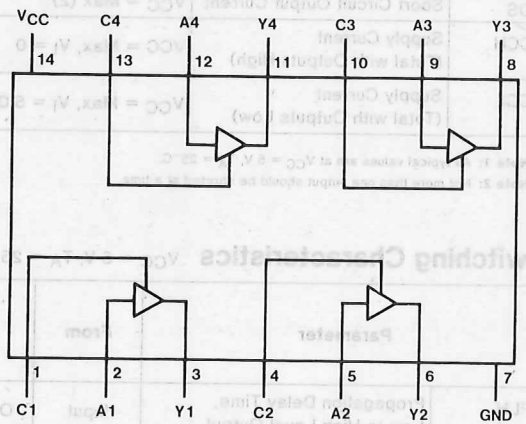
## Features

- Pin equivalent to DM54125/74125 (7093/8093) and DM54126/74126 (7094/8094)
- Up to 128 devices can be connected to a common bus line
- High capacitive-drive capability
- Independent control of each buffer
- Typical propagation delay—12 ns

## Connection Diagrams




7093 (J,W); 8093 (N)




7094 (J,W); 8094 (N)

## Truth Tables

DM7093/DM8093

| Data | Controls | Outputs |
|---|---|---|
| H | L | H |
| L | L | L |
| X | H | Hi-Z |

DM7094/DM8094

| Data | Controls | Outputs |
|---|---|---|
| H | H | H |
| L | H | L |
| X | L | Hi-Z |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | DM70 93, 94 | | | DM80 93, 94 | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ Min, $I_I = -12$ mA | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | −2.0 | | | −5.2 | mA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | 2.4 | 3.4 | | 2.4 | 3.1 | | V |
| $I_{OL}$ | Low Level Output Current | | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | V |
| $I_{O(OFF)}$ | Off-State (High Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $V_O$ = 0.4 V | | | −40 | | | −40 | μA |
| | | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $V_O$ = 2.4 V | | | 40 | | | 40 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | −1.6 | | | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | −30 | | −70 | −28 | | −70 | mA |
| $I_{CCH}$ | Supply Current (Total, Outputs High) | $V_{CC}$ = Max | | 32 | 54 | | 32 | 54 | mA |
| $I_{CCL}$ | Supply Current (Total, Outputs Low) | $V_{CC}$ = Max | | 36 | 62 | | 36 | 62 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | DM70/80 93 | | | DM70/80 94 | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $C_L$ = 50 pF, $R_L$ = 400 Ω | | 10 | 15 | | 10 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | 12 | 18 | | 12 | 18 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | | | 12 | 18 | | 13 | 19 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | 16 | 25 | | 16 | 25 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | $C_L$ = 5 pF, $R_L$ = 400 Ω | | 5 | 8 | | 10 | 16 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | | 9 | 14 | | 14 | 20 | ns |

7

# TRI-STATE® Hex Buffers

## General Description

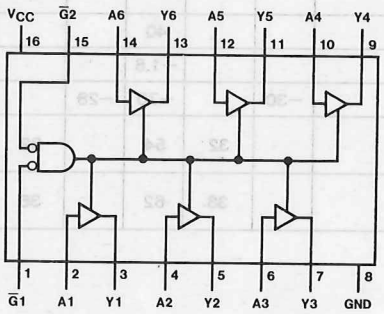
These devices provide six, two-input buffers in each package. Both the standard (7400 compatible) TTL technology, and the "true tenth-power" (74L compatible) low power versions are available for each of the four types. One of the two inputs to each buffer is used as a control line to gate the output into the high-impedance state, while the other input passes the data through the buffer. The 95 and 97 present the true data at the outputs, while the 96 and 98 are inverting. On the 95 and 96 versions, all six control lines for TRI-STATE enable are common in a single line. On the 97 and 98 versions, four buffers are enabled from a common line, and the other two buffers from a separate common line. In all cases, the outputs are placed in the TRI-STATE condition by applying a high logic level to the control pins. With either the standard TTL or the low power versions of these circuits, it is possible to connect over 100 like devices to a common bus line and still have adequate drive capability.

## Features

| Type | Typical Power Dissipation | Typical Propagation Delay |
|---|---|---|
| 95, 97 | 325 mW | 12 ns |
| L95, L97 | 20 mW | 34 ns |
| 96, 98 | 295 mW | 11 ns |
| L96, L98 | 15 mW | 31 ns |

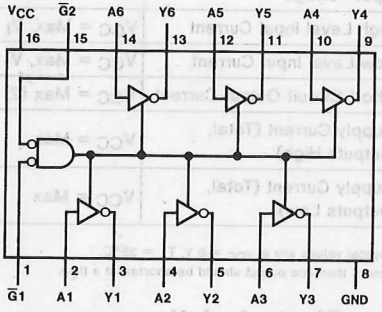
- Pin equivalent to DM54365 (95), DM54366 (96), DM54367 (97), DM54368 (98)

## Connection Diagrams



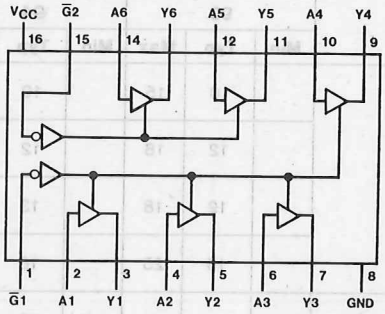

**7095 (J,W)**
**70L95 (J,W)**

**8095 (N)**
**80L95 (N)**



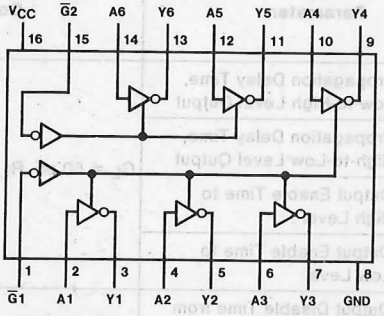

**7096 (J,W)**
**70L96 (J,W)**

**8096 (N)**
**80L96 (N)**




**7097 (J,W)**
**70L97 (J,W)**

**8097 (N)**
**80L97 (N)**




**7098 (J,W)**
**70L98 (J,W)**

**8098 (N)**
**80L98 (N)**

## Truth Table (Each Driver)

**95, L95**

| Inputs | | | Outputs |
|---|---|---|---|
| G̅1 | G̅2 | A | Y |
| H | X | X | Hi-Z |
| X | H | X | Hi-Z |
| L | L | H | H |
| L | L | L | L |

**96, L96**

| Inputs | | | Outputs |
|---|---|---|---|
| G̅1 | G̅2 | A | Y |
| H | X | X | Hi-Z |
| X | H | X | Hi-Z |
| L | L | H | L |
| L | L | L | H |

**97, L97**

| Inputs | | Outputs |
|---|---|---|
| G̅ | A | Y |
| H | X | Hi-Z |
| L | H | H |
| L | L | L |

**98, L98**

| Inputs | | Outputs |
|---|---|---|
| G̅ | A | Y |
| H | X | Hi-Z |
| L | H | L |
| L | L | H |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM70/80 95, 96, 97, 98 | | | DM70/80 L95, L96, L97, L98 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | | | 0.7 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | N/A | V |
| $I_{OH}$ | High Level Output Current | | DM70 | | | −2.0 | | | −1.0 | mA |
| | | | DM80 | | | −5.2 | | | −1.0 | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | 2.4 | 3.1 | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | DM70 | | | 32 | | | 2.0 | mA |
| | | | DM80 | | | 32 | | | 3.6 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OL}$ = Max | DM70 | | | 0.4 | | | 0.3 | V |
| | | | DM80 | | | 0.4 | | | 0.4 | |
| $I_{O(OFF)}$ | Off-State (High-Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $V_O$ = 0.3 V | | | | | | −10 | μA |
| | | | $V_O$ = 0.4 V | | | −40 | | | | |
| | | | $V_O$ = 2.4 V | | | 40 | | | 10 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | | | 10 | μA |
| $I_{IL}$ | Level Input Current, A Input | $V_{CC}$ = Max, Both $\overline{G}$ Inputs at 2 V | $V_I$ = 0.3 V | | | | | | −10 | μA |
| | | | $V_I$ = 0.5 V | | | −40 | | | | |
| | | $V_{CC}$ = Max, Both $\overline{G}$ Inputs at 0.4 V | $V_I$ = 0.3 V | | | | | | −0.18 | mA |
| | | | $V_I$ = 0.4 V | | | −1.6 | | | | |
| | $\overline{G}$ Input | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | | −0.18 | mA |
| | | | $V_I$ = 0.4 V | | | −1.6 | | | | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −40 | | −115 | −3 | | −15 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | 95, 97 | | 65 | 85 | | 4.0 | 5.8 | mA |
| | | | 96, 98 | | 59 | 77 | | 3.0 | 4.5 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time, and for the DM70/DM8095, 96, 97, 98 duration of short circuit should not exceed one second.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | | | DM70/80 95, 97 | | DM70/80 96, 98 | | DM70/80 L95, L97 | | DM70/80 L96, L98 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Both | Std. | Low Power | Typ | Max | Typ | Max | Typ | Max | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $C_L$ = 50 pF | $R_L$ = 400 Ω | $R_L$ = 4 kΩ | 10 | 16 | 11 | 17 | 30 | 60 | 26 | 48 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | 14 | 22 | 10 | 16 | 37 | 75 | 35 | 53 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | | | | 21 | 35 | 21 | 35 | 47 | 96 | 42 | 90 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | | 24 | 37 | 24 | 37 | 21 | 45 | 42 | 75 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | $C_L$ = 5 pF | | | 6 | 11 | 6 | 11 | 47 | 90 | 25 | 43 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | | | 16 | 27 | 16 | 27 | 30 | 63 | 34 | 63 | ns |

# TRI-STATE® Data Selectors/Multiplexers

## General Description

These data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources, and feature a strobe-controlled TRI-STATE output. The strobe must be at a low logic level to enable these devices. The TRI-STATE outputs permit direct connection to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transitors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

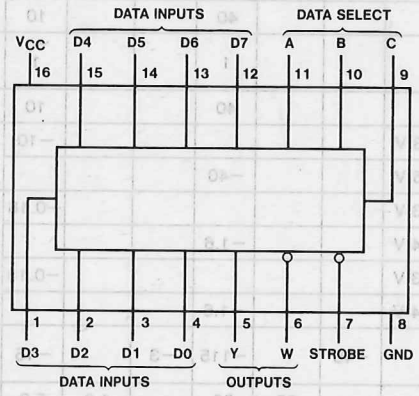
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

## Features

- TRI-STATE versions of DM54/74151
- Interface directly with system bus
- Perform parallel-to-serial conversion
- Permit multiplexing from N-lines to one line
- Complementary outputs provide true and inverted data
- Pin equivalent DM54251/DM74251

| Type | Max No. of Common Outputs | Typical Prop Delay Time (D to Y) | Typical Power Dissipation |
|---|---|---|---|
| DM7121 | 49 | 17 ns | 155 mW |
| DM8121 | 129 | 17 ns | 155 mW |

## Connection Diagram



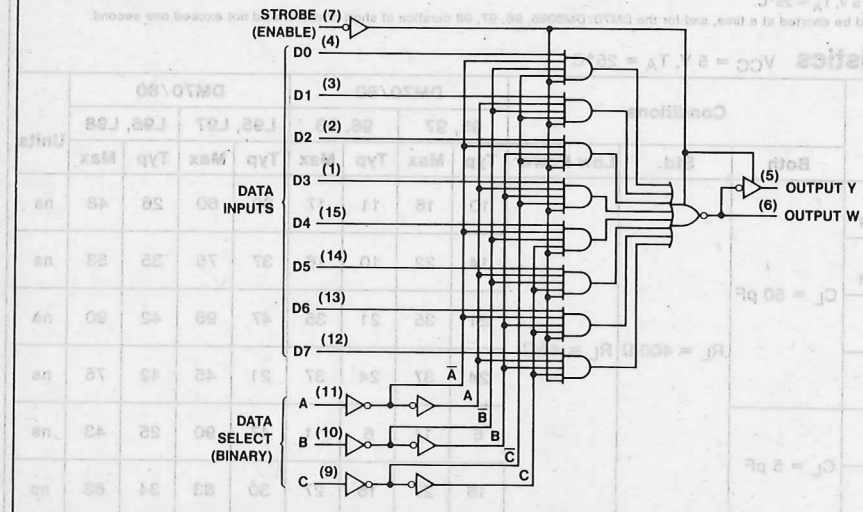

7121 (J,W); 8121 (N)

## Truth Table

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| Select | | | Strobe | | |
| C | B | A | S | Y | W |
| X | X | X | H | Z | Z |
| L | L | L | L | D0 | $\overline{D0}$ |
| L | L | H | L | D1 | $\overline{D1}$ |
| L | H | L | L | D2 | $\overline{D2}$ |
| L | H | H | L | D3 | $\overline{D3}$ |
| H | L | L | L | D4 | $\overline{D4}$ |
| H | L | H | L | D5 | $\overline{D5}$ |
| H | H | L | L | D6 | $\overline{D6}$ |
| H | H | H | L | D7 | $\overline{D7}$ |

H = High Logic Level, L = Low Logic Level
X = Don't Care, Z = High Impedance (Off)
D0, D1...D7 = The level of the respective D input.

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM71/81 | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | 21 | | | |
| | | | | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | DM54 | | | −2 | mA |
| | | | DM74 | | | −5.2 | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | | 0.4 | V |
| $I_{O(OFF)}$ | Off-State (High-Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V | $V_O$ = 0.4 V | | | −40 | μA |
| | | | $V_O$ = 2.4 V | | | 40 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −18 | | −70 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | | 31 | 51 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.
**Note 3:** All inputs at 4.5 V and all outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Conditions | DM71/81 21 Min | DM71/81 21 Typ | DM71/81 21 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A, B, or C (4 levels) | Y | $C_L$ = 50 pF, $R_L$ = 400 Ω | | 22 | 36 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 23 | 36 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A, B, or C (3 levels) | W | | | 18 | 29 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 16 | 27 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Any D | Y | | | 17 | 28 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 18 | 28 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | W | | | 11 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 10 | 15 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | Strobe | Y | | | 15 | 27 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | | | 18 | 36 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | | W | | | 15 | 27 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | | | 19 | 38 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | | Y | $C_L$ = 5 pF, $R_L$ = 400 Ω | | 4 | 8 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | | | | 14 | 23 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | | W | | | 4 | 8 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | | | | 15 | 23 | ns |

# Quad 2-Input Data Selectors/Multiplexers

## General Description

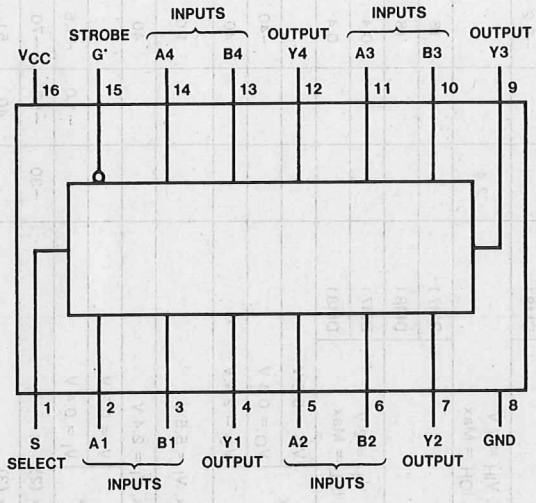
These devices contain four, two-input multiplexers with common input select logic and common output disable circuitry. The DM71L22/81L22 provides conventional totem-pole output TTL construction, whereas the DM7123/8123 and the DM71L23/81L23 provide both conventional TTL outputs and TRI-STATE outputs. When the enable/strobe input is at a low logic level, the outputs of all devices are conventional TTL. However, when the enable/strobe input is raised to a high logic level, the outputs of the DM71L22/81L22 go to the low logic state, and the outputs of the DM7123/8123 and DM71L23/81L23 go to the high-impedance third state. These devices provide the designer with TRI-STATE and/or low power pin/pin replacements for the popular 9322 and 54/74157 multiplexers.

## Features

- Pin equivalents popular 9322 and 54/74157 multiplexers
- Both conventional TTL and TRI-STATE outputs available
- Both conventional TTL and "one-tenth-power technology" available

| Type | Typical Propagation Delay | Typical Power Dissipation |
|---|---|---|
| 7123/8123 | 9.5 ns | 200 mW |
| 71L22/81L22 | 40 ns | 15 mW |
| 71L23/81L23 | 40 ns | 20 mW |

## Connection Diagram




*Enable for '23 and 'L23

71L22 (J,W)
7123 (J,W)
71L23 (J,W)

81L22 (N)
8123 (N)
81L23 (N)

## Truth Tables

L22

| Strobe | Select | Inputs | | Output |
|---|---|---|---|---|
| | | A | B | Y |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |
| H | X | X | X | L |

23, L23

| Enable | Select | Inputs | | Output |
|---|---|---|---|---|
| | | A | B | Y |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |
| H | X | X | X | Hi-Z |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM71/81 23 | | | DM71/81 L22 | | | DM71/81 L23 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | | | 0.7 | | | 0.7 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA, $T_A$ = 25°C | | | | −1.5 | | | N/A | | | N/A | V |
| $I_{OH}$ | High Level Output Current | | DM71 | | | −2.0 | | | −0.2 | | | −0.2 | mA |
| | | | DM81 | | | −5.2 | | | −0.2 | | | −0.2 | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | 2.4 | | | 2.4 | 2.8 | | 2.4 | 2.8 | | V |
| $I_{OL}$ | Low Level Output Current | | DM71 | | | 16 | | | 2.0 | | | 2.0 | mA |
| | | | DM81 | | | 16 | | | 3.6 | | | 3.6 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OL}$ = Max | DM71 | | | 0.4 | | 0.15 | 0.3 | | 0.15 | 0.3 | V |
| | | | DM81 | | | 0.4 | | 0.20 | 0.4 | | 0.20 | 0.4 | |
| $I_{O(OFF)}$ | Off-State (High-Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $V_O$ = 0.3 V | | | | | | N/A | | | −40 | μA |
| | | | $V_O$ = 0.4 V | | | −40 | | | N/A | | | | |
| | | | $V_O$ = 2.4 V | | | 40 | | | N/A | | | 20 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1.0 | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | | | 10 | | | 10 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | | −0.18 | | | −0.18 | mA |
| | | | $V_I$ = 0.4 V | | −1.0 | −1.6 | | | | | | | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −30 | −50 | −70 | −3 | −9 | −15 | −3 | −9 | −15 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | | 40 | 51 | | 3 | 4 | | 4 | 5.3 | mA |

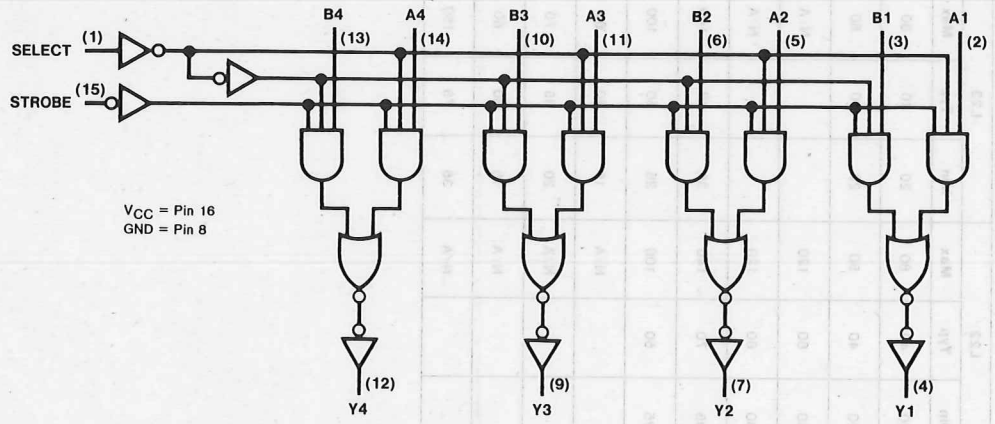
**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.
**Note 3:** $I_{CC}$ is measured with all inputs grounded, and all outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

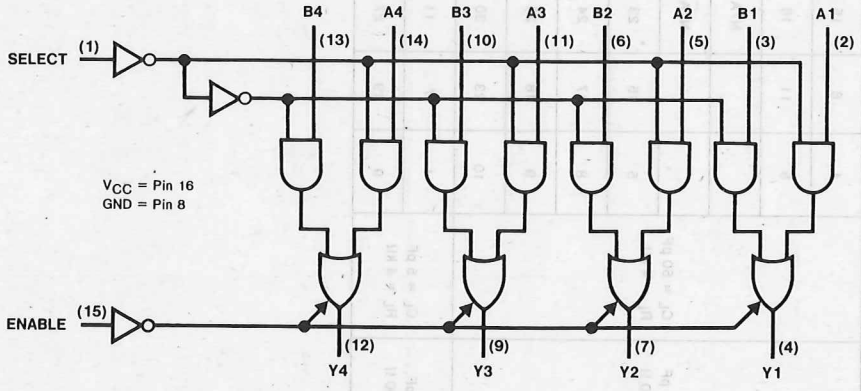
| Parameter | | From | To | Conditions | | DM71/81 | | | DM71/81 | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | DM71/81 | DM71L/81L | 23 | | | L22 | | | L23 | | | |
| | | | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Output | $C_L$ = 50 pF $R_L$ = 400 Ω | $C_L$ = 50 pF $R_L$ = 4 kΩ | 4 | 8 | 15 | 20 | 40 | 80 | 20 | 40 | 80 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Data | Output | | | 5 | 11 | 18 | 20 | 40 | 80 | 20 | 40 | 80 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Strobe | Output | | | | | N/A | 30 | 60 | 120 | | | N/A | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Strobe | Output | | | | | N/A | 30 | 60 | 120 | | | N/A | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Select | Output | | | 5 | 15 | 23 | 35 | 70 | 140 | 35 | 70 | 140 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Select | Output | | | 8 | 17 | 24 | 25 | 50 | 100 | 25 | 50 | 100 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | Enable | Output | | | 9 | 18 | 25 | | | N/A | 15 | 30 | 60 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | Enable | Output | | | 10 | 23 | 30 | | | N/A | 20 | 35 | 70 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | Enable | Output | $C_L$ = 5 pF $R_L$ = 400 Ω | $C_L$ = 5 pF $R_L$ = 4 kΩ | 4 | 7 | 11 | | | N/A | 15 | 30 | 60 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | Enable | Output | | | 9 | 19 | 27 | | | N/A | 35 | 75 | 150 | ns |

## Logic Diagrams

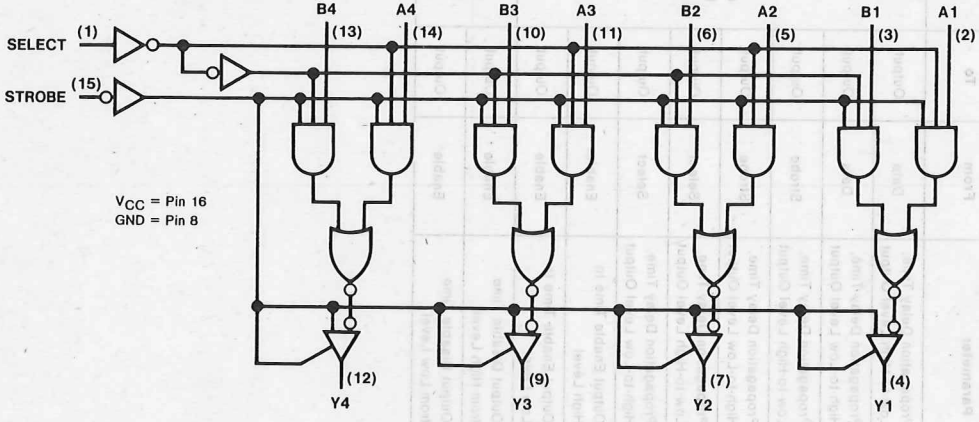
L22




23




L23



# Magnitude Comparators

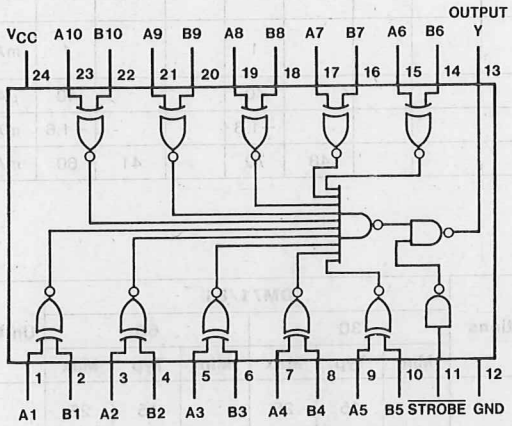
## General Description

These devices offer comparisons to determine equality between two binary words. The DM7130/DM8130 compares two ten-bit words, and the DM7160/DM8160 compares two six-bit words. A strobe override is provided on both devices. When the strobe is taken to a high logic level, the output is forced to a high logic level. The devices also feature open collector outputs for expansion.

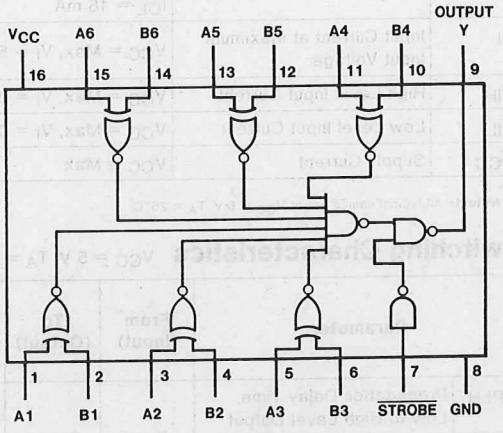
## Features

- Typical propagation delay 21 ns
- Typical power dissipation
  - DM7130/8130 240 mW
  - DM7160/8160 205 mW
- Open-collector outputs for expansion

## Connection Diagrams




7130 (J,F); 8130 (N)




7160 (J,W); 8160 (N)

## Truth Table

| Condition | $\overline{\text{STROBE}}$ S | Output Y |
|---|---|---|
| A = B, A ≠ B | H | H |
| A = B | L | H |
| A ≠ B | L | L |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | DM71/81 | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 30 | | | 60 | | | |
| | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA<br>$T_A$ = 25°C | | | −1.5 | | | −1.5 | V |
| $I_{CEX}$ | High Level Output Current | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{OH}$ = 5.5 V | | | 100 | | | 100 | μA |
| $I_{OL}$ | Low Level Output Current | | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IL}$ = 0.8 V<br>$I_{OL}$ = 16 mA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | −1.6 | | | −1.6 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | 48 | 70 | | 41 | 60 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Conditions | DM71/81 | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 30 | | | 60 | | | |
| | | | | | Min | Typ | Max | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Output | $C_L$ = 15 pF<br>$R_L$ = 400 Ω | | 15 | 25 | | 15 | 25 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 27 | 40 | | 27 | 40 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Strobe | Output | | | 9 | 18 | | 9 | 18 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 20 | 30 | | 20 | 30 | |

# 6-Bit Unified Bus Comparators

## General Description

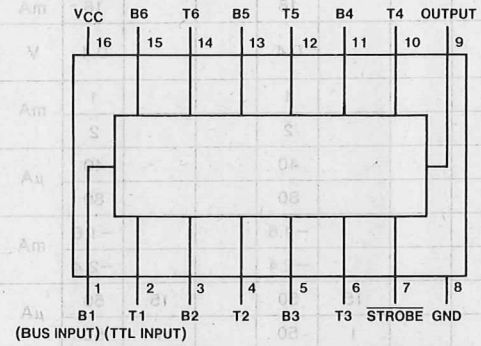
The DM7131/DM8131, DM7136/DM8136 compare two binary words of two-to-six-bits in length, and indicates matching (bit-for-bit) of the two words. Inputs for one word are 54/74 series-compatible TTL inputs, whereas those of the second word are high-impedance receivers driven by a terminated data bus. These bus inputs include 0.65 V typical hysteresis, which provides 1.4 V noise immunity. The DM7131/DM8131 has active pull-up outputs and goes to the low state upon equality. The DM7136/DM8136 has open-collector outputs which go to the high state upon equality, and is expandable to n bits by collector-ORing. Both devices have an output latch which is strobe controlled.

The transfer of information to the output occurs when the $\overline{\text{STROBE}}$ input goes from a logic "1" to a logic "0" state. Inputs may be changed while the $\overline{\text{STROBE}}$ is at the logic "1" level, without affecting the state of the output. These devices are useful as address comparators in computer systems utilizing unified data bus organization.

## Features

- Low bus input current 15 $\mu$A typ
- High bus input noise immunity 1.4 V typ
- Bus inputs comply with IEEE 488-1975
- TTL-compatible output
- Output latch provision

## Connection Diagram



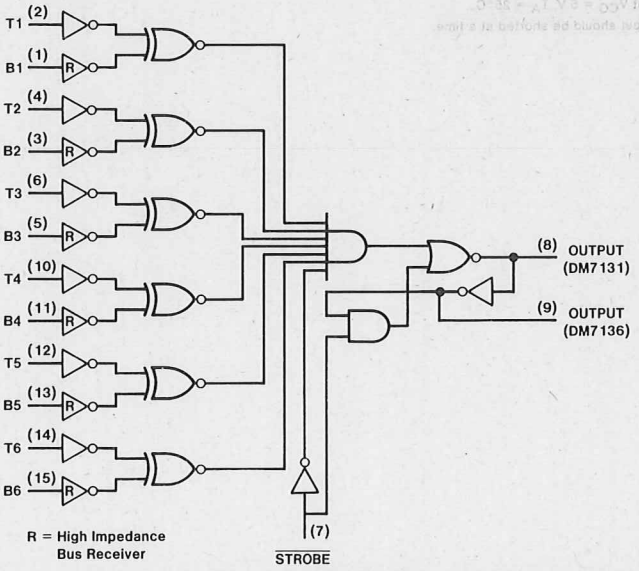

7131 (J,W) 8131 (N)
7136 (J,W) 8136 (N)

## Truth Table

| Condition | $\overline{\text{STROBE}}$ | Output | |
|---|---|---|---|
| | | DM71/8131 | DM71/8136 |
| T = B, T ≠ B | H | $Q_{N-1}$* | $Q_{N-1}$* |
| T = B | L | L | H |
| T ≠ B | L | H | L |

*Latched in previous state

## Logic Diagram



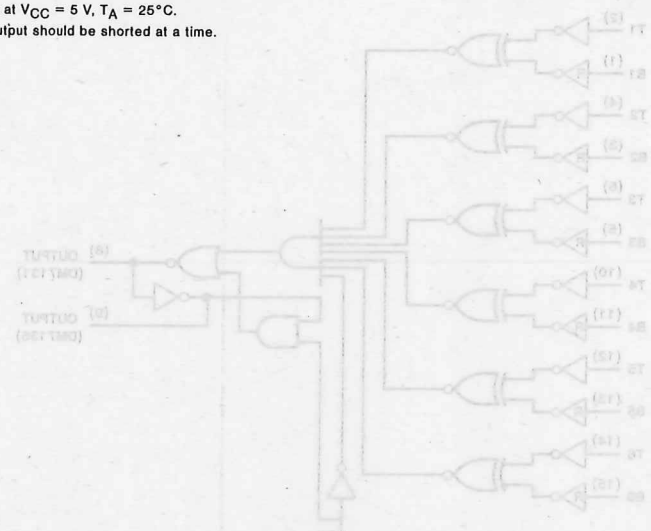

R = High Impedance Bus Receiver

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM71/81 | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 31 | | | 36 | | | |
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | (Exc. Bus Inputs) | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | (Exc. Bus Inputs) | | | | 0.8 | | | 0.8 | V |
| $V_{T+}$ | Positive Going Threshold Voltage | $V_{CC}$ = 5 V, Bus Inputs | DM71 | 1.40 | 1.75 | 2.0 | 1.40 | 1.75 | 2.0 | V |
| | | | DM81 | 1.45 | 1.75 | 1.95 | 1.45 | 1.75 | 1.95 | |
| $V_{T-}$ | Negative Going Threshold Voltage | $V_{CC}$ = 5 V, Bus Inputs | DM71 | 0.90 | 1.10 | 1.35 | 0.90 | 1.10 | 1.35 | V |
| | | | DM81 | 0.95 | 1.10 | 1.30 | 0.95 | 1.10 | 1.30 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA, $T_A$ = 25°C | | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | $V_{CC}$ = Min, $V_{IH}$ = 2 V | $V_{OH}$ = 5.5 V | | | 250 | | | 250 | μA |
| | | | | | | −400 | | | | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | 2.4 | | | | | 5.5 | V |
| $I_{OL}$ | Low Level Output Current | | | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | | 0.4 | | | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | TTL Input | | | 1 | | | 1 | mA |
| | | | Strobe | | | 2 | | | 2 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | TTL Input | | | 40 | | | 40 | μA |
| | | | Strobe | | | 80 | | | 80 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | TTL Input | | | −1.6 | | | −1.6 | mA |
| | | | Strobe | | | −2.4 | | | −2.4 | |
| $I_{IN}$ | Bus Input Current | $V_I$ = 4 V | $V_{CC}$ = Max | | 15 | 50 | | 15 | 50 | μA |
| | | | $V_{CC}$ = 0 | | 1 | 50 | | 1 | 50 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −18 | | −55 | | N/A | | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | 50 | 74 | | 50 | 74 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time.



## Switching Characteristics Table $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Conditions | DM71/81 | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 31 | | | 36 | | | |
| | | | | | Min | Typ | Max | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | TTL Input | Output | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 20 | 30 | | 20 | 30 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 20 | 30 | | 20 | 30 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Bus Input | Output | | | 30 | 45 | | 30 | 45 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 30 | 45 | | 30 | 45 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Strobe Input | Output | | | 20 | 30 | | 20 | 30 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 20 | 30 | | 20 | 30 | |

# DM71/DM81LS95A, LS96A, LS97A, LS98A

## TRI-STATE® Octal Buffers

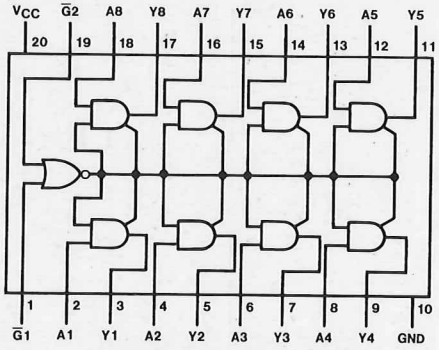
## General Description

These devices provide eight, two-input buffers in each package. All employ the newest low power-Schottky TTL technology. One of the two inputs to each buffer is used as a control line to gate the output into the high-impedance state, while the other input passes the data through the buffer. The 95 and 97 present true data at the outputs, while the 96 and 98 are inverting. On the 95 and 96 versions, all eight TRI-STATE enable lines are common, with access through a 2-input NOR gate. On the 97 and 98 versions, four buffers are enabled from one common line, and the other four buffers are enabled from another common line. In all cases the outputs are placed in the TRI-STATE condition by applying a high logic level to the enable pins. These devices represent octal, low power-Schottky versions of the very popular DM70/8095, 96, 97, and 98 TRI-STATE hex buffers.

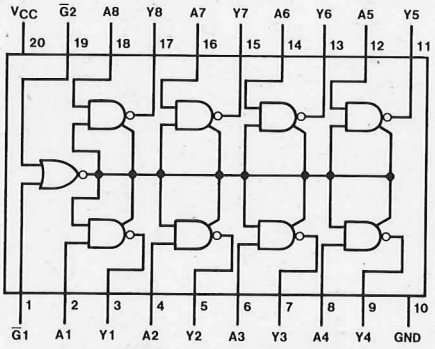
## Features

- Octal versions of popular DM8095, 8096, 8097, 8098
- Typical power dissipation
  - LS95A, LS97A 80 mW
  - LS96A, LS98A 65 mW
- Typical propagation delay
  - LS95A, LS97A 15 ns
  - LS96A, LS98A 10 ns
- Low power-Schottky, TRI-STATE technology

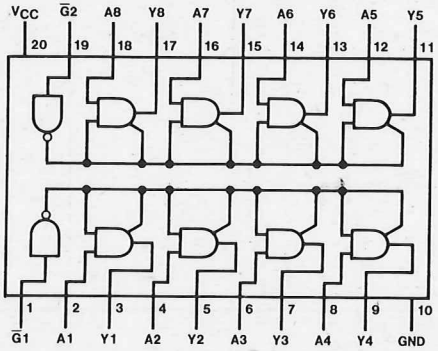
## Connection Diagrams



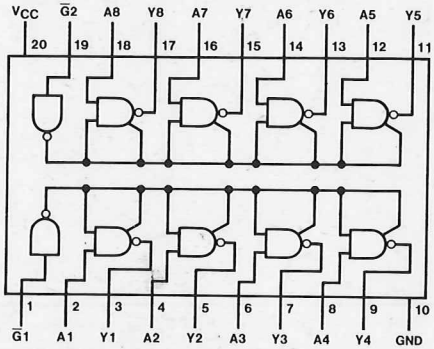

71LS95A (J,W)/81LS95A (N)




71LS96A (J,W)/81LS96A (N)




71LS97A (J,W)/81LS97A (N)




71LS98A (J,W)/81LS98A (N)

## Truth Tables

LS95A

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{G}1$ | $\overline{G}2$ | A | Y |
| H | X | X | Z |
| X | H | X | Z |
| L | L | H | H |
| L | L | L | L |

LS96A

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{G}1$ | $\overline{G}2$ | A | Y |
| H | X | X | Z |
| X | H | X | Z |
| L | L | H | L |
| L | L | L | H |

LS97A

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{G}$ | A | Y |
| H | X | Z |
| L | H | H |
| L | L | L |

LS98A

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{G}$ | A | Y |
| H | X | Z |
| L | H | L |
| L | L | H |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM71/81 LS95A, LS96A, LS97A, LS98A Min | Typ (1) | Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | DM71 | | | −2.6 | mA |
| | | | | | DM81 | | | −5.2 | |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | DM71 | 2.5 | | | V |
| | | | | | DM81 | 2.7 | | | |
| $I_{OL}$ | Low Level Output Current | | | | DM71 | | | 12 | mA |
| | | | | | DM81 | | | 24 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = Max | | DM71 | | | 0.4 | V |
| | | | | | DM81 | | | 0.5 | |
| $I_{OZ}$ | Off-State (High-Impedance State) Output Current | | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $V_O$ = 0.4 V | | | | −20 | μA |
| | | | | $V_O$ = 2.4 V | | | | 20 | |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max, $V_I$ = 7 V | | | | | 0.1 | mA |
| $I_{IH}$ | High Level Input Current | | $V_{CC}$ = Max, $V_I$ = 2.7 V | | | | | 20 | μA |
| $I_{IL}$ | Low Level Input Current | A Input | $V_{CC}$ = Max | Both $\overline{G}$ Inputs at 2 V | $V_I$ = 0.5 V | | | −20 | μA |
| | | | | Both $\overline{G}$ Inputs at 0.4 V | $V_I$ = 0.4 V | | | −50 | |
| | | $\overline{G}$ Input | | | $V_I$ = 0.4 V | | | −50 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max | | 95,97 | | 16 | 26 | mA |
| | | | | | 96,98 | | 13 | 21 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | DM71/81 | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | LS95A, LS97A | | | LS96A, LS98A | | | |
| | | | Min | Typ | Max | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $C_L$ = 45 pF, $R_L$ = 667 Ω | | 10 | 16 | | 6 | 10 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | 19 | 28 | | 13 | 17 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | | | 11 | 25 | | 10 | 15 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | 20 | 30 | | 23 | 35 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | $C_L$ = 5 pF, $R_L$ = 667 Ω | | 13 | 20 | | 13 | 20 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | | 19 | 27 | | 18 | 27 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $C_L$ = 150 pF, $R_L$ = 667 Ω | | 15 | 25 | | 11 | 16 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | 25 | 40 | | 19 | 30 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | | | 20 | 30 | | 20 | 30 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | 28 | 42 | | 30 | 45 | ns |

# 4-Bit Magnitude Comparators

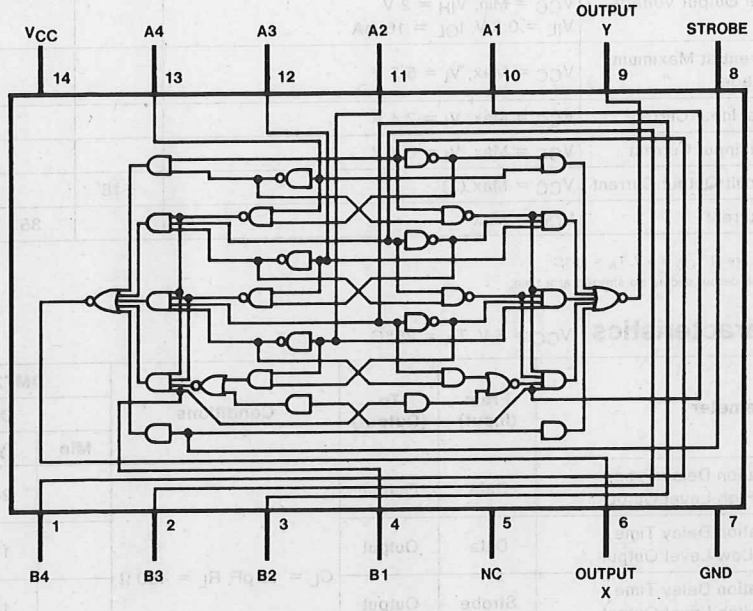
## General Description

These devices compare two binary words of four bits in length; and the outputs indicate 1) word A > word B, 2) word A < word B, or 3) word A = word B. A strobe input overrides all other inputs, and when taken to a high logic level, places both outputs in the low state. Comparison of words longer than four bits each may be accomplished through the use of additional DM7200/DM8200 devices.

## Features

- Typical power dissipation 175 mW
- Typical propagation delay 20 ns

## Connection Diagram




A4, B4 are most significant bits.

7200 (J,W); 8200 (N),

## Truth Table

| Inputs | | Outputs | |
|---|---|---|---|
| Condition | Strobe | X | Y |
| Don't Care | H | L | L |
| A > B | L | H | L |
| A < B | L | L | H |
| A = B | L | H | H |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | DM72/82 00 | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OH}$ = −400 μA | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | 80 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | −3.2 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | −18 | | −55 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | 35 | 53 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Conditions | DM72/82 00 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Output | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 24 | 40 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Data | Output | | | 17 | 30 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Strobe | Output | | | 15 | 27 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Strobe | Output | | | 8 | 18 | ns |
| $t_{SETUP}$ | Setup Time | | | | 10 | 0 | | ns |
| $t_{HOLD}$ | Hold Time | | | | 0 | −10 | | ns |

# TRI-STATE® Data Selectors/Multiplexers

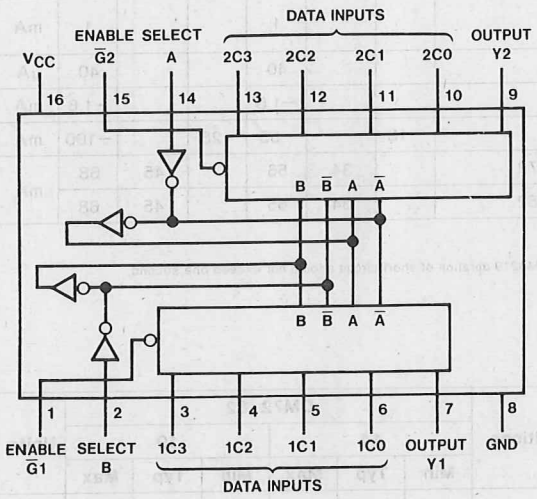
## General Description

These devices are the TRI-STATE versions of the very popular DM54153 (DM7214) and DM54150 (DM7219) data selectors/multiplexers. They contain full on-chip decoding to select the desired data input. The DM7214/8214 is a dual, four-line multiplexer, while the DM7219/ 8219 selects one of sixteen input data lines, depending upon the binary number applied to the select inputs. The DM7214/8214 has common select lines, which therefore select the same input line of both multiplexers. However, the two outputs can be individually controlled by means of the separate enable lines; which, when taken to a high logic level, places the output in the high-impedance TRI-STATE condition. The data at the output of the DM7214/8214 is true, whereas the DM7219/8219 is inverted.

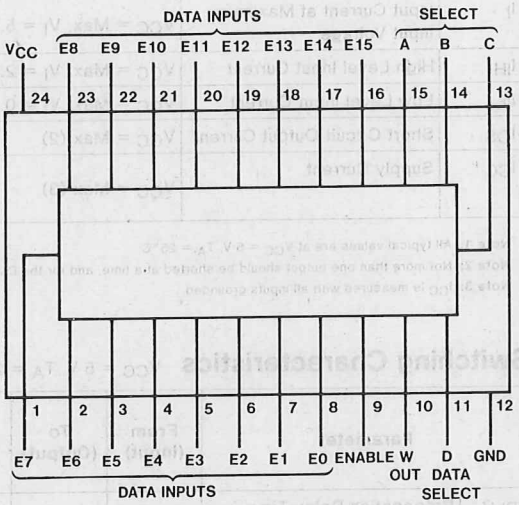
## Features

- TRI-STATE pin equivalents to popular 54/74 TTL devices
  - DM7214/8214 — 54153/74153
  - DM7219/8219 — 54150/74150
- Typical propagation delay
  - DM7214/8214 13.5 ns
  - DM7219/8219 11 ns
- Typical power dissipation
  - DM7214/8214 170 mW
  - DM7219/8219 225 mW
- Strobe/enable override

## Connection Diagrams




7214 (J,W); 8214 (N)




7219 (J,F); 8219 (N)

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM72/82 | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 14 | | | 19 | | | |
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | High Level Output Current | | DM72 | | | −2.0 | | | −2.0 | mA |
| | | | DM82 | | | −5.2 | | | −5.2 | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | | 0.4 | | | 0.4 | V |
| $I_{O(OFF)}$ | Off-State (High-Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $V_O$ = 0.4 V | | | −40 | | | −40 | μA |
| | | | $V_O$ = 2.4 V | | | 40 | | | 40 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −1.6 | | | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −18 | | −55 | −28 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | DM72 | | 34 | 56 | | 45 | 68 | mA |
| | | | DM82 | | 34 | 65 | | 45 | 68 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time, and for the DM7219/DM8219 duration of short circuit should not exceed one second.
**Note 3:** $I_{CC}$ is measured with all inputs grounded.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Conditions | DM72/82 | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 14 | | | 19 | | | |
| | | | | | Min | Typ | Max | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Output | $C_L$ = 50 pF, $R_L$ = 400 Ω | | 15 | 23 | | 13 | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Data | Output | | | 12 | 18 | | 9 | 14 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Select | Output | | | 20 | 34 | | 21 | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Select | Output | | | 20 | 34 | | 22 | 33 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | Enable | Output | | | 12 | 18 | | 15 | 23 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | Enable | Output | | | 14 | 21 | | 17 | 27 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | Enable | Output | $C_L$ = 5 pF, $R_L$ = 400 Ω | | 5 | 10 | | 5 | 10 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | Enable | Output | | | 15 | 23 | | 21 | 30 | ns |

## Truth Tables

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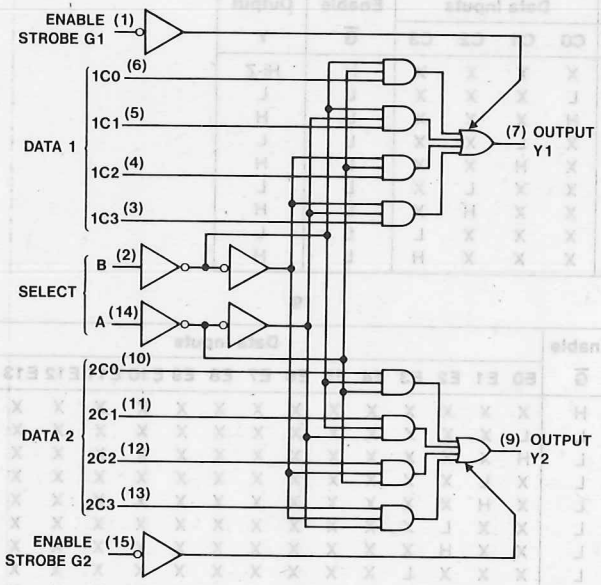
| Select Inputs | | Data Inputs | | | | Enable | Output |
|---|---|---|---|---|---|---|---|
| B | A | C0 | C1 | C2 | C3 | $\overline{G}$ | Y |
| X | X | X | X | X | X | H | Hi-Z |
| L | L | L | X | X | X | L | L |
| L | L | H | X | X | X | L | H |
| L | H | X | L | X | X | L | L |
| L | H | X | H | X | X | L | H |
| H | L | X | X | L | X | L | L |
| H | L | X | X | H | X | L | H |
| H | H | X | X | X | L | L | L |
| H | H | X | X | X | H | L | H |

19

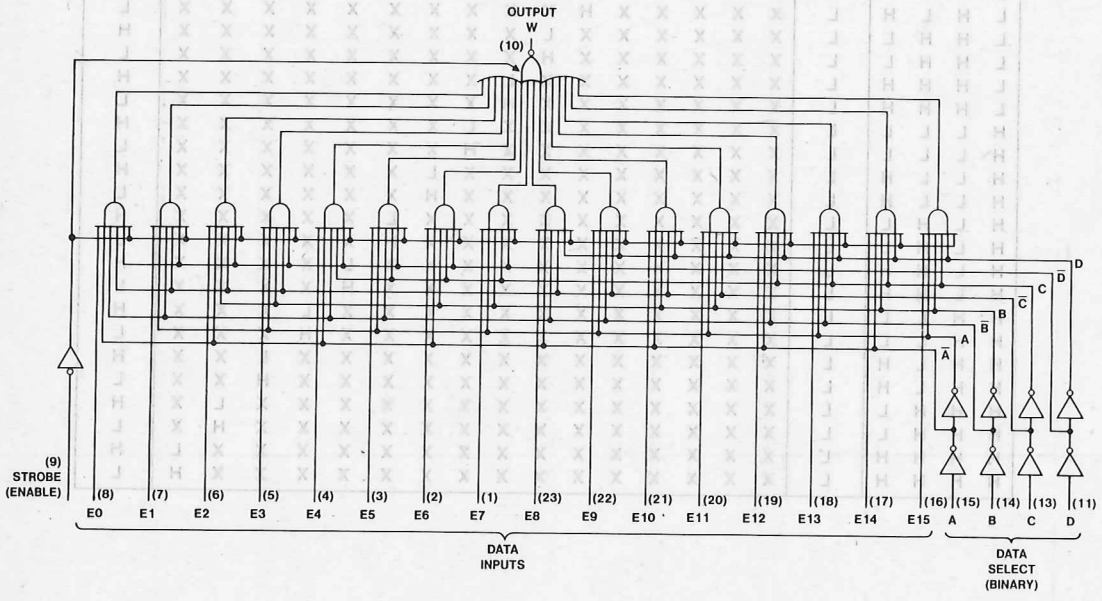
| Select | | | | Enable | Data Inputs | | | | | | | | | | | | | | Output |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D | C | B | A | $\overline{G}$ | E0 | E1 | E2 | E3 | E4 | E5 | E6 | E7 | E8 | E9 | E10 | E11 | E12 | E13 | E14 | E15 | Y |
| X | X | X | X | H | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | Hi-Z |
| L | L | L | L | L | L | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | H |
| L | L | L | L | L | H | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | L |
| L | L | L | H | L | X | L | X | X | X | X | X | X | X | X | X | X | X | X | X | X | H |
| L | L | L | H | L | X | H | X | X | X | X | X | X | X | X | X | X | X | X | X | X | L |
| L | L | H | L | L | X | X | L | X | X | X | X | X | X | X | X | X | X | X | X | X | H |
| L | L | H | L | L | X | X | H | X | X | X | X | X | X | X | X | X | X | X | X | X | L |
| L | L | H | H | L | X | X | X | L | X | X | X | X | X | X | X | X | X | X | X | X | H |
| L | L | H | H | L | X | X | X | H | X | X | X | X | X | X | X | X | X | X | X | X | L |
| L | H | L | L | L | X | X | X | X | L | X | X | X | X | X | X | X | X | X | X | X | H |
| L | H | L | L | L | X | X | X | X | H | X | X | X | X | X | X | X | X | X | X | X | L |
| L | H | L | H | L | X | X | X | X | X | L | X | X | X | X | X | X | X | X | X | X | H |
| L | H | L | H | L | X | X | X | X | X | H | X | X | X | X | X | X | X | X | X | X | L |
| L | H | H | L | L | X | X | X | X | X | X | L | X | X | X | X | X | X | X | X | X | H |
| L | H | H | L | L | X | X | X | X | X | X | H | X | X | X | X | X | X | X | X | X | L |
| L | H | H | H | L | X | X | X | X | X | X | X | L | X | X | X | X | X | X | X | X | H |
| L | H | H | H | L | X | X | X | X | X | X | X | H | X | X | X | X | X | X | X | X | L |
| H | L | L | L | L | X | X | X | X | X | X | X | X | L | X | X | X | X | X | X | X | H |
| H | L | L | L | L | X | X | X | X | X | X | X | X | H | X | X | X | X | X | X | X | L |
| H | L | L | H | L | X | X | X | X | X | X | X | X | X | L | X | X | X | X | X | X | H |
| H | L | L | H | L | X | X | X | X | X | X | X | X | X | H | X | X | X | X | X | X | L |
| H | L | H | L | L | X | X | X | X | X | X | X | X | X | X | L | X | X | X | X | X | H |
| H | L | H | L | L | X | X | X | X | X | X | X | X | X | X | H | X | X | X | X | X | L |
| H | L | H | H | L | X | X | X | X | X | X | X | X | X | X | X | L | X | X | X | X | H |
| H | L | H | H | L | X | X | X | X | X | X | X | X | X | X | X | H | X | X | X | X | L |
| H | H | L | L | L | X | X | X | X | X | X | X | X | X | X | X | X | L | X | X | X | H |
| H | H | L | L | L | X | X | X | X | X | X | X | X | X | X | X | X | H | X | X | X | L |
| H | H | L | H | L | X | X | X | X | X | X | X | X | X | X | X | X | X | L | X | X | H |
| H | H | L | H | L | X | X | X | X | X | X | X | X | X | X | X | X | X | H | X | X | L |
| H | H | H | L | L | X | X | X | X | X | X | X | X | X | X | X | X | X | X | L | X | H |
| H | H | H | L | L | X | X | X | X | X | X | X | X | X | X | X | X | X | X | H | X | L |
| H | H | H | H | L | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | L | H |
| H | H | H | H | L | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | H | L |

## Logic Diagrams

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# 9-Bit Parity Generators/Checkers

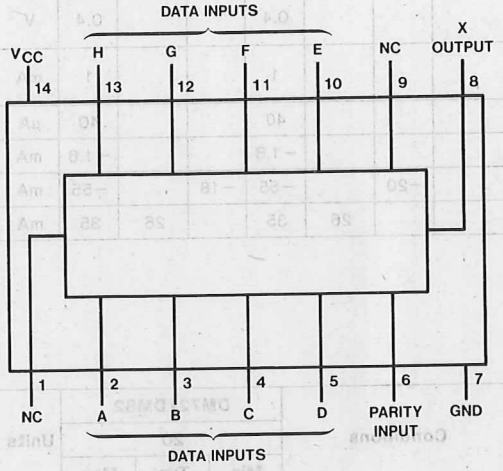
## General Description

These circuits can be used both to check for parity and to generate a parity bit. When the generation of a parity bit is desired, the eight data inputs are connected to the transmission lines. If a low logic level is then connected to the parity input, the circuit will generate odd parity. The succeeding parity checker will acknowledge an odd number of "1's" (odd parity) with a low logic level on its output. If a high logic level is connected to the parity input of the first parity generator, the parity checker will acknowledge even parity with a high logic level on its output, although the output of the parity generator will be low.

## Features

- Typical propagation delay 34 ns
- Typical power dissipation 130 mW

## Connection Diagram




7220 (J,W)/8220 (N)

## Truth Table

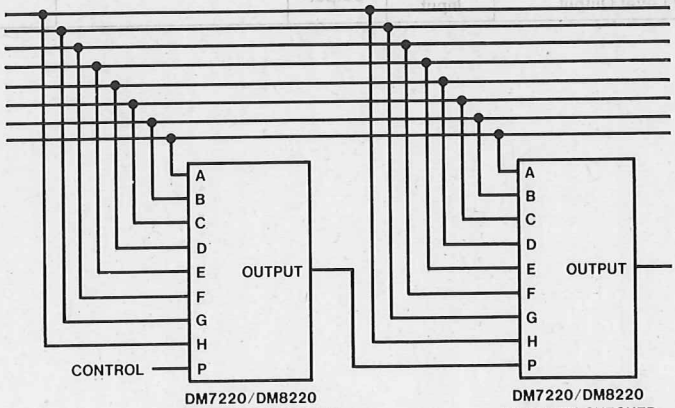
| Parity Input | Output* | Inputs A Thru H |
|---|---|---|
| H | L | Even number of inputs are High |
| L | L | Odd number of inputs are High |

*Single device

## Typical Application

If the control line is a logical "0" the parity generator will generate odd parity. The parity checker will acknowledge the presence of an odd number of "1's" (odd parity) with a logical "0" on its output.

If the control line is a logical "1" the parity generator will generate even parity. The parity checker will acknowledge the presence of an even number of "1's" (even parity) with a logical "1" on its output.



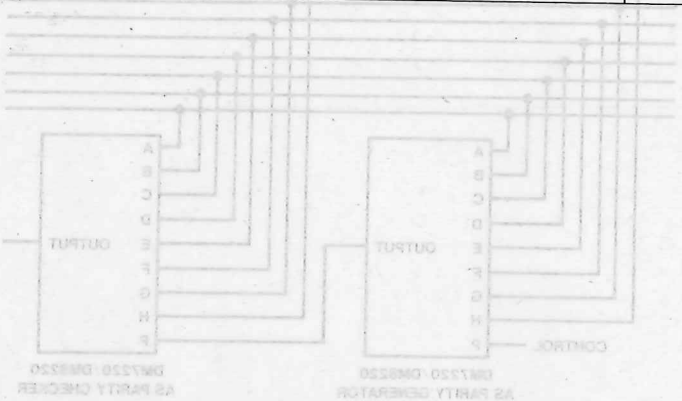
## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | DM72 | | | DM82 | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 20 | | | 20 | | | |
| | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA, $T_A$ = 25°C | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | −400 | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −400 μA | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | −1.6 | | | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | −20 | | −55 | −18 | | −55 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | 26 | 35 | | 26 | 35 | mA |

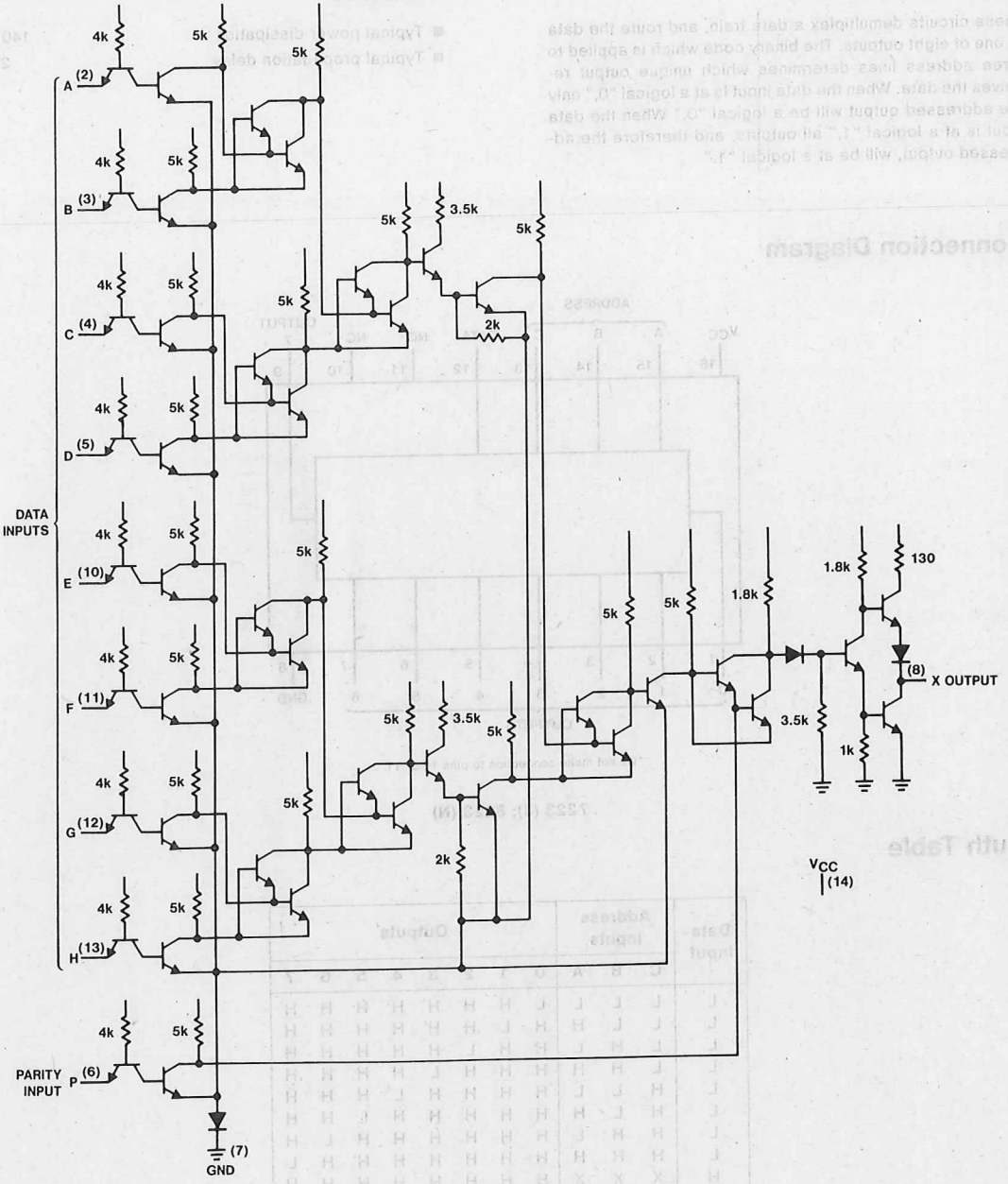
**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From | To | Conditions | DM72/DM82 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | | 20 | | | |
| | | | | | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data Inputs | Output | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 36 | 58 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Data Inputs | Output | | | 32 | 52 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Parity Input | Output | | | 21 | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Parity Input | Output | | | 14 | 25 | ns |



## Schematic Diagram



# DM72/DM8223

## 1-Line to 8-Line Demultiplexers

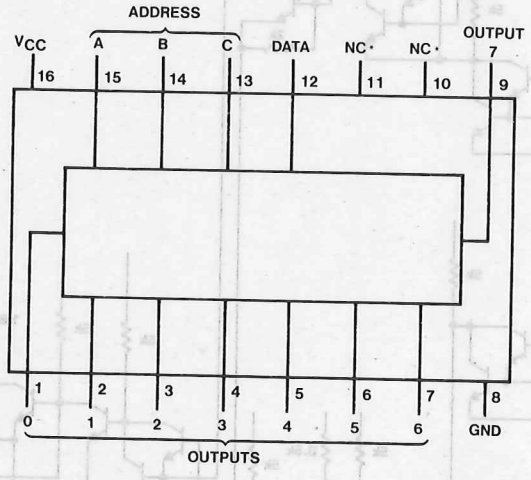
## General Description

These circuits demultiplex a data train, and route the data to one of eight outputs. The binary code which is applied to three address lines determines which unique output receives the data. When the data input is at a logical "0," only the addressed output will be a logical "0." When the data input is at a logical "1," all outputs, and therefore the addressed output, will be at a logical "1."

## Features

- Typical power dissipation 140 mW
- Typical propagation delay 25 ns

## Connection Diagram




*Do not make connection to pins 10 or 11.

7223 (J); 8223 (N)

## Truth Table

| Data Input | Address Inputs | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| L | L | L | L | L | H | H | H | H | H | H | H |
| L | L | L | H | H | L | H | H | H | H | H | H |
| L | L | H | L | H | H | L | H | H | H | H | H |
| L | L | H | H | H | H | H | L | H | H | H | H |
| L | H | L | L | H | H | H | H | L | H | H | H |
| L | H | L | H | H | H | H | H | H | L | H | H |
| L | H | H | L | H | H | H | H | H | H | L | H |
| L | H | H | H | H | H | H | H | H | H | H | L |
| H | X | X | X | H | H | H | H | H | H | H | H |

X = Don't Care

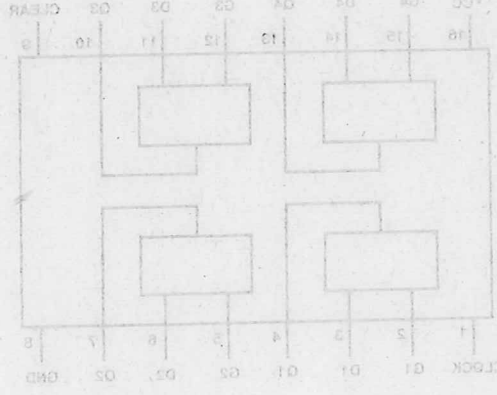
## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | DM72 | | | DM82 | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 23 | | | 23 | | | |
| | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | −400 | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OH}$ = −400 μA | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | −1.6 | | | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | −20 | | −55 | −18 | | −57 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | 28 | 41 | | 28 | 41 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | DM72/82 | | | Units |
|---|---|---|---|---|---|---|
| | | | 23 | | | |
| | | | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $C_L$ = 15 pF,<br>$R_L$ = 400 Ω | | 26 | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | 24 | 35 | ns |



# Dual/Quad Gated Flip-Flops

## General Description

The DM7511/8511 or the low-power versions DM75L11/85L11, are dual, gated, D-type flip-flops. Each flip-flop has its own clock, clear line, and two gated inputs. Both gate inputs must be low to enable data transfer to the output.

The DM7512/8512, and DM75L12/85L12 are dual, gated flip-flops which can operate in either a J-K mode, or as D-type flip-flops. They have a common clock and common, asynchronous clear, but have separate mode inputs such that one side can operate as J-K while the other side operates as a D-type flip-flop.

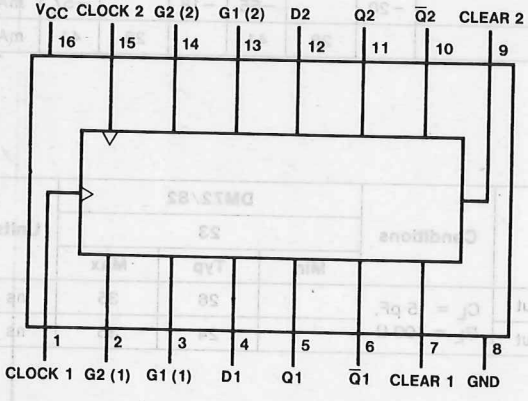
The DM7613/8613, and DM76L13/86L13 are quad, gated, D-type flip-flops with common clock, common clear, and gated input. When a high logic level is applied to the gated input, data entry to the flip-flop is inhibited.

## Features

- Positive-edge triggered
- Do-nothing state
- Buffered inputs

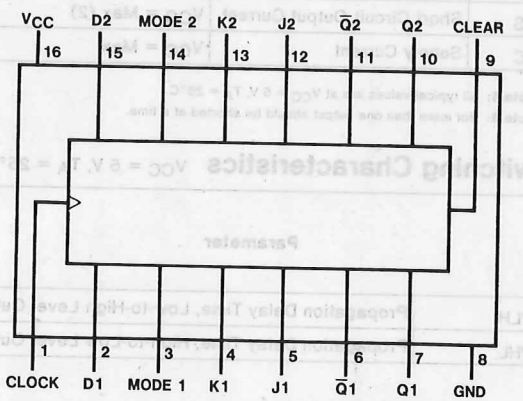
| Type | Typical Toggle Rate | Typical Power Dissipation |
|---|---|---|
| DM7511/8511 | 45 MHz | 210 mW |
| DM75L11/85L11 | 9 MHz | 17.5 mW |
| DM7512/8512 | 28 MHz | 220 mW |
| DM75L12/85L12 | 10 MHz | 16.0 mW |
| DM7613/8613 | 30 MHz | 290 mW |
| DM76L13/86L13 | 7 MHz | 28.5 mW |

## Connection Diagrams



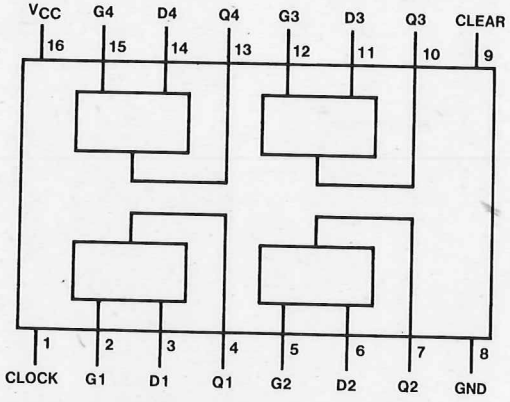

7511 (J,W)
75L11 (J,W)

8511 (N)
85L11 (N)




7512 (J,W)
75L12 (J,W)

8512 (N)
85L12 (N)




7613 (J,W)
76L13 (J,W)

8613 (N)
86L13 (N)

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM75/85 11, 12 | | | DM76/86 13 | | | DM75L/85L11, 12 DM76L/86L13 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | | | 0.8 | | | 0.7 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | | | N/A | V |
| $I_{OH}$ | High Level Output Current | | | | | −800 | | | −800 | | | −200 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = Max, $I_{OH}$ = Max | | 2.4 | | | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | Military | | | 16 | | | 16 | | | 2.0 | mA |
| | | | Commercial | | | 16 | | | 16 | | | 3.6 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = Max, $I_{OL}$ = Max | Military | | | 0.4 | | | 0.4 | | | 0.3 | V |
| | | | Commercial | | | 0.4 | | | 0.4 | | | 0.4 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1.0 | | | 1.0 | | | 0.1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | | | 40 | | | 10 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | | | | | −0.18 | mA |
| | | | $V_I$ = 0.4 V | | | −1.6 | | | −1.6 | | | | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −18 | | −55 | −18 | | −55 | −3 | −9 | −15 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | 11, L11 | | 42 | 55 | | | | | 3.5 | 4.9 | mA |
| | | | 12, L12 | | 44 | 57 | | | | | 3.2 | 4.5 | |
| | | | 13, L13 | | | | | 58 | 76 | | 5.7 | 7.9 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.
**Note 3:** Supply current is measured with clear/clock at 3 V, all other inputs at 0 V.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C.

| Parameter | | | From | To | Conditions | DM75/85 11, L11 | | | DM75/85 12, L12 | | | DM76/86 13, L13 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | | | $C_L$ = 15 pF, $R_L$ = 400 Ω (Standard) | 30 | 45 | | 20 | 28 | | 20 | 30 | | MHz |
| | | | | | | 6 | 9 | | 6 | 10 | | 5 | 7 | | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock | Q | | | 14 | 20 | | 21 | 35 | | 17 | 24 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clock | Q | | | 55 | 95 | | 35 | 70 | | 41 | 60 | |
| | | | | | $C_L$ = 50 pF, $R_L$ = 4 kΩ (Low Power) | | 19 | 30 | | 26 | 40 | | 22 | 33 | ns |
| | | | | | | | 75 | 125 | | 60 | 120 | | 70 | 100 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clear | $\overline{Q}$ | | | 14 | 20 | | 22 | 35 | | N/A | | ns |
| | | | | | | | 55 | 95 | | 32 | 65 | | N/A | | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Output | | Clear | Q | | | 19 | 30 | | 26 | 40 | | 21 | 31 | ns |
| | | | | | | | 75 | 125 | | 57 | 114 | | 68 | 100 | |
| $t_{W(CLOCK)}$ | Width of Clock Pulse | | | | | 20 | 11 | | 25 | 15 | | 24 | 16 | | ns |
| | | | | | | 100 | 30 | | 100 | 30 | | 100 | 50 | | |
| $t_{W(CLEAR}$ | Width of Clear Pulse | | | | | 20 | 10 | | 25 | 13 | | 27 | 18 | | ns |
| | | | | | | 100 | 30 | | 100 | 30 | | 100 | 50 | | |
| $t_{SETUP}$ | Setup Time | J, D Inputs | | | | 15 | 9 | | 15 | 9 | | 24 | 16 | | ns |
| | | | | | | 80 | 40 | | 110 | 55 | | 100 | 55 | | |
| | | Mode Inputs | | | | | N/A | | 30 | 20 | | | N/A | | ns |
| | | | | | | | N/A | | 150 | 85 | | | N/A | | |
| | | K Inputs | | | | | N/A | | 20 | 13 | | | N/A | | ns |
| | | | | | | | N/A | | 150 | 80 | | | N/A | | |
| | | G1 or G2 Inputs | | | | 30 | 21 | | | N/A | | 30 | 21 | | ns |
| | | | | | | 120 | 60 | | | N/A | | 150 | 85 | | |
| $t_{HOLD}$ | Hold Time | All | | | | 0 | | | 0 | | | 0 | | | ns |
| | | | | | | 0 | | | 0 | | | 0 | | | |

## Truth Tables

11, L11

| D | G1 | G2 | CLR | $Q_{n+1}$ | $\overline{Q}_{n+1}$ |
|---|---|---|---|---|---|
| L | L | L | L | L | H |
| H | L | L | L | H | L |
| X | H | X | L | $Q_n$ | $\overline{Q}_n$ |
| X | X | H | L | $Q_n$ | $\overline{Q}_n$ |
| X | X | X | H | L | H* |

12, L12

| J | K | M | Clear | $Q_{n+1}$ |
|---|---|---|---|---|
| L | L | H | L | $Q_n$ |
| H | L | H | L | H |
| L | H | H | L | L |
| H | H | H | L | $\overline{Q}_n$ |
| X | X | L | L | D |
| X | X | X | H | L* |

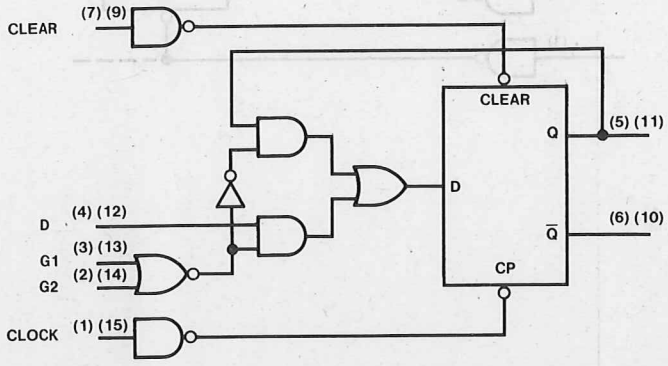
13, L13

| D | G | CLR | $Q_{n+1}$ |
|---|---|---|---|
| H | L | L | H |
| L | L | L | L |
| X | H | L | $Q_n$ |
| X | X | H | L* |

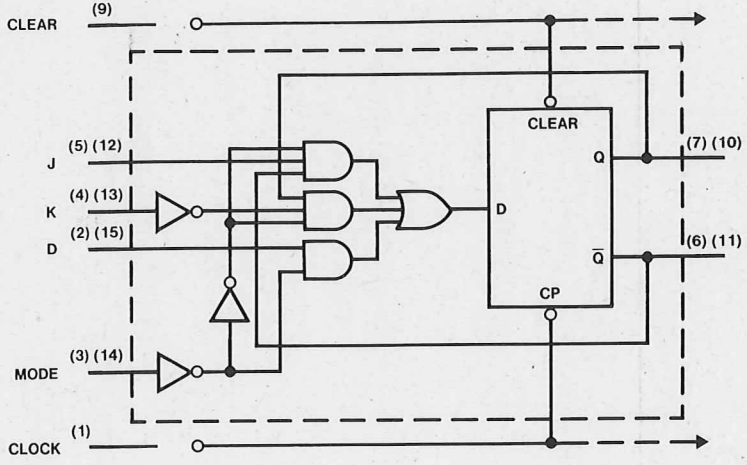
*Asynchronous Transition
X = Don't Care

## Logic Diagrams

11, L11

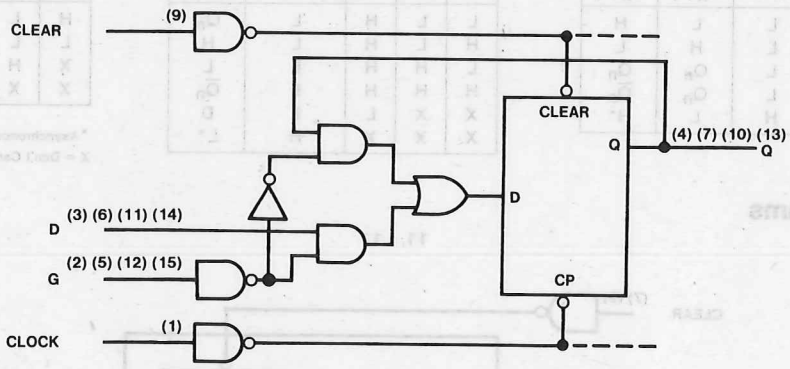



12, L12



## Logic Diagrams (Continued)

13, L13



# Modulo-N Dividers

## General Description

Although extremely versatile in a number of applications, the primary uses of these circuits are in two areas:

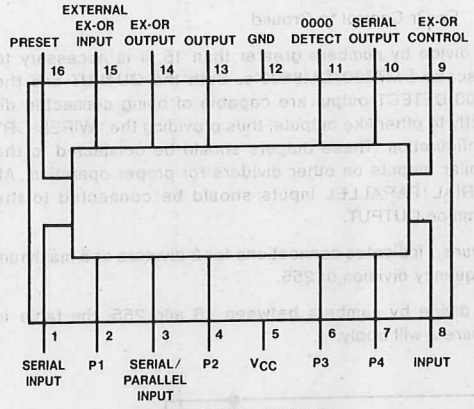
1. **MODULO-N DIVIDER**
   A single DM7520/DM8520 can be programmed without external components to divide by any number from 2 to 15. Cascading of these dividers will provide division by any number from 2 to very large numbers.
2. **SHIFT REGISTER**
   Since the basic organization of the logic is that of a serial shift register, the device may be used where four-bit parallel-in-serial-out shifting is required.

(continued)

## Features

- Fully programmable divider—any number from 2 to ∞
- Also functions as a four-bit parallel shift register
- Typical propagation delay 36 ns
- Typical power dissipation 250 mW

## Connection Diagram



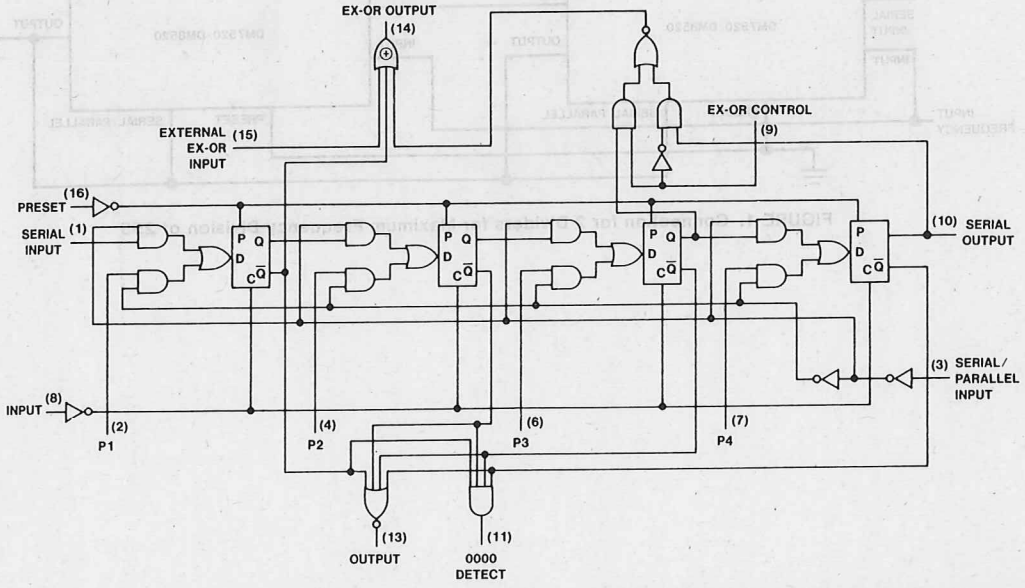

**7520 (J,W); 8520 (N)**

## Truth Table

**Table for Division By N**

| Setting | | | | ÷ BY |
|---|---|---|---|---|
| P1 | P2 | P3 | P4 | |
| H | H | H | L | 2 |
| H | H | L | L | 3 |
| H | L | L | L | 4 |
| L | L | L | H | 5 |
| L | L | H | L | 6 |
| L | H | L | L | 7 |
| H | L | L | H | 8 |
| L | L | H | H | 9 |
| L | H | H | L | 10 |
| H | H | L | H | 11 |
| H | L | H | L | 12 |
| L | H | L | H | 13 |
| H | L | H | H | 14 |
| L | H | H | H | 15 |

## Logic Diagram



## General Description (Continued)

### THEORY OF OPERATION

The basic operation of the DM7520/DM8520 is derived from the fact that when several outputs of a shift register are EXCLUSIVE OR'ed and the result fed back to the register's input, a unique progression of stable states results on the outputs of the flip-flops. Depending upon which outputs are EXCLUSIVE OR'ed, the number of different states can be varied. Even if optimum gating is provided the most states which can be obtained is $2^n - 1$, where n is equal to the number of flip-flops in the register. The all-zero state is precluded; and, therefore, the maximum number of states is always one less than the theoretical maximum number. Since the DM7520/DM8520 contains four flip-flops, its maximum number of states is 15. Because the 1111 state occurs only once during a 15-state sequence this state is detected, and its output becomes the output of the divider.

To obtain frequency division by numbers other than the maximum, it is necessary to cause the register to "jump" immediately from its initial 1111 to the state which it would normally reach in 16 m (m = desired frequency division) pulses. For example, to divide by eleven it would be necessary to jump to the fifth state and then simply allow the register to normally progress forward to its original state. The output of the divider is also used as a control pulse. Since the 1111 state is detected and since the "jump-state" information is of interest only at the time that this state is reached, the OUTPUT is used to gate the parallel inputs, through the SERIAL/PARALLEL input, so that it recognizes this "jump-state" information only at this time. Subsequently as the states change, the parallel input information is locked from the divider.

Should the divider ever be accidentally set in the forbidden 0000 state, an output is provided to detect this state. If this output is in turn fed into the EXTERNAL EX-OR input, a 1 will be forced into the register at the next clock pulse, thus clearing the unallowed state.

A PRESET input is provided which when taken to a logical "1" level overrides all other inputs and sets the register to the 1111 state.

To summarize, the following connections should be made for operation of a single DM7520/DM8520.

Ex-Or Output to Serial Input
0000 Detect to External Ex-Or Input
Output to Serial/Parallel Input
Preset to Ground
Ex-Or Control to Ground

To divide by numbers greater than 15, it is necessary to cascade DM7520/DM8520's. Both the OUTPUT and the 0000 DETECT output are capable of being connected directly to other like outputs, thus providing the "WIRED-OR" configuration. These outputs should be connected to the similar outputs on other dividers for proper operation. All SERIAL/PARALLEL inputs should be connected to the common OUTPUT.

*Figure 1* indicates connections for 2 dividers or a maximum frequency division of 255.

To divide by numbers between 16 and 255, the table in *Figure 2* will apply.

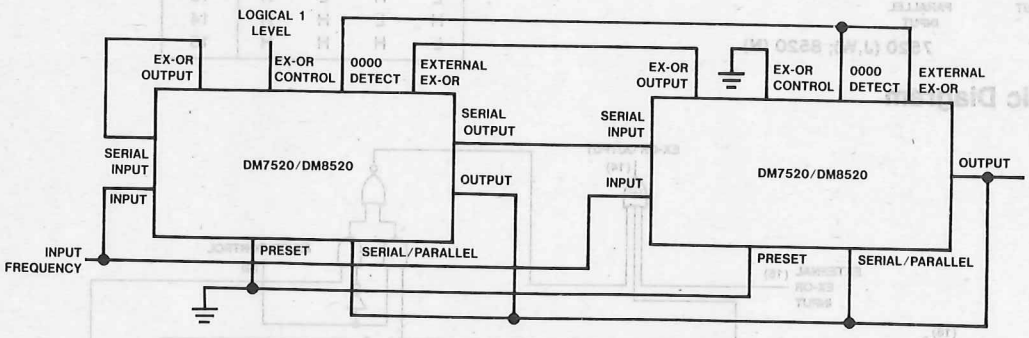



**FIGURE 1. Connection for 2 Dividers for Maximum Frequency Division of 255**

THEORY OF OPERATION (Continued)

| Setting | | | | | | | | | Setting | | | | | | | | | Setting | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Divider 1 | | | | Divider 2 | | | | By | Divider 1 | | | | Divider 2 | | | | By | Divider 1 | | | | Divider 2 | | | | By |
| P1 | P2 | P3 | P4 | P1 | P2 | P3 | P4 | | P1 | P2 | P3 | P4 | P1 | P2 | P3 | P4 | | P1 | P2 | P3 | P4 | P1 | P2 | P3 | P4 | |
| L | H | H | H | H | H | H | H | 255 | H | L | L | L | H | L | L | H | 195 | L | L | H | H | H | L | L | H | 135 |
| H | L | H | H | H | H | H | H | 254 | H | H | L | L | L | H | L | L | 194 | H | L | L | H | H | H | L | L | 134 |
| L | H | L | H | H | H | H | H | 253 | H | H | H | L | L | L | H | L | 193 | L | H | L | L | H | H | H | L | 133 |
| L | L | H | L | H | H | H | H | 252 | L | H | H | H | L | L | L | H | 192 | H | L | H | L | L | H | H | H | 132 |
| H | L | L | H | L | H | H | H | 251 | L | L | H | H | H | L | L | L | 191 | H | H | L | H | L | L | H | H | 131 |
| L | H | L | L | H | L | H | H | 250 | L | L | L | H | H | H | L | L | 190 | L | H | H | L | H | L | L | H | 130 |
| L | L | H | L | L | H | L | H | 249 | H | L | L | L | H | H | H | L | 189 | H | L | H | H | L | H | L | L | 129 |
| L | L | L | H | L | L | H | L | 248 | L | H | L | L | L | H | H | H | 188 | L | H | L | H | H | L | H | L | 128 |
| L | L | L | L | H | L | L | H | 247 | H | L | H | L | L | L | H | H | 187 | H | L | H | L | H | H | L | H | 127 |
| L | L | L | L | L | H | L | L | 246 | H | H | L | H | L | L | L | H | 186 | L | H | L | H | L | H | H | L | 126 |
| L | L | L | L | L | L | H | L | 245 | L | H | H | L | H | L | L | L | 185 | L | L | H | L. | H | L | H | H | 125 |
| L | L | L | L | L | L | L | H | 244 | L | L | H | H | L | H | L | L | 184 | H | L | L | H | L | H | L | H | 124 |
| H | L | L | L | L | L | L | L | 243 | H | L | L | H | H | L | H | L | 183 | L | H | L | L | H | L | H | L | 123 |
| H | H | L | L | L | L | L | L | 242 | L | H | L | L | H | H | L | H | 182 | H | L | H | L | L | H | L | H | 122 |
| H | H | H | L | L | L | L | L | 241 | L | L | H | L | L | H | H | L | 181 | H | H | L | H | L | L | H | L | 121 |
| L | H | H | H | L | L | L | L | 240 | H | L | L | H | L | L | H | H | 180 | H | H | H | L | H | L | L | H | 120 |
| H | L | H | H | H | L | L | L | 239 | L | H | L | L | H | L | L | H | 179 | L | H | H | H | L | H | L | L | 119 |
| H | H | L | H | H | H | L | L | 238 | L | L | H | L | L | H | L | L | 178 | H | L | H | H | H | L | H | L | 118 |
| L | H | H | L | H | H | H | L | 237 | H | L | L | H | L | L | H | L | 177 | H | H | L | H | H | H | L | H | 117 |
| L | L | H | H | L | H | H | H | 236 | H | H | L | L | H | L | L | H | 176 | H | H | H | L | H | H | H | L | 116 |
| L | L | L | H | H | L | H | H | 235 | H | H | H | L | L | H | L | L | 175 | H | H | H | H | L | H | H | H | 115 |
| L | L | L | L | H | H | L | H | 234 | L | H | H | H | L | L | H | L | 174 | H | H | H | H | H | L | H | H | 114 |
| L | L | L | L | L | H | H | L | 233 | H | L | H | H | H | L | L | H | 173 | L | H | H | H | H | H | L | H | 113 |
| L | L | L | L | L | L | H | H | 232 | L | H | L | H | H | H | L | L | 172 | H | L | H | H | H | H | H | L | 112 |
| H | L | L | L | L | L | L | H | 231 | H | L | H | L | H | H | H | L | 171 | H | H | L | H | H | H | H | H | 111 |
| L | H | L | L | L | L | L | L | 230 | H | H | L | H | L | H | H | H | 170 | H | H | H | L | H | H | H | H | 110 |
| L | L | H | L | L | L | L | L | 229 | L | H | H | L | H | L | H | H | 169 | L | H | H | H | L | H | H | H | 109 |
| H | L | L | H | L | L | L | L | 228 | H | L | H | H | L | H | L | H | 168 | L | L | H | H | H | L | H | H | 108 |
| H | H | L | L | H | L | L | L | 227 | H | H | L | H | H | L | H | L | 167 | H | L | L | H | H | H | L | H | 107 |
| L | H | H | L | L | H | L | L | 226 | L | H | H | L | H | H | L | H | 166 | H | H | L | L | H | H | H | L | 106 |
| H | L | H | H | L | L | H | L | 225 | H | L | H | H | L | H | H | L | 165 | L | H | H | L | L | H | H | H | 105 |
| L | H | L | H | H | L | L | H | 224 | L | H | L | H | H | L | H | H | 164 | L | L | H | H | L | L | H | H | 104 |
| L | L | H | L | H | H | L | L | 223 | L | L | H | L | H | H | L | H | 163 | L | L | L | H | H | L | L | H | 103 |
| L | L | L | H | L | H | H | L | 222 | H | L | L | H | L | H | H | L | 162 | L | L | L | L | H | H | L | L | 102 |
| L | L | L | L | H | L | H | H | 221 | H | H | L | L | H | L | H | H | 161 | H | L | L | L | L | H | H | L | 101 |
| L | L | L | L | L | H | L | H | 220 | H | H | H | L | L | H | L | H | 160 | H | H | L | L | L | L | H | H | 100 |
| H | L | L | L | L | L | H | L | 219 | H | H | H | H | L | L | H | L | 159 | L | H | H | L | L | L | L | H | 99 |
| H | H | L | L | L | L | L | H | 218 | L | H | H | H | H | L | L | H | 158 | L | L | H | H | L | L | L | L | 98 |
| L | H | H | L | L | L | L | L | 217 | H | L | H | H | H | H | L | L | 157 | H | L | L | H | H | L | L | L | 97 |
| H | L | H | H | L | L | L | L | 216 | H | H | L | H | H | H | H | L | 156 | L | H | L | L | H | H | L | L | 96 |
| L | H | L | H | H | L | L | L | 215 | L | H | H | L | H | H | H | H | 155 | H | L | H | L | L | H | H | L | 95 |
| H | L | H | L | H | H | L | L | 214 | H | L | H | H | L | H | H | H | 154 | L | H | L | H | L | L | H | H | 94 |
| H | H | L | H | L | H | H | L | 213 | H | H | L | H | H | L | H | H | 153 | H | L | H | L | H | L | L | H | 93 |
| H | H | H | L | H | L | H | H | 212 | H | H | H | L | H | H | L | H | 152 | L | H | L | H | L | H | L | L | 92 |
| L | H | H | H | L | H | L | H | 211 | L | H | H | H | L | H | H | L | 151 | L | L | H | L | H | L | H | L | 91 |
| L | L | H | H | H | L | H | L | 210 | H | L | H | H | H | L | H | H | 150 | L | L | L | H | L | H | L | H | 90 |
| L | L | L | H | H | H | L | H | 209 | L | H | L | H | H | H | L | H | 149 | H | L | L | L | H | L | H | L | 89 |
| L | L | L | L | H | H | H | L | 208 | L | L | H | L | H | H | H | L | 148 | L | H | L | L | L | H | L | H | 88 |
| H | L | L | L | L | H | H | H | 207 | L | L | L | H | L | H | H | H | 147 | H | L | H | L | L | L | H | L | 87 |
| L | H | L | L | L | L | H | H | 206 | H | L | L | L | H | L | H | H | 146 | L | H | L | H | L | L | L | H | 86 |
| H | L | H | L | L | L | L | H | 205 | H | H | L | L | L | H | L | H | 145 | H | L | H | L | H | L | L | L | 85 |
| H | H | L | H | L | L | L | L | 204 | L | H | H | L | L | L | H | L | 144 | H | H | L | H | L | H | L | L | 84 |
| H | H | H | L | H | L | L | L | 203 | H | L | H | H | L | L | L | H | 143 | H | H | H | L | H | L | H | L | 83 |
| H | H | H | H | L | H | L | L | 202 | H | H | L | H | H | L | L | L | 142 | H | H | H | H | L | H | L | H | 82 |
| L | H | H | H | H | L | H | L | 201 | L | H | H | L | H | H | L | L | 141 | H | H | H | H | H | L | H | L | 81 |
| L | L | H | H | H | H | L | L | 200 | L | L | H | H | L | H | H | L | 140 | H | H | H | H | H | H | L | H | 80 |
| H | L | L | H | H | H | H | L | 199 | H | L | L | H | H | L | H | H | 139 | L | H | H | H | H | H | H | L | 79 |
| L | H | L | L | H | H | H | H | 198 | H | H | L | L | H | H | L | H | 138 | L | L | H | H | H | H | H | H | 78 |
| L | L | H | L | L | H | H | H | 197 | H | H | H | L | L | H | H | L | 137 | H | L | L | H | H | H | H | H | 77 |
| L | L | L | H | L | L | H | H | 196 | L | H | H | H | L | L | H | H | 136 | H | H | L | L | H | H | H | H | 76 |

FIGURE 2. DM7520/DM8520 Shift Register Divider Input Coding Table (2 Package Combinations)

**THEORY OF OPERATION** (Continued)

| Setting | | | | | | | | | Setting | | | | | | | | | Setting | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Divider 1 | | | | Divider 2 | | | | By | Divider 1 | | | | Divider 2 | | | | By | Divider 1 | | | | Divider 2 | | | | By |
| P1 | P2 | P3 | P4 | P1 | P2 | P3 | P4 | | P1 | P2 | P3 | P4 | P1 | P2 | P3 | P4 | | P1 | P2 | P3 | P4 | P1 | P2 | P3 | P4 | |
| H | H | H | L | L | H | H | H | 75 | L | L | H | H | H | H | L | L | 50 | L | H | H | L | L | H | H | L | 25 |
| H | H | H | H | L | L | H | H | 74 | L | L | L | H | H | H | H | L | 49 | H | L | H | H | L | L | H | H | 24 |
| H | H | H | H | H | L | L | H | 73 | H | L | L | L | H | H | H | H | 48 | H | H | L | H | H | L | L | H | 23 |
| L | H | H | H | H | H | L | L | 72 | H | H | L | L | L | H | H | H | 47 | H | H | H | L | H | H | L | L | 22 |
| L | L | H | H | H | H | H | L | 71 | L | H | H | L | L | L | H | H | 46 | H | H | H | H | L | H | H | L | 21 |
| L | L | L | H | H | H | H | H | 70 | L | L | H | H | L | L | L | H | 45 | L | H | H | H | H | L | H | H | 20 |
| L | L | L | L | H | H | H | H | 69 | L | L | L | H | H | L | L | L | 44 | H | L | H | H | H | H | L | H | 19 |
| L | L | L | L | L | H | H | H | 68 | H | L | L | L | H | H | L | L | 43 | L | H | L | H | H | H | H | L | 18 |
| H | L | L | L | L | L | H | H | 67 | L | H | L | L | L | H | H | L | 42 | H | L | H | L | H | H | H | H | 17 |
| L | H | L | L | L | L | L | H | 66 | L | L | H | L | L | L | H | H | 41 | L | H | L | H | L | H | H | H | 16 |
| H | L | H | L | L | L | L | L | 65 | L | L | L | H | L | L | L | H | 40 | H | L | H | L | H | L | H | H | 15 |
| L | H | L | H | L | L | L | L | 64 | H | L | L | L | H | L | L | L | 39 | L | H | L | H | L | H | L | H | 14 |
| L | L | H | L | H | L | L | L | 63 | L | H | L | L | L | H | L | L | 38 | H | L | H | L | H | L | H | L | 13 |
| L | L | L | H | L | H | L | L | 62 | L | L | H | L | L | L | H | L | 37 | H | H | L | H | L | H | L | H | 12 |
| L | L | L | L | H | L | H | L | 61 | H | L | L | H | L | L | L | H | 36 | L | H | H | L | H | L | H | L | 11 |
| H | L | L | L | L | H | L | H | 60 | L | H | L | L | H | L | L | L | 35 | L | L | H | H | L | H | L | H | 10 |
| L | H | L | L | L | L | H | L | 59 | H | L | H | L | L | H | L | L | 34 | L | L | L | H | H | L | H | L | 9 |
| L | L | H | L | L | L | L | H | 58 | L | H | L | H | L | L | H | L | 33 | H | L | L | L | H | H | L | H | 8 |
| L | L | L | H | L | L | L | L | 57 | L | L | H | L | H | L | L | H | 32 | H | H | L | L | L | H | H | L | 7 |
| L | L | L | L | H | L | L | L | 56 | H | L | L | H | L | H | L | L | 31 | H | H | H | L | L | L | H | H | 6 |
| H | L | L | L | L | H | L | L | 55 | H | H | L | L | H | L | H | L | 30 | H | H | H | H | L | L | L | H | 5 |
| H | H | L | L | L | L | H | L | 54 | L | H | H | L | L | H | L | H | 29 | H | H | H | H | H | L | L | L | 4 |
| H | H | H | L | L | L | L | H | 53 | L | L | H | H | L | L | H | L | 28 | H | H | H | H | H | H | L | L | 3 |
| H | H | H | H | L | L | L | L | 52 | H | L | L | H | H | L | L | H | 27 | H | H | H | H | H | H | H | L | 2 |
| L | H | H | H | H | L | L | L | 51 | H | H | L | L | H | H | L | L | 26 | | | | | | | | | |

**FIGURE 2. DM7520/DM8520 Shift Register Divider Input Coding Table (2 Package Combinations) (Continued)**

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

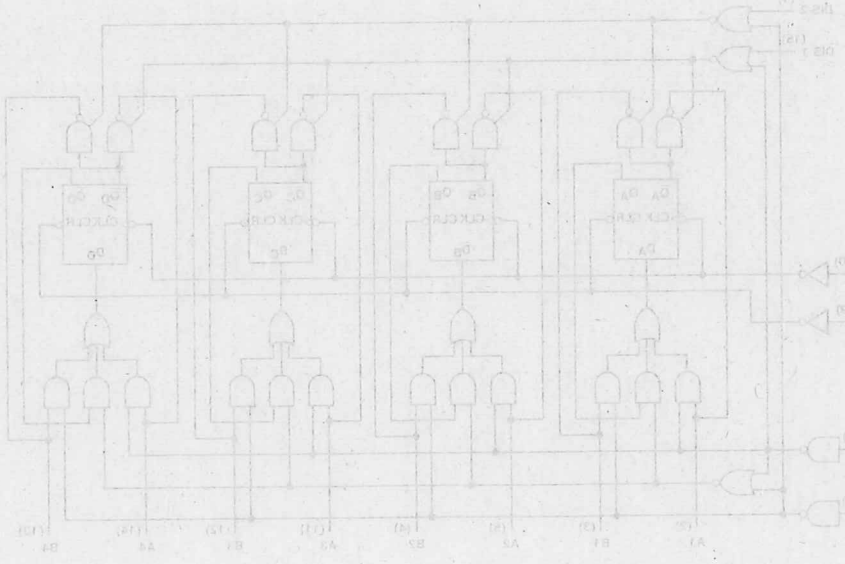
| Parameter | | Conditions | | DM75 | | | DM85 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 20 | | | 20 | | | |
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −400 | | | −400 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −400 μA | | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | | 0.4 | | | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | Ex-Or Input | | | 80 | | | 80 | μA |
| | | | Others | | | 40 | | | 40 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | Ex-Or Input | | | −3.2 | | | −3.2 | mA |
| | | | Others | | | −1.6 | | | −1.6 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −20 | | −55 | −18 | | −55 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | 50 | 75 | | 50 | 75 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | DM75/85 | | | Units |
|---|---|---|---|---|---|---|
| | | | 20 | | | |
| | | | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | $C_L$ = 15 pF, $R_L$ = 400 Ω | 15 | 20 | | MHz |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | 38 | 55 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | | 35 | 50 | ns |



# TRI-STATE® Quad I/O Registers

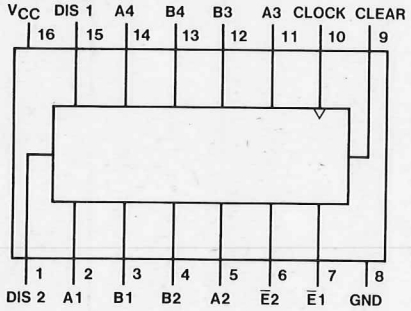
## General Description

These circuits are four-bit storage registers having two terminals per bit, which may be used as either inputs or outputs while tied to their individual bus lines. Storage capability is also provided by means of positive-edge triggered flip-flops having a common clock and asynchronous clear. Each I/O terminal can be forced into the high-impedance state by applying a high logic level to its disable control. The four A outputs are tied together on one disable control, while the four B outputs are tied together on a separate disable control.

## Features

- TRI-STATE outputs
- Typical clock frequency 40 MHz
- Typical propagation delay 24 ns
- Typical power dissipation 400 mW

## Connection Diagram




**7542 (J,W); 8542 (N)**

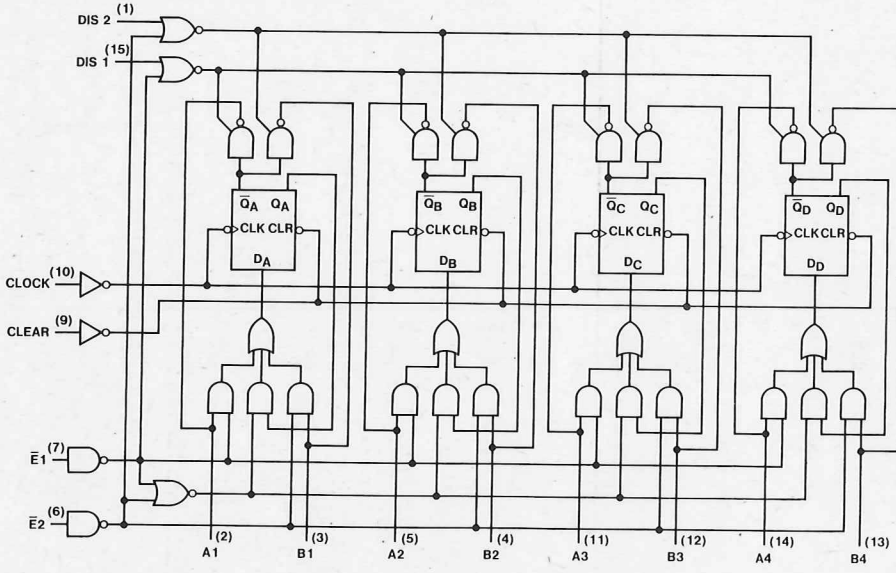
## Truth Table

MODES OF OPERATION

| DIS 1 | DIS 2 | $\overline{E1}$ | $\overline{E2}$ | A (1-4) | B (1-4) | Comments |
|---|---|---|---|---|---|---|
| L | H | H | H | Q | Hi-Z | Output data to Bus A |
| H | L | H | H | Hi-Z | Q | Output data to Bus B |
| L | L | H | H | Q | Q | Output data to both buses |
| H | H | H | H | Hi-Z | Hi-Z | Store data with output in high impedance state |
| X | L | L | H | Data | Qn | Enter data from Bus A |
| X | H | L | H | Data | Hi-Z | Enter data from Bus A |
| L | X | H | L | $Q_n$ | Data | Enter data from Bus B |
| H | X | H | L | Hi-Z | Data | Enter data from Bus B |
| X | X | L | L | Data | Data | Enter data from both buses (logical "1" on either will dominate) |

Clear = Logical "1," puts all outputs to L state.
X = Don't Care
$Q_n$ = Data After Clock Transition

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM75 42 | | | DM85 42 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −2.0 | | | −5.2 | mA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | | 0.4 | | | 0.4 | V |
| $I_{O(OFF)}$ | Off State (High Impedance State) Output Current | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V | $V_O$ = 0.4 V | | | −40 | | | −40 | μA |
| | | | $V_O$ = 2.4 V | | | 40 | | | 40 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | −1.0 | −1.6 | | −1.0 | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −25 | | −70 | −25 | | −70 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | 80 | 120 | | 80 | 120 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From | To | Conditions | DM75/85 42 | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | | | $C_L$ = 50 pF, $R_L$ = 400 Ω | 30 | 40 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock | Output | | | 25 | 38 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clock | Output | | | 23 | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clear | Output | | | 24 | 36 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | | Disable | Output | | | 20 | 30 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | Disable | Output | | | 17 | 25 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | | Disable | Output | $C_L$ = 5 pF, $R_L$ = 400 Ω | | 6 | 15 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | Disable | Output | | | 15 | 25 | ns |
| $t_{W(CLOCK)}$ | Clock Pulse Width | | | | $C_L$ = 50 pF, $R_L$ = 400 Ω | 20 | | | ns |
| $t_{W(CLEAR)}$ | Clear Pulse Width | | | | | 20 | | | ns |
| $t_{SETUP}$ | Enable Setup Time | High Level | | | | 20 | 12 | | ns |
| | | Low Level | | | | 20 | 13 | | |
| $t_{SETUP}$ | Data SetupTime | High Level | | | | 5.0 | −4.0 | | ns |
| | | Low Level | | | | 10 | 4.5 | | |
| $t_{HOLD}$ | Data Hold Time | High Level | | | | 5.0 | −3.5 | | ns |
| | | Low Level | | | | 10 | 4.5 | | |

# TRI-STATE® Quad Switch Debouncers

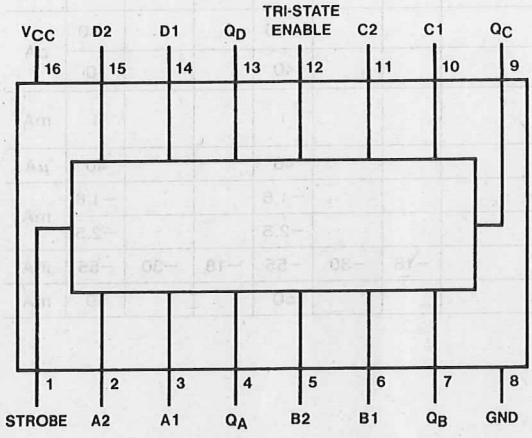
## General Description

These circuits are for use in front panels, and similar applications where contact bounce must be eliminated. Within the single package, these circuits do the job of four R-S latches plus pull-up resistors. A strobe is also available which permits sampling of the switch information at a predetermined time. TRI-STATE outputs are also provided for direct connections to the switch line bus.

## Features

- Replaces SN54279/74279
- Eliminates push-button noise
- Allows clocked devices to be operated from switches
- Maximum power dissipation 250 mW
- Bus-line connectable
- TRI-STATE outputs
- Typical propagation delay 18 ns

## Connection Diagram

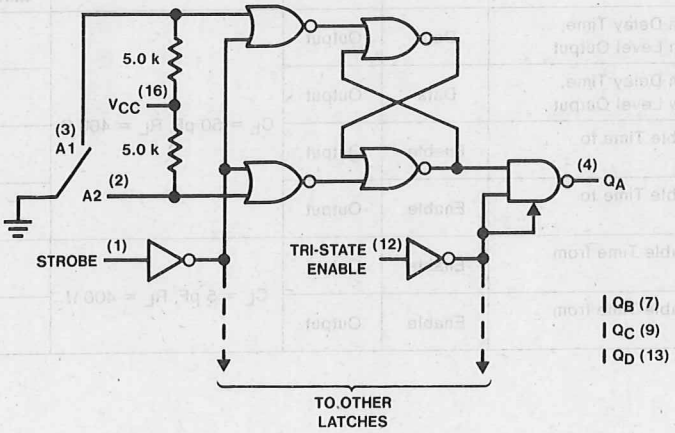



7544 (J,W)/8544 (N)

## Truth Table

| A1 | A2 | Tri-State Enable | Strobe | $Q_{A(t)}$ |
|---|---|---|---|---|
| X | X | H | X | Hi-Z |
| X | X | L | L | $Q_{A(t-1)}$ |
| L | L | L | ⌐ | Indeterminate |
| L | H | L | H | L |
| H | L | L | H | H |
| H | H | L | H | $Q_{A(t)}$ |

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM75 44 Min | DM75 44 Typ (1) | DM75 44 Max | DM85 44 Min | DM85 44 Typ (1) | DM85 44 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −2.0 | | | −5.2 | mA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | | 0.4 | | | 0.4 | V |
| $I_{O(OFF)}$ | Off State (High Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $V_O$ = 0.4 V | | | −40 | | | −40 | μA |
| | | | $V_O$ = 2.4 V | | | 40 | | | 40 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_{IH}$ = 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | Strobe/Enable | | | −1.6 | | | −1.6 | mA |
| | | | Data | | | −2.5 | | | −2.5 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −18 | −30 | −55 | −18 | −30 | −55 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | | 50 | | | 50 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C.

| Parameter | | From (Input) | To (Output) | Conditions | DM75/85 44 Min | DM75/85 44 Typ | DM75/85 44 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Output | $C_L$ = 50 pF, $R_L$ = 400 Ω | | 20 | 36 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Data | Output | | | 17 | 30 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | Enable | Output | | | 15 | 25 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | Enable | Output | | | 12 | 24 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | Enable | Output | $C_L$ = 5 pF, $R_L$ = 400 Ω | | 5 | 10 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | Enable | Output | | | 10 | 20 | ns |

# TRI-STATE® 8-Bit Universal I/O Shift Registers

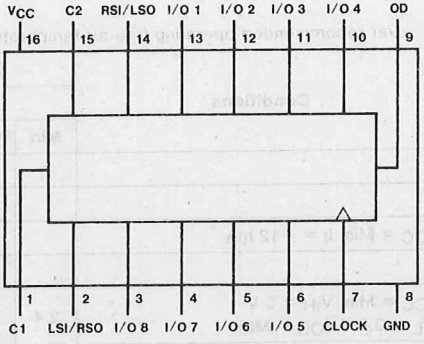
## General Description

These circuits are TRI-STATE, 8-bit, edge-triggered, universal shift registers which are capable of operating in any of the following modes: shift left, shift right, parallel load, or inhibit. Since the clock is edge-triggered, the control lines which determine the mode of operation are completely independent of the logic level applied to the clock. Designed for bus-oriented systems, these circuits have their TRI-STATE inputs and outputs on the same pins.

## Features

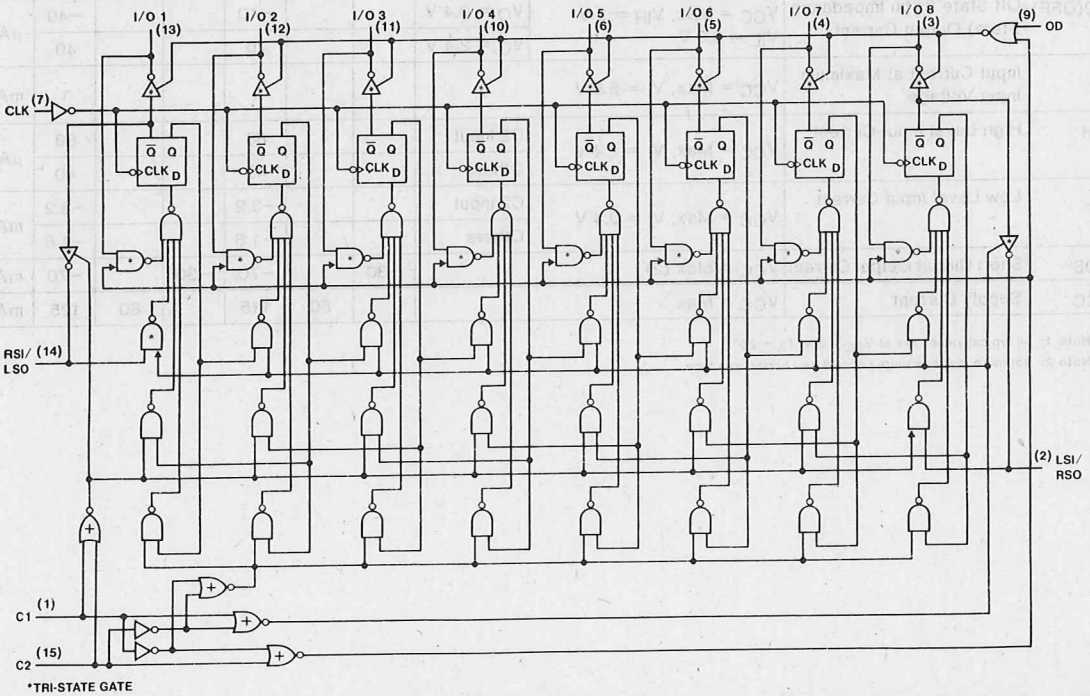
- Positive-edge triggered clock
- "Do nothing" state without gating the clock
- Both parallel and serial data lines are TRI-STATE
- High impedance state does not impede shift mode with parallel outputs

## Connection Diagram




7546 (J,W); 8546 (N)

## Logic Diagram



## Truth Table

| OD | C1 | C2 | Mode of Operation | State of Parallel I/O | State of Serial I/O | |
|---|---|---|---|---|---|---|
| | | | | | RSI/LSO | LSI/RSO |
| L | H | H | Inhibit | $Q_{OUT}$ | Hi-Z* | Hi-Z* |
| H | H | H | Inhibit | Hi-Z* | Hi-Z* | Hi-Z* |
| X | H | L | Parallel Load | Data In | Hi-Z* | Hi-Z* |
| L | L | H | Right Shift | $Q_{OUT}$ | Data In | $Q_{OUT}$ 8 |
| H | L | H | Right Shift | Hi-Z* | Data In | $Q_{OUT}$ 8 |
| L | L | L | Left Shift | $Q_{OUT}$ | $Q_{OUT}$ 1 | Data In |
| H | L | L | Left Shift | Hi-Z* | $Q_{OUT}$ 1 | Data In |

OD = Output Disable (C1, C2 = Mode Controls)

*Both Input and Output of the I/O pin are in the high impedance state.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM75 | | | DM85 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 46 | | | 46 | | | |
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −2.0 | | | −5.2 | mA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | | 0.4 | | | 0.4 | V |
| $I_{O(OFF)}$ | Off State (High Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $V_O$ = 0.4 V | | | −40 | | | −40 | μA |
| | | | $V_O$ = 2.4 V | | | 40 | | | 40 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | C2 Input | | | 80 | | | 80 | μA |
| | | | Others | | | 40 | | | 40 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | C2 Input | | | −3.2 | | | −3.2 | mA |
| | | | Others | | | −1.6 | | | −1.6 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −30 | | −70 | −30 | | −70 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | 80 | 115 | | 80 | 125 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more that one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

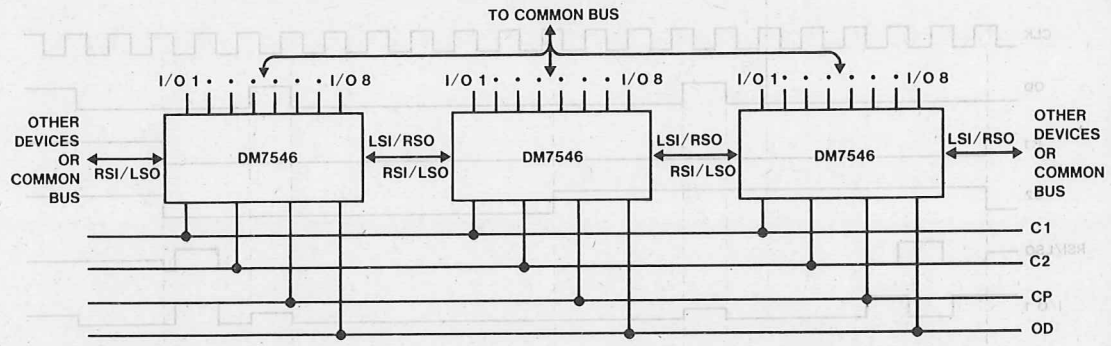
| Parameter | | Conditions | DM75/85 46 | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | $C_L$ = 50 pF, $R_L$ = 400 Ω | 15 | 22 | | MHz |
| $t_{PLH}$ | Propagation Delay, Low-to-High From Clock to Output | | | 16 | 24 | ns |
| $t_{PHL}$ | Propagation Delay, High-to-Low Level, From Clock to Output | | | 27 | 40 | ns |
| $t_{ZH}$ | Propagation Delay From High Impedance State to High Logic Level (From Output Disable) | | | 22 | 33 | ns |
| $t_{ZH}$ | Propagation Delay From High Impedance State to High Logic Level (From Mode Control C1/C2) | | | 13 | 20 | ns |
| $t_{ZL}$ | Propagation Delay From High Impedance State to Low Logic Level (From Output Disable) | | | 18 | 27 | ns |
| $t_{ZL}$ | Propagation Delay From High Impedance State to Low Logic Level (From Mode Control C1/C2) | | | 15 | 23 | ns |
| $t_{HZ}$ | Propagation Delay From High Logic Level to High Impedance State (From Output Disable) | $C_L$ = 5 pF, $R_L$ = 400 Ω | | 5 | 8 | ns |
| $t_{HZ}$ | Propagation Delay From High Logic Level to High Impedance State (From Mode Control C1/C2) | | | 9 | 14 | ns |
| $t_{LZ}$ | Propagation Delay From Low Logic Level to High Impedance State (From Output Disable) | | | 16 | 24 | ns |
| $t_{LZ}$ | Propagation Delay From Low Logic Level to High Impedance State (From Mode Control C1/C2) | | | 17 | 26 | ns |

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

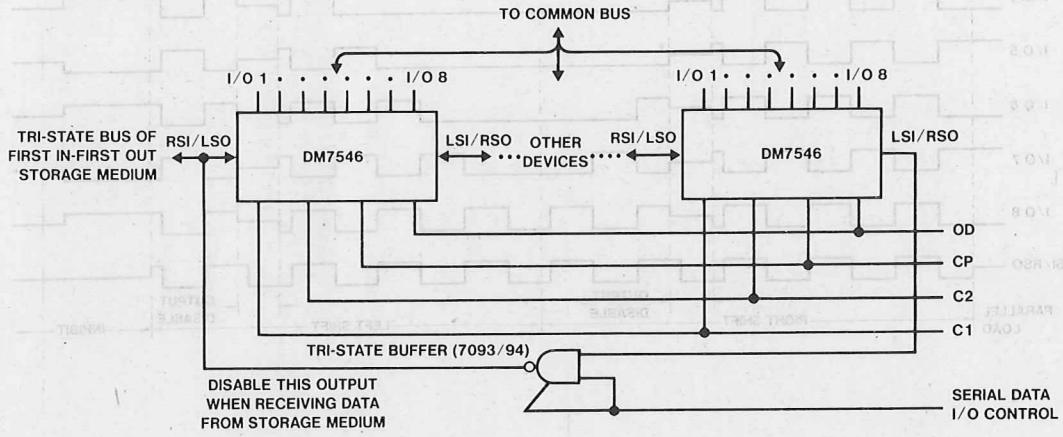
| Parameter | | Conditions | DM75/85 | | | Units |
|---|---|---|---|---|---|---|
| | | | 46 | | | |
| | | | Min | Typ | Max | |
| $t_{W(Clock)}$ | Clock Pulse Width | $C_L$ = 50 pF, $R_L$ = 400 Ω | 18 | 12 | | ns |
| $t_{SETUP\ (HIGH)}$ | Serial Data | | 38 | 25 | | ns |
| $t_{SETUP\ (HIGH)}$ | Parallel Data | | 33 | 22 | | ns |
| $t_{SETUP\ (LOW)}$ | Serial Data | | 21 | 14 | | ns |
| $t_{SETUP\ (LOW)}$ | Parallel Data | | 18 | 12 | | ns |
| $t_{HOLD\ (HIGH)}$ | Serial Data | | 0 | −11 | | ns |
| $t_{HOLD\ (HIGH)}$ | Parallel Data | | 0 | −11 | | ns |
| $t_{HOLD\ (LOW)}$ | Serial Data | | 0 | −22 | | ns |
| $t_{HOLD\ (LOW)}$ | Parallel Data | | 0 | −21 | | ns |
| SETUP AND HOLD TIMES BETWEEN CHANGES IN MODE CONTROL AND CLOCKING | | | | | | |
| $t_{SETUP}$ | Parallel Load to Right Shift | $C_L$ = 50 pF, $R_L$ = 400 Ω | 32 | 21 | | ns |
| $t_{SETUP}$ | Parallel Load to Left Shift | | 40 | 27 | | ns |
| $t_{SETUP}$ | Right Shift to Parallel Load | | 60 | 40 | | ns |
| $t_{SETUP}$ | Left Shift to Parallel Load | | 53 | 35 | | ns |
| $t_{SETUP}$ | Right Shift to Left Shift | | 33 | 21 | | ns |
| $t_{SETUP}$ | Left Shift to Right Shift | | 56 | 37 | | ns |
| $t_{SETUP}$ | Inhibit to Right Shift | | 57 | 38 | | ns |
| $t_{SETUP}$ | Inhibit to Left Shift | | 65 | 43 | | ns |
| $t_{SETUP}$ | Right Shift to Inhibit | | 50 | 33 | | ns |
| $t_{SETUP}$ | Left Shift to Inhibit | | 50 | 32 | | ns |
| $t_{HOLD}$ | Parallel Load to Right Shift | | 9 | 6 | | ns |
| $t_{HOLD}$ | Parallel Load to Left Shift | | 6 | 4 | | ns |
| $t_{HOLD}$ | Right Shift to Parallel Load | | 0 | −13 | | ns |
| $t_{HOLD}$ | Left Shift to Parallel Load | | 0 | −46 | | ns |
| $t_{HOLD}$ | Right Shift to Left Shift | | 0 | −10 | | ns |
| $t_{HOLD}$ | Left Shift to Right Shift | | 0 | −23 | | ns |
| $t_{HOLD}$ | Inhibit to Right Shift | | 0 | −18 | | ns |
| $t_{HOLD}$ | Inhibit to Left Shift | | 0 | −16 | | ns |
| $t_{HOLD}$ | Right Shift to Inhibit | | 0 | −12 | | ns |
| $t_{HOLD}$ | Left Shift to Inhibit | | 0 | −29 | | ns |

## Typical Applications

### Cascading Devices



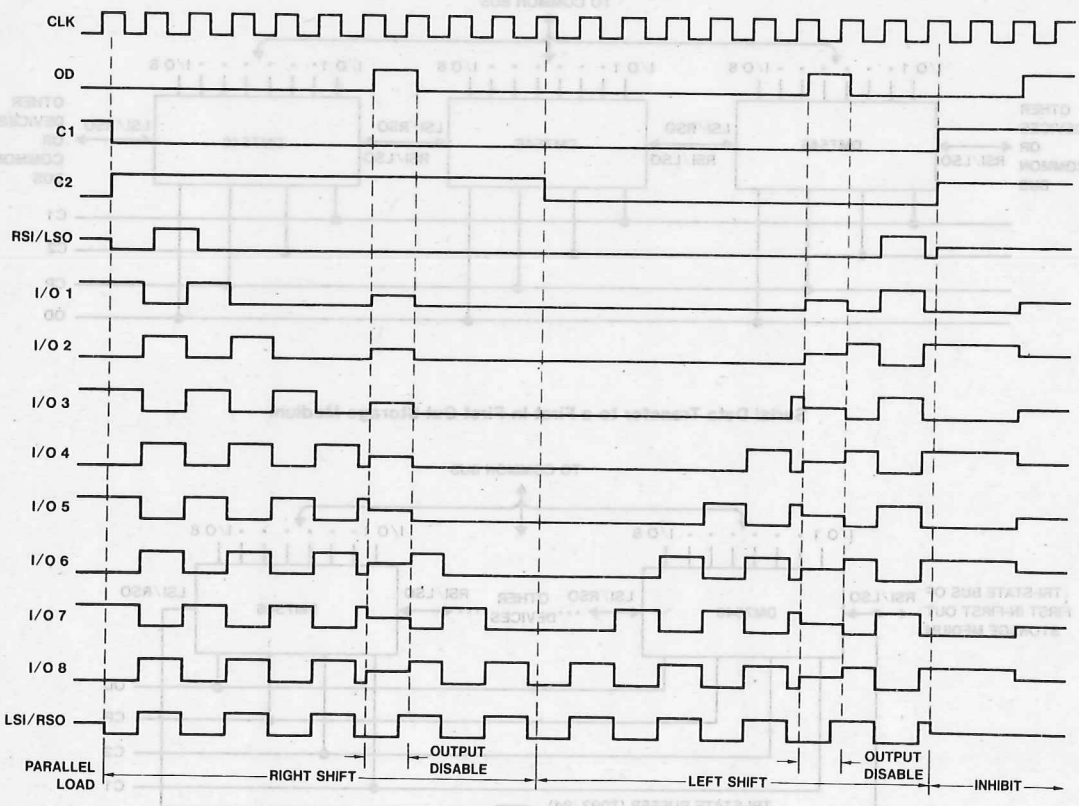

### Serial Data Transfer to a First In-First Out Storage Medium




7

## Typical Applications (Continued)

**Typical Parallel Load, Right Shift, Left Shift and Inhibit Sequences**



# TRI-STATE® 4-Bit D Type Registers

## General Description

These four-bit registers contain D-type flip-flops with totem-pole TRI-STATE outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.

Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus lines. Detailed operation is given in the truth table.

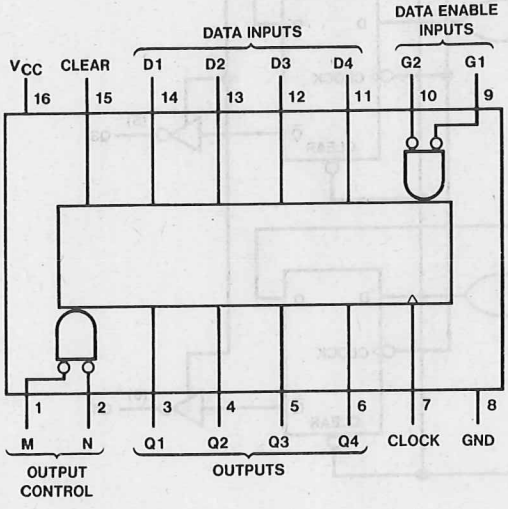
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

## Features

- TRI-STATE outputs interface directly with system bus
- Gated output control lines for enabling or disabling the outputs
- Fully independent clock eliminates restrictions for operating in one of two modes:
  - Parallel load
  - Do nothing (hold)
- For application as bus buffer registers

| Type | Typical Propagation Delay | Typical Frequency | Typical Power Dissipation |
|---|---|---|---|
| 7551/8551 | 18 ns | 30 MHz | 250 mW |
| 75L51/85L51 | 59 ns | 15 MHz | 27.5 mW |

## Connection Diagram




7551 (J,W)
75L51 (J,W)

8551 (N)
85L51 (N)

## Truth Table

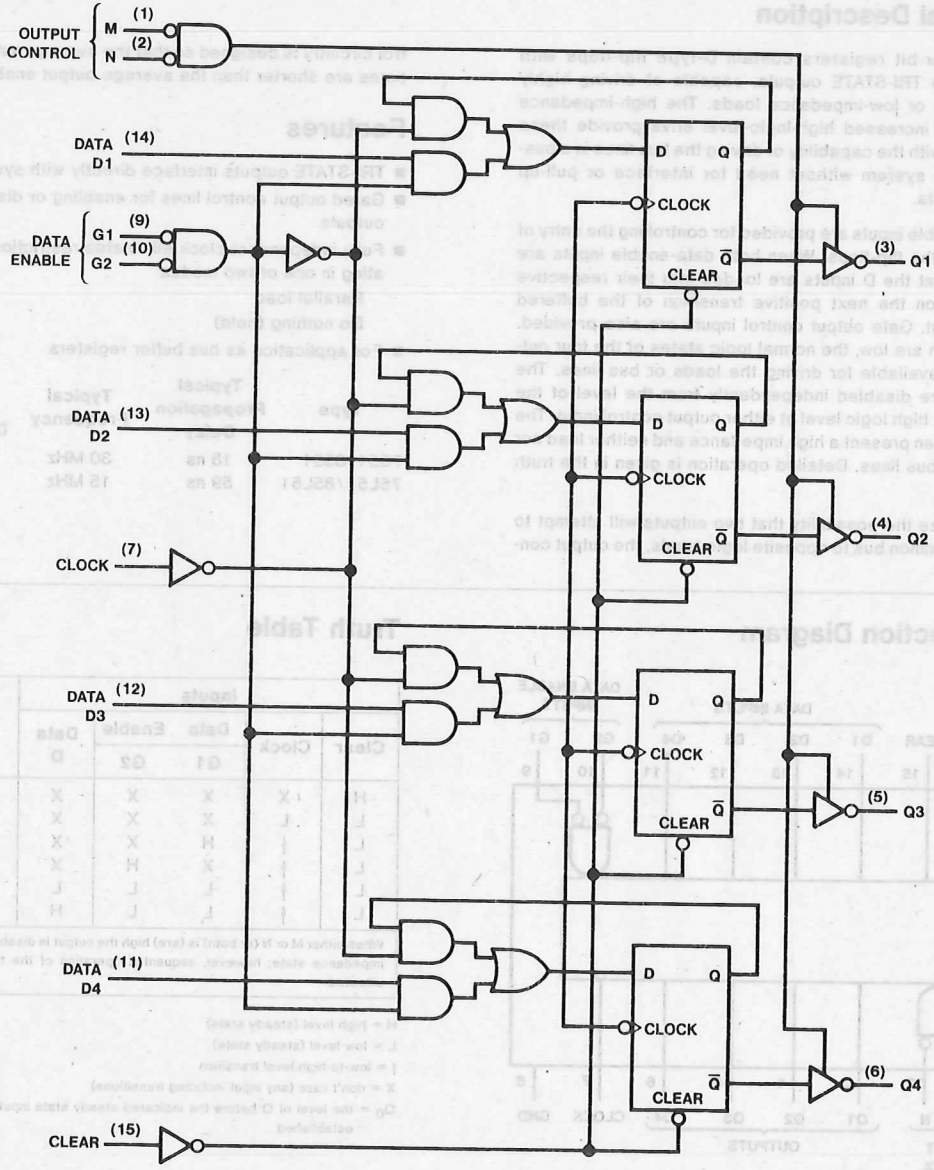
| Inputs | | | | | Output |
|---|---|---|---|---|---|
| Clear | Clock | Data Enable G1 | Data Enable G2 | Data D | Q |
| H | X | X | X | X | L |
| L | L | X | X | X | $Q_0$ |
| L | ↑ | H | X | X | $Q_0$ |
| L | ↑ | X | H | X | $Q_0$ |
| L | ↑ | L | L | L | L |
| L | ↑ | L | L | H | H |

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

H = high level (steady state)
L = low level (steady state)
↑ = low-to-high level transition
X = don't care (any input including transitions)
$Q_0$ = the level of Q before the indicated steady state input conditions were established

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## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM75/85 51 | | | DM75/85 L51 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | | | 0.7 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | N/A | V |
| $I_{OH}$ | High Level Output Current | | DM75 | | | −2.0 | | | −1.0 | mA |
| | | | DM85 | | | −5.2 | | | −1.0 | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | DM75 | | | 16 | | | 2.0 | mA |
| | | | DM85 | | | 16 | | | 3.6 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OL}$ = Max | DM75 | | | 0.4 | | 0.15 | 0.3 | V |
| | | | DM85 | | | 0.4 | | 0.2 | 0.4 | |
| $I_{O(OFF)}$ | Off State (High Impedance State) Output Current | $V_{CC}$ = Max, $V_{IL}$ = 2 V | $V_O$ = 0.3 V | | | | | | −40 | μA |
| | | | $V_O$ = 0.4 V | | | −40 | | | | |
| | | $V_{IL}$ = Max | $V_O$ = 2.4 V | | | 40 | | | 20 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | | 0.01 | 0.1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | | 1 | 10 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | | −0.18 | mA |
| | | | $V_I$ = 0.4 V | | | −1.6 | | | | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −30 | | −70 | −3 | −8 | −15 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | | 50 | 72 | | 5.5 | 9 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time.

**Note 3:** $I_{CC}$ is measured with all outputs open; clear grounded following momentary connection to 4 5 V; N, G1, G2, and all data inputs grounded; and the clock input and M at 4.5 V.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From | To | Conditions | | | DM75/85 51 | | | DM75/85 L51 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Both | Std. | Low Power | Min | Typ | Max | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | | | $C_L$ = 50 pF | $R_L$ = 400 Ω | $R_L$ = 4 kΩ | 25 | 30 | | 6 | 15 | | MHz |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clear | Output | | | | | 18 | 27 | | 72 | 110 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock | Output | | | | | 16 | 25 | | 39 | 70 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clock | Output | | | | | 20 | 28 | | 77 | 120 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | | Enable | Output | | | | 7 | 16 | 30 | | 28 | 55 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | Enable | Output | | | | 7 | 21 | 30 | | 35 | 60 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | | Enable | Output | $C_L$ = 5 pF | | | 3 | 5 | 14 | | 18 | 50 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | Enable | Output | | | | 3 | 11 | 20 | | 32 | 75 | ns |
| $t_W$ | Width of Clock or Clear Pulse | | | | | | | 20 | | | 100 | | | ns |
| $t_{SETUP}$ | Setup Time | Data Enable | | | | | | 17 | | | 45 | | | ns |
| | | Data | | | | | | 10 | | | 30 | | | |
| | | Clear Inactive State | | | | | | 10 | | | 30 | | | |
| $t_{HOLD}$ | Hold Time | Data Enable | | | | | | 2 | | | 0 | | | ns |
| | | Data | | | | | | 10 | | | 10 | | | |

# TRI-STATE® Synchronous Counters/Latches

## General Description

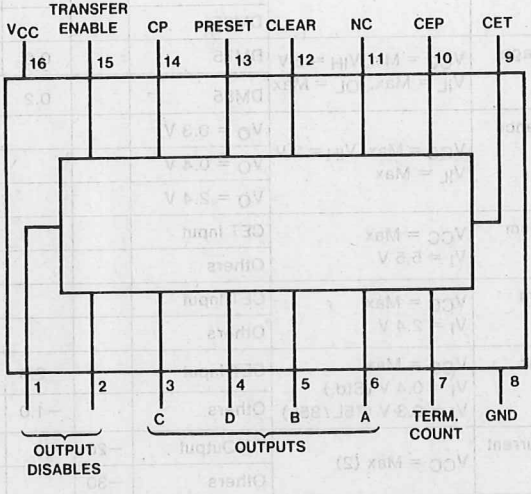
These circuits logically combine the functions of counters for frequency division, latches to store the data from the counters, and output buffer gates which provide both standard TTL outputs as well as high-impedance outputs for multiplexing of data. The counters are fully synchronous, and are made up of four edge-triggered JK flip-flops. To further facilitate operation, the Count Mode and Terminal Count outputs are also operable when the data outputs are in the high-impedance state or the latch mode.

## Features

- DM7552/8552 DM75L52/85L52 — Decade counter/latch
- DM7554/8554 DM75L54/85L54 — Binary counter/latch

| Type | Typical Power Dissipation | Typical Clock Frequency |
|---|---|---|
| 52, 54 | 330 mW | 23 MHz |
| L52, L54 | 38 mW | 11 MHz |

## Connection Diagram




7552 (J,W)
75L52 (J,W)
7554 (J,W)
75L54 (J,W)

8552 (N)
85L52 (N)
8554 (N)
85L54 (N)

## Truth Table

| Inputs | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OD1 | OD2 | CEP | CET | Clear | Preset | TE | A | B | C | D | TC |
| H | X | X | X | X | X | X | "High Impedance State" | | | | • |
| X | H | X | X | X | X | X | "High Impedance State" | | | | • |
| L | L | X | X | H | X | H | L | L | L | L | L |
| L | L | X | X | L | H | H | H | H | H | H | • |
| L | L | X | X | X | X | L | LATCH | | | | • |
| L | L | H | H | L | L | H | COUNT | | | | • |

*Function of the count sequence.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | DM75/85 52, 54 | | | DM75/85 L52, L54 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.8 | | | 0.7 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | N/A | V |
| $I_{OH}$ | High Level Output Current | | | DM75 | | | −2.0 | | | −1.0 | mA |
| | | | | DM85 | | | −5.2 | | | −1.0 | |
| $V_{OH}$ | High Level Output Voltage | Terminal Count | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $I_{OH}$ = 0.2 mA | | | | 2.4 | 2.8 | | V |
| | | | | $I_{OH}$ = 0.4 mA | 2.4 | 3.3 | | | | | |
| | | Others | | $I_{OH}$ = Max | 2.4 | 3.3 | | 2.4 | 2.7 | | |
| $I_{OL}$ | Low Level Output Current | | | DM75 | | | 16 | | | 2.0 | mA |
| | | | | DM85 | | | 16 | | | 3.6 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OL}$ = Max | DM75 | | 0.2 | 0.4 | | 0.15 | 0.3 | V |
| | | | | DM85 | | 0.2 | 0.4 | | 0.2 | 0.4 | |
| $I_{O(OFF)}$ | Off State (High Impedance State) Output Current | | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $V_O$ = 0.3 V | | | | | | −40 | μA |
| | | | | $V_O$ = 0.4 V | | | −40 | | | | |
| | | | | $V_O$ = 2.4 V | | | 40 | | | 20 | |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max, $V_I$ = 5.5 V | CET Input | | | 2 | | 0.02 | 0.2 | mA |
| | | | | Others | | | 1 | | 0.01 | 0.1 | |
| $I_{IH}$ | High Level Input Current | | $V_{CC}$ = Max, $V_I$ = 2.4 V | CET Input | | | 80 | | 2 | 20 | μA |
| | | | | Others | | | 40 | | 1 | 10 | |
| $I_{IL}$ | Low Level Input Current | | $V_{CC}$ = Max, $V_I$ = 0.4 V (Std.), $V_I$ = 0.3 V (75L/85L) | CET Input | | −2.0 | −3.2 | | −0.24 | −0.36 | mA |
| | | | | Others | | −1.0 | −1.6 | | −0.12 | −0.18 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | TC Output | −20 | | −55 | −3 | −8 | −15 | mA |
| | | | | Others | −30 | | −70 | −3 | −8 | −15 | |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max | | | 66 | 106 | | 7.6 | 13 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time, and for DM7554/8554 duration of short circuit should not exceed one second.

## Switching Characteristics $V_{CC}$= 5 V, $T_A$ = 25°C

| Parameter | | From | To | Conditions | | | DM75/85 52, 54 | | | DM75/85 L52, L54 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Both | Std. | Low Power | Min | Typ | Max | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | | $C_L$ = 50 pF | $R_L$ = 400 Ω | $R_L$ = 4 kΩ | 15 | 23 | | 6 | 11 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Clock | Output | | | | | 34 | 70 | | 115 | 220 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low-Level Output | Clock | Output | | | | | 23 | 45 | | 75 | 150 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Transfer Enable | Output | | | | | 26 | 50 | | 90 | 160 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Transfer Enable | Output | | | | | 26 | 50 | | 90 | 160 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | Output Disable | Output | | | | | 21 | 45 | | 75 | 150 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | Output Disable | Output | | | | | 25 | 50 | | 90 | 150 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | Output Disable | Output | $C_L$ = 5 pF | | | | 3 | 8 | | 8 | 15 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | Output Disable | Output | | | | | 17 | 40 | | 57 | 105 | ns |

## Mode of Operation

When the Transfer Enable (TE) is at a logical "1" level, the data transfer paths between the counter outputs and the output buffer gates are maintained. When the Transfer Enable is at a logical "0" level, the data transfer paths are inhibited, and the state of the output buffer gates are locked in by the latches. The counter and Terminal Count (TC) output remain operable during this time.

Asynchronous Clear resets the counter to 0000.

Asynchronous Preset sets the counter to 1111. The 1111 state may be used in the 52 for blanking out leading zeroes in visual displays. The next clock pulse will advance the 52 to 0001 which denotes the first count of the blanked zero. The next clock pulse will advance the 54 to 0000.

The Terminal Count (TC) output is active high when the counters are at terminal count and the CET is high. The Terminal Count logic equations are:

(52) $TC = CET \cdot A \cdot \overline{B} \cdot \overline{C} \cdot D$
(54) $TC = CET \cdot A \cdot B \cdot C \cdot D$

The following logic levels control the device:

- The counters change state on the positive-going transition of the clock.
- Clearing or presetting is enabled by taking the respective input to a logical "1" level.
- To enable the count mode both CET and CEP inputs must be at a logical "1" level.
- To latch the outputs the Transfer Enable (TE) input must be taken to the logical "0" level.
- To place the TRI-STATE outputs into the "third-state," either of the Output Disable (OD) inputs must be taken to the logical "1" level.

The clock input must be high during the high to low transition of CEP and/or CET for correct logic operation. The CEP and CET inputs may be used in a high speed look ahead technique.

Counter stages can be cascaded to provide multiple stage BCD or Binary synchronous counting by using the 52 or the 54 respectively. With a Terminal Count (TC) fan out of ten, eleven stages are able to operate at the maximum frequency equivalent to a two stage counter.

The characters displayed can be held with a low level on the TE input while the counters can continue counting. The display can be updated at any time by applying a positive pulse to the TE input.

**DM7552/DM8552**
**DM75L52/DM85L52**
**DECADE COUNT SEQUENCE**

| Count | Outputs | | | | |
|---|---|---|---|---|---|
| | A | B | C | D | TC |
| 0 | L | L | L | L | L |
| 1 | H | L | L | L | L |
| 2 | L | H | L | L | L |
| 3 | H | H | L | L | L |
| 4 | L | L | H | L | L |
| 5 | H | L | H | L | L |
| 6 | L | H | H | L | L |
| 7 | H | H | H | L | L |
| 8 | L | L | L | H | L |
| 9 | H | L | L | H | H |
| **If Preset Applied Next Count | H<br>H | H<br>L | H<br>L | H<br>L | L<br>L |

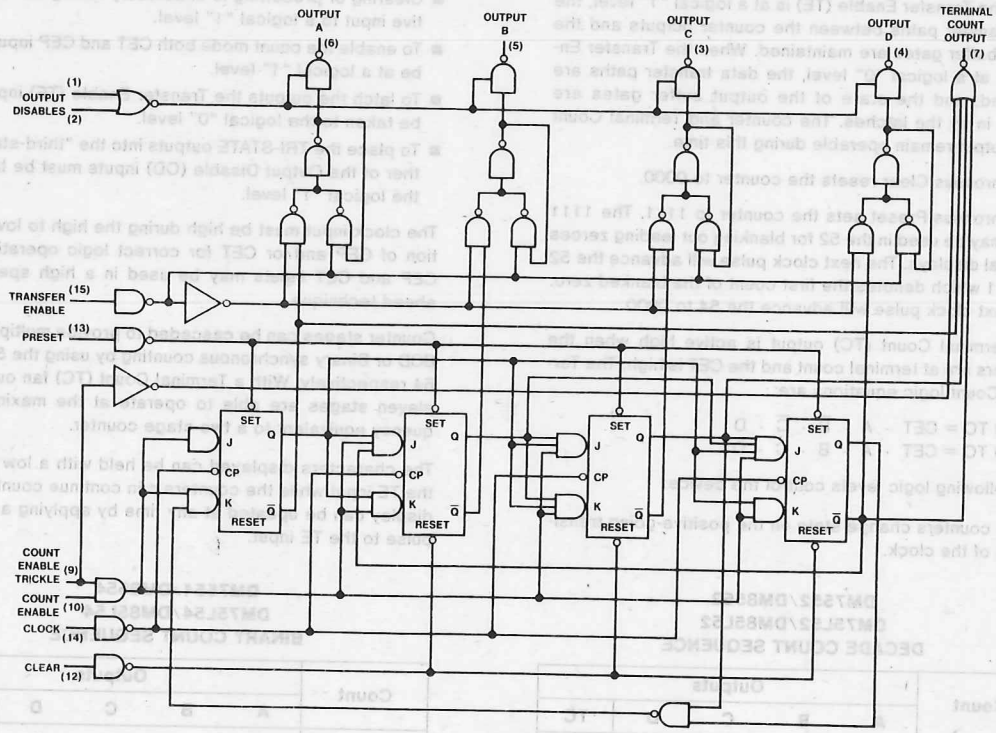
**The 111 state may be used in conjunction with certain decoder/drivers (DM7446A, 7447A, 7448) for blanking leading zeroes.

**DM7554/DM8554**
**DM75L54/DM85L54**
**BINARY COUNT SEQUENCE**

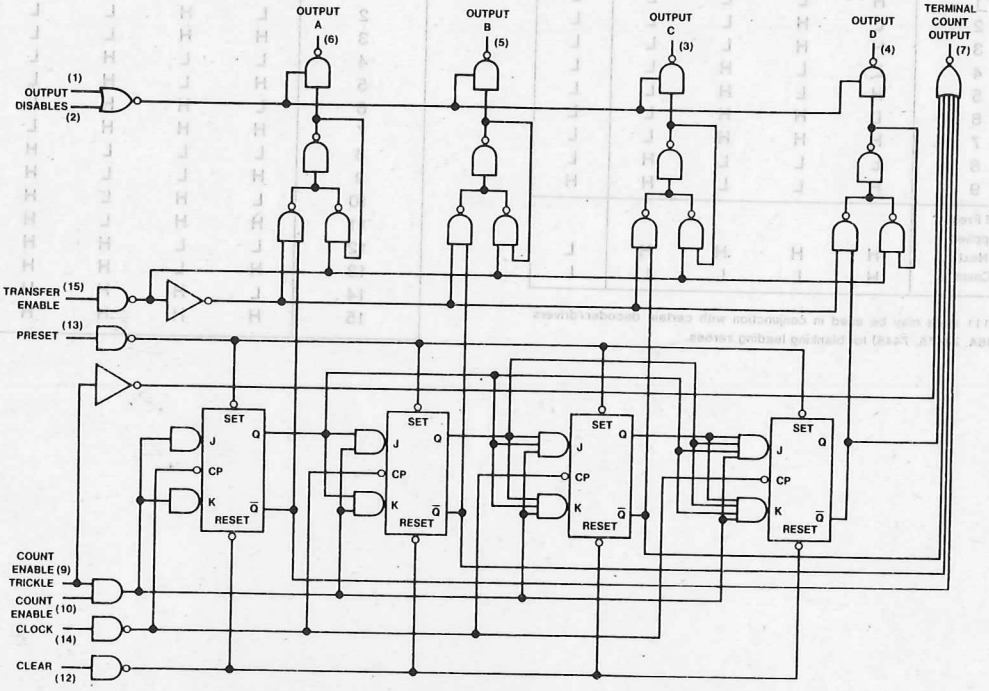
| Count | Outputs | | | | |
|---|---|---|---|---|---|
| | A | B | C | D | TC |
| 0 | L | L | L | L | L |
| 1 | H | L | L | L | L |
| 2 | L | H | L | L | L |
| 3 | H | H | L | L | L |
| 4 | L | L | H | L | L |
| 5 | H | L | H | L | L |
| 6 | L | H | H | L | L |
| 7 | H | H | H | L | L |
| 8 | L | L | L | H | L |
| 9 | H | L | L | H | L |
| 10 | L | H | L | H | L |
| 11 | H | H | L | H | L |
| 12 | L | L | H | H | L |
| 13 | H | L | H | H | L |
| 14 | L | H | H | H | L |
| 15 | H | H | H | H | H |

## Logic Diagrams

52, L52

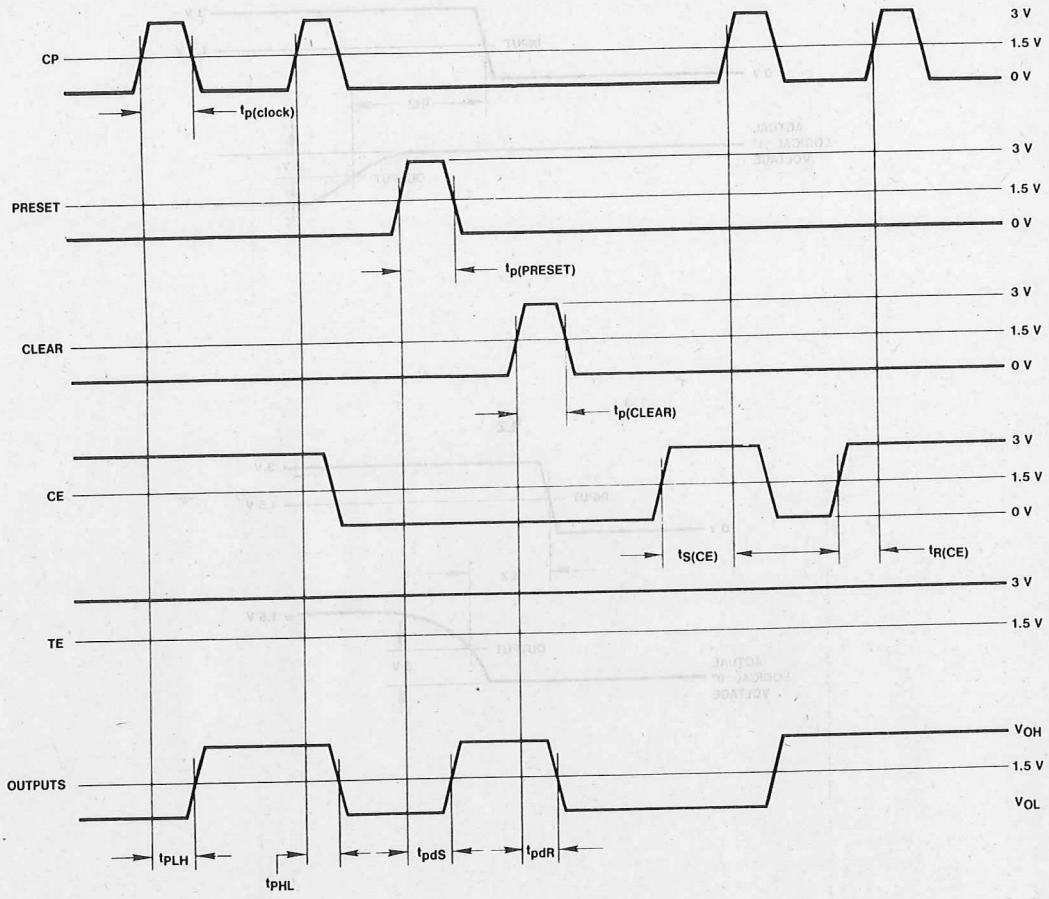


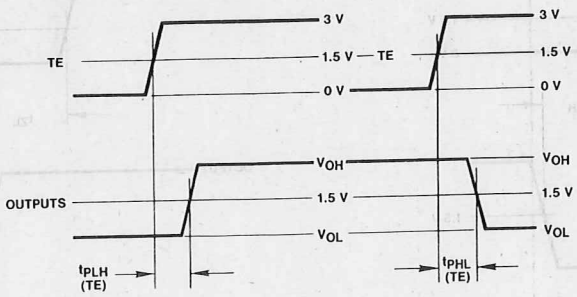

54, L54



## Switching Time Waveforms

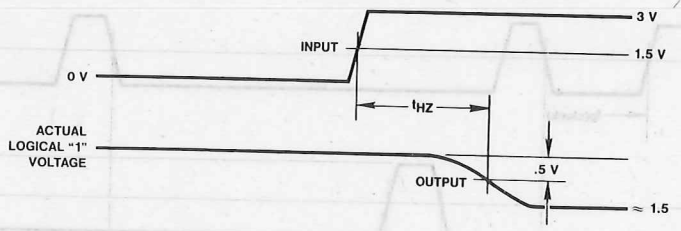
52, 54



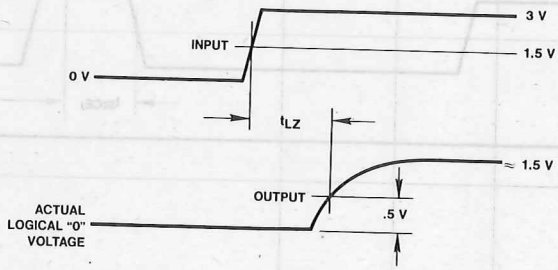



## Switching Time Waveforms (Continued)

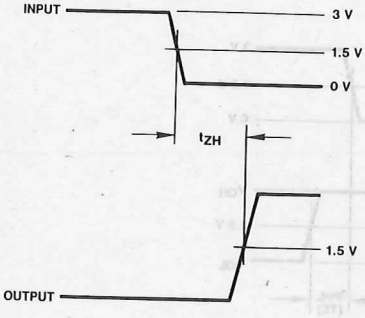
$t_{HZ}$



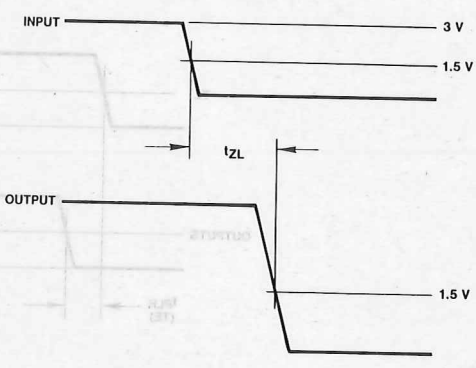

$t_{LZ}$




$t_{ZH}$

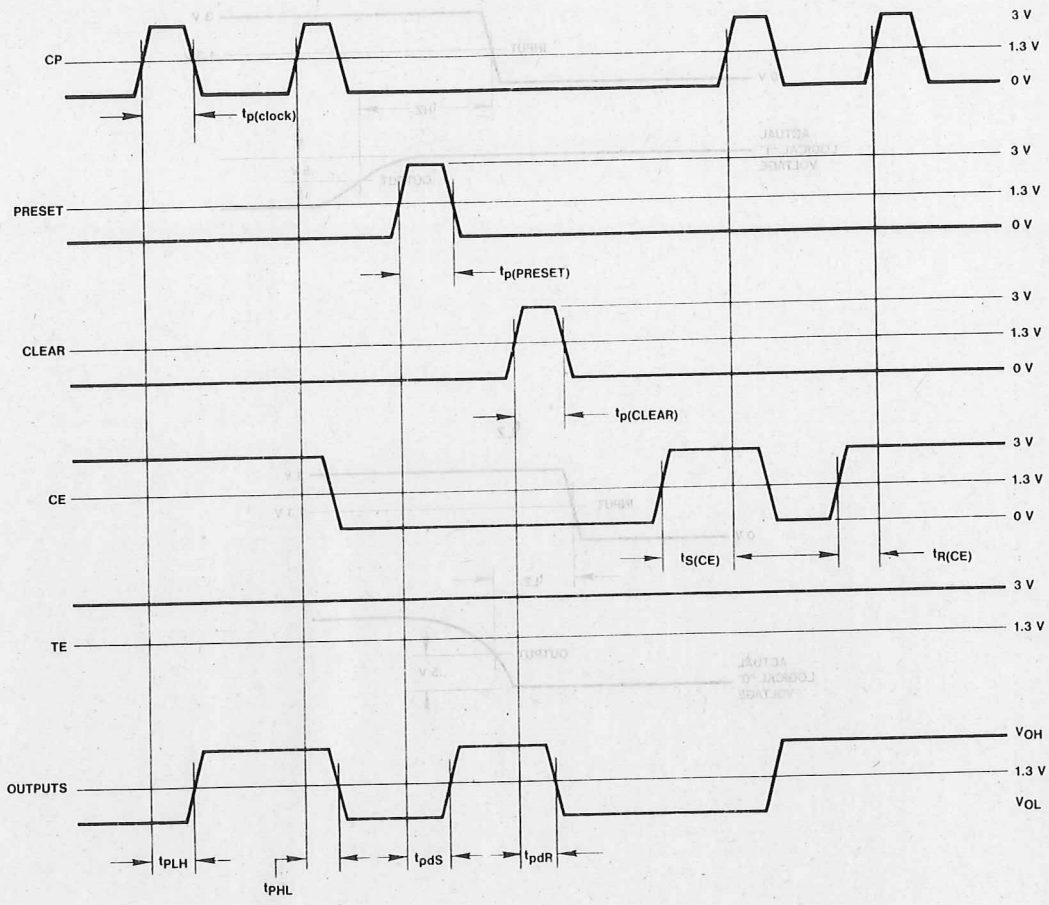


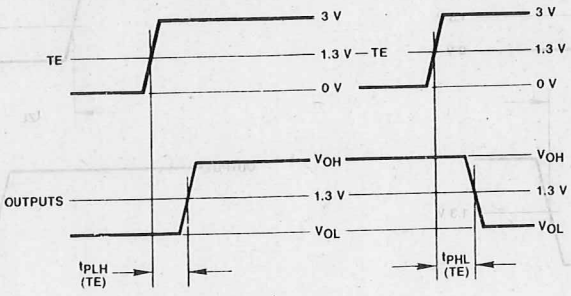

$t_{ZL}$



## Switching Time Waveforms (Continued)

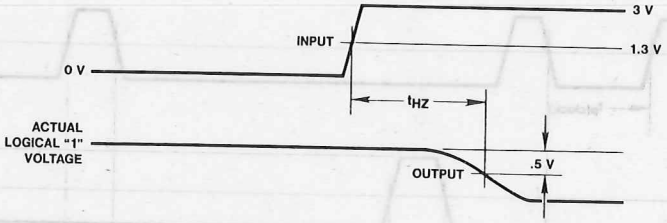
L52, L54



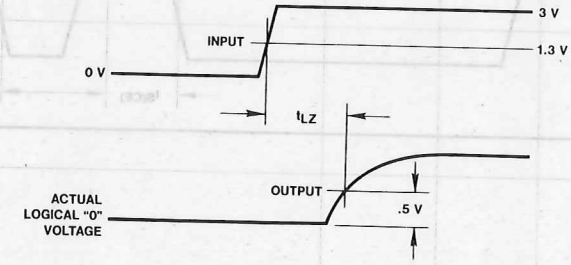



## Switching Time Waveforms (Continued)

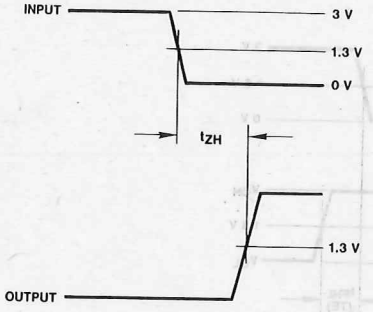
$t_{HZ}$



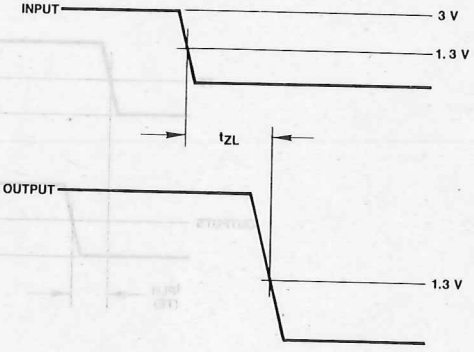

$t_{LZ}$




$t_{ZH}$




$t_{ZL}$



# TRI-STATE® 8-Bit Latches

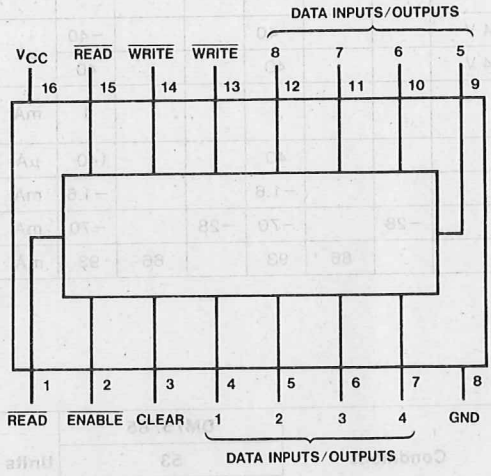
## General Description

By utilizing TRI-STATE circuitry on the outputs, the inputs and outputs can be accessed on the same pins, and these circuits provide eight separate $\overline{R}$-$\overline{S}$ latches in the popular 16-pin package. While in the high-impedance state, the inputs and outputs are disabled and no information can be entered. When both $\overline{WRITE}$ inputs are brought to a low logic level, the outputs are disabled and new information may be entered at the inputs. When a low logic level is applied to both $\overline{READ}$ inputs, and a high logic level to both $\overline{WRITE}$ inputs, the inputs are rendered inactive and data may be read from the outputs.

## Features

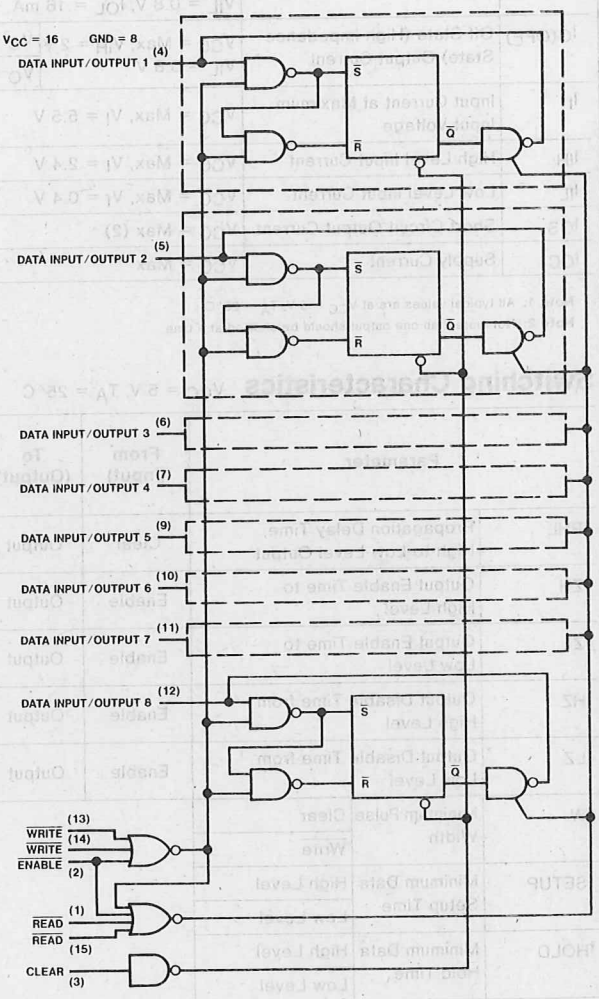
- TRI-STATE I/O pins
- 8 latches in popular 16-pin package
- Typical propagation delay—22 ns

## Connection Diagram




7553 (J,W); 8553 (N)

## Logic Diagram




## Truth Table

| Clear | $\overline{Enable}$ | $\overline{Read}$* | $\overline{Write}$** | Operation | State of Bus |
|---|---|---|---|---|---|
| H | L | L | H | Enter L | L |
| H | L | L | L | Enter L | Hi-Z |
| L | X | H | H | Do Nothing | Hi-Z |
| L | H | X | X | Do Nothing | Hi-Z |
| L | L | X | L | Write | H or L *** |
| L | L | L | H | Read | H or L *** |

*Both Read Inputs
**Both Write Inputs
***Depends on State of Latch

7

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

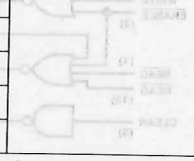
| Parameter | | Conditions | DM75 53 Min | DM75 53 Typ (1) | DM75 53 Max | DM85 53 Min | DM85 53 Typ (1) | DM85 53 Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | −2.0 | | | −5.2 | mA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | V |
| $I_{O(OFF)}$ | Off State (High Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $V_O$ = 0.4 V | | | −40 | | | −40 | μA |
| | | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $V_O$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | −1.6 | | | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | −28 | | −70 | −28 | | −70 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | 66 | 93 | | 66 | 93 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | To (Output) | Conditions | DM75/85 53 Min | DM75/85 53 Typ | DM75/85 53 Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation Delay Time, High-to-Low-Level Output | | Clear | Output | $C_L$ = 50 pF, $R_L$ = 400 Ω | | 21 | 32 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | | Enable | Output | | | 22 | 33 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | Enable | Output | | | 25 | 38 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | | Enable | Output | $C_L$ = 5 pF, $R_L$ = 400 Ω | | 7 | 12 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | Enable | Output | | | 20 | 30 | ns |
| $t_W$ | Minimum Pulse Width | Clear | | | | 15 | 10 | | ns |
| | | $\overline{\text{Write}}$ | | | | 40 | 28 | | |
| $t_{SETUP}$ | Minimum Data Setup Time | High Level | | | | 20 | 14 | | ns |
| | | Low Level | | | | 36 | 26 | | |
| $t_{HOLD}$ | Minimum Data Hold Time | High Level | | | | −15 | −26 | | ns |
| | | Low Level | | | | −8 | −14 | | |



# TRI-STATE® Programmable Decade/Binary Counters

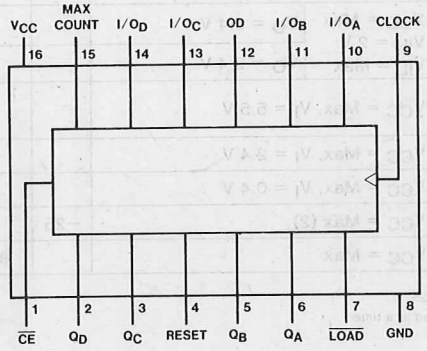
## General Description

These circuits are synchronous, edge-sensitive, fully-programmable 4-bit counters. The counters feature both conventional totem-pole and TRI-STATE outputs; such that when the outputs are in the high-impedance mode, they can be used to enter data from the bus lines. In addition, the clear input operates completely independent of all other inputs. During the programming operation, data is loaded into the flip-flops on the positive-going edge of the clock pulse. To facilitate cascading of these counters, the MAX COUNT output can be tied directly into the count enable input of the next counter.

## Features

- DM7555/8555—Decade counter
- DM7556/8556—Binary counter
- Typical clock frequency 35 MHz
- TRI-STATE outputs
- Fully independent clear
- Synchronous loading
- Cascading circuitry provided internally

## Connection Diagram




**7555 (J,W)**
**7556 (J,W)**

**8555 (N)**
**8556 (N)**

## Truth Table

| Control Inputs | | | | | I/O Ports | | | | Active Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{LOAD}$ | $\overline{CE}$ | CLK | OD | Reset | $I/O_A$ | $I/O_B$ | $I/O_C$ | $I/O_D$ | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| H | X | X | L | H | L | L | L | L | L | L | L | L |
| H | X | X | H | H | Z | Z | Z | Z | L | L | L | L |
| H | X | L | L | L | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| H | X | L | H | L | Z | Z | Z | Z | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| L | H | ↑ | L | L | a | b | c | d | A | B | C | D |
| H | L | ↑ | L | L | | COUNT | | | | COUNT | | |
| H | L | ↑ | H | L | Z | Z | Z | Z | | COUNT | | |

The I/O pins are used as inputs when they are TRI-STATED, and the $\overline{LOAD}$ input is Low. They are outputs and active when $\overline{LOAD}$ input is High and OD is Low.

H = High Level (Steady State)

L = Low Level (Steady State)

X = Don't Care including transitions

a, b, c, d = The level of the steady state input at inputs A, B, C, D respectively

$Q_{A0}$, $Q_{B0}$, $Q_{C0}$, $Q_{D0}$ = The level of $Q_A$, $Q_B$, $Q_C$, $Q_D$ repectively, before the indicated steady state input conditions were established.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM75/85 | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 55 | | | 56 | | | |
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | DM75 | | | −2.0 | | | −2.0 | mA |
| | | | DM85 | | | −5.2 | | | −5.2 | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | 0.4 | | | 0.4 | | | V |
| $I_{O(OFF)}$ | Off State (High Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = Max | $V_O$ = 0.4 V | | | −40 | | | −40 | μA |
| | | | $V_O$ = 2.4 V | | | 40 | | | 40 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −1.6 | | | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −25 | | −70 | −25 | | −70 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | 80 | 110 | | 75 | 100 | mA |

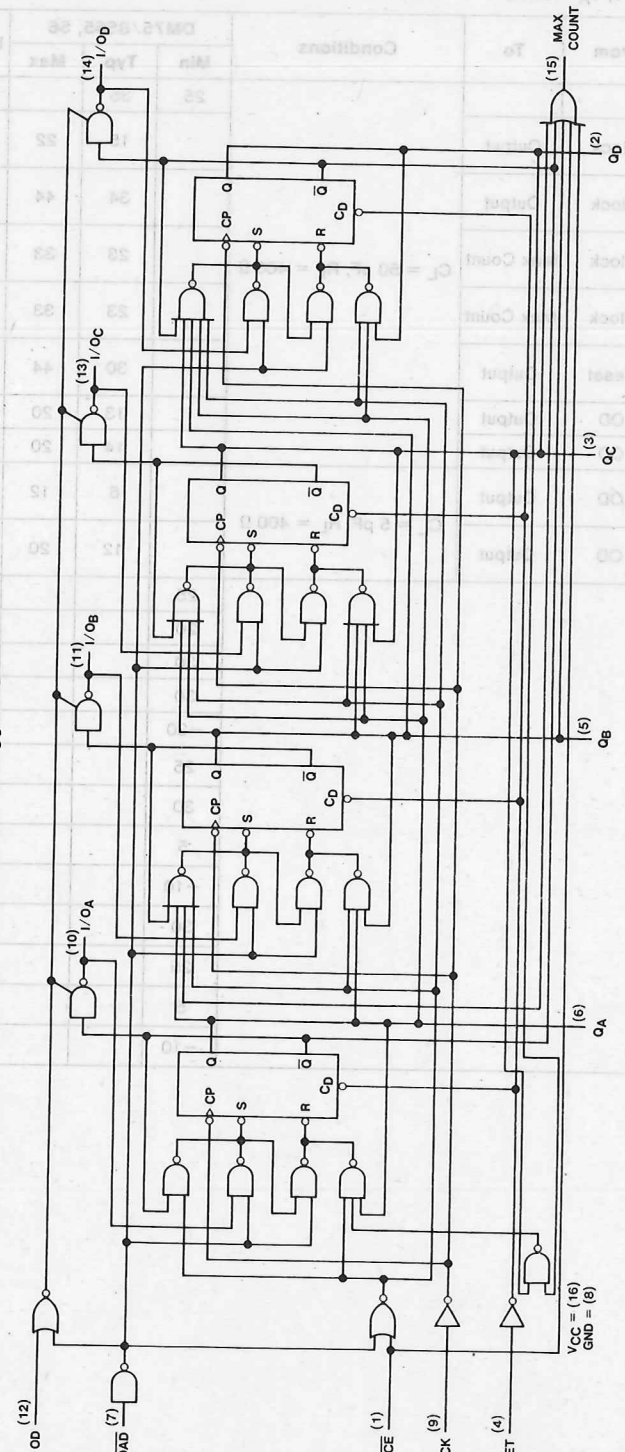
**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C.

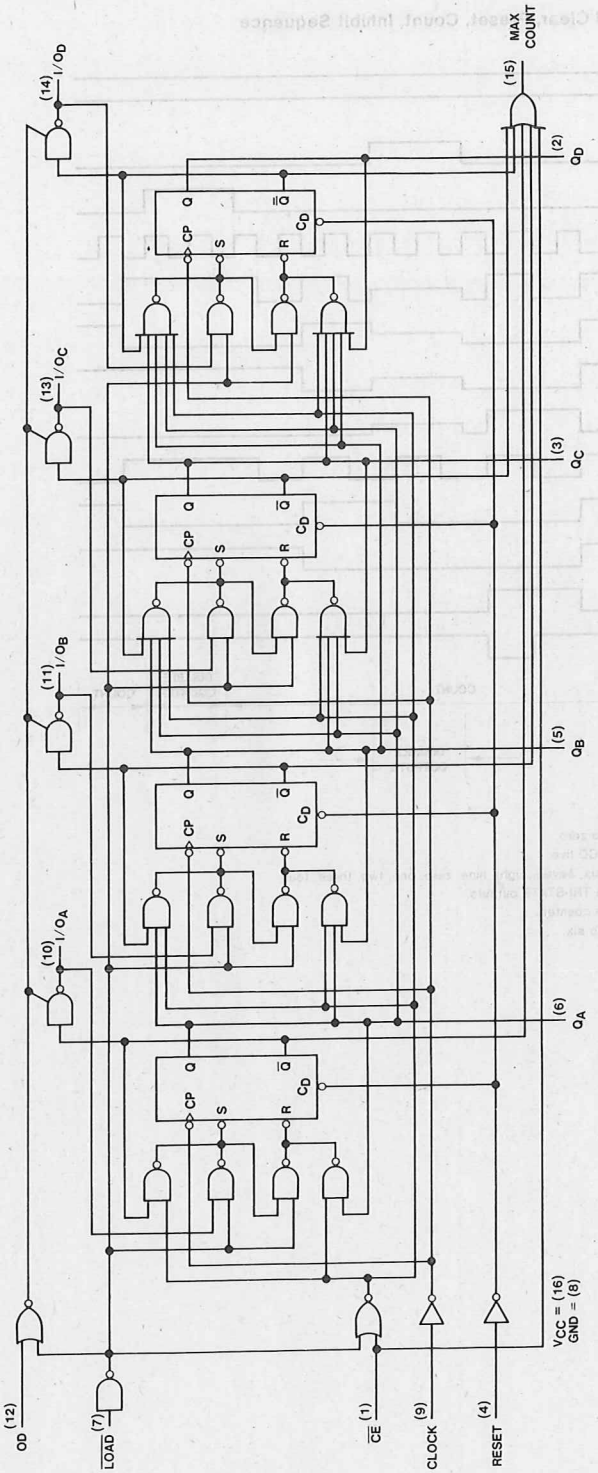
| Parameter | | | From | To | Conditions | DM75/8555, 56 Min | DM75/8555, 56 Typ | DM75/8555, 56 Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | | | | $C_L$ = 50 pF, $R_L$ = 400 Ω | 25 | 35 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock | Output | | | 15 | 22 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clock | Output | | | 34 | 44 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock | Max Count | | | 23 | 33 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clock | Max Count | | | 23 | 33 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Reset | Output | | | 30 | 44 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | | OD | Output | | | 13 | 20 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | OD | Output | | | 14 | 20 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | | OD | Output | $C_L$ = 5 pF, $R_L$ = 400 Ω | | 6 | 12 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | OD | Output | | | 12 | 20 | ns |
| $t_W$ | Minimum Pulse Width | Clock | | | | 25 | | | ns |
| | | Clear | | | | 20 | | | |
| | | Load | | | | 30 | | | |
| $t_{\overline{CE}}$ | Count Enable Time | Setup | | | | 30 | | | ns |
| | | Hold | | | | −30 | | | |
| $t_{SETUP(1)}$ | Setup Time—High Logic Level | Data | | | | 25 | | | ns |
| | | Load | | | | 30 | | | |
| $t_{HOLD(1)}$ | Hold Time—High Logic Level | Data | | | | 5 | | | ns |
| | | Load | | | | −10 | | | |
| $t_{SETUP(0)}$ | Setup Time—Low Logic Level | Data | | | | 30 | | | ns |
| | | Load | | | | 25 | | | |
| $t_{HOLD(0)}$ | Hold Time—Low Logic Level | Data | | | | 5 | | | ns |
| | | Load | | | | −10 | | | |

7

## Logic Diagrams

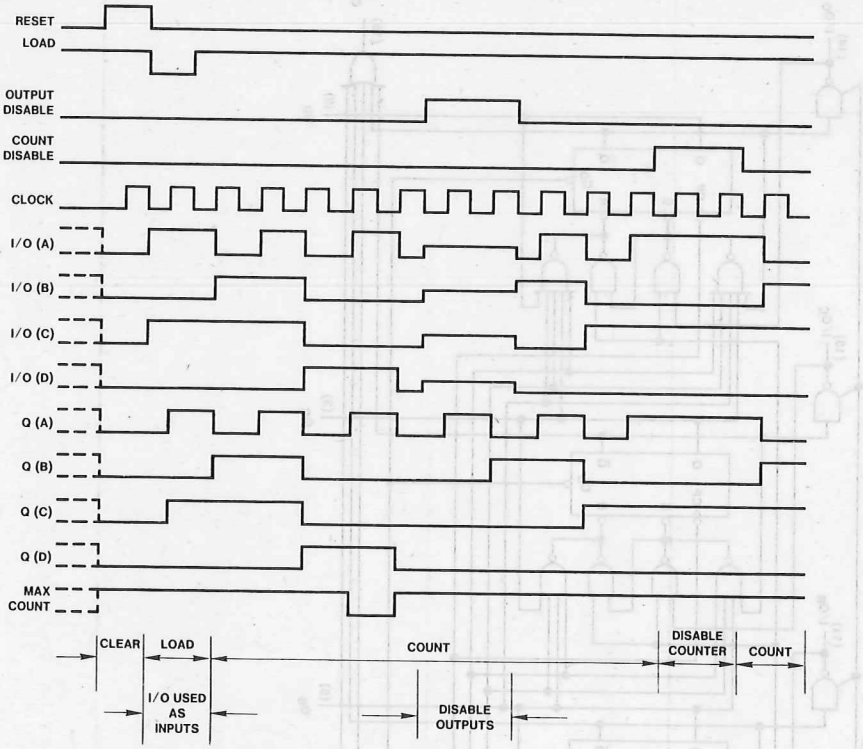


## Logic Diagrams (Continued)



## Timing Diagrams

**55 Typical Clear, Preset, Count, Inhibit Sequence**

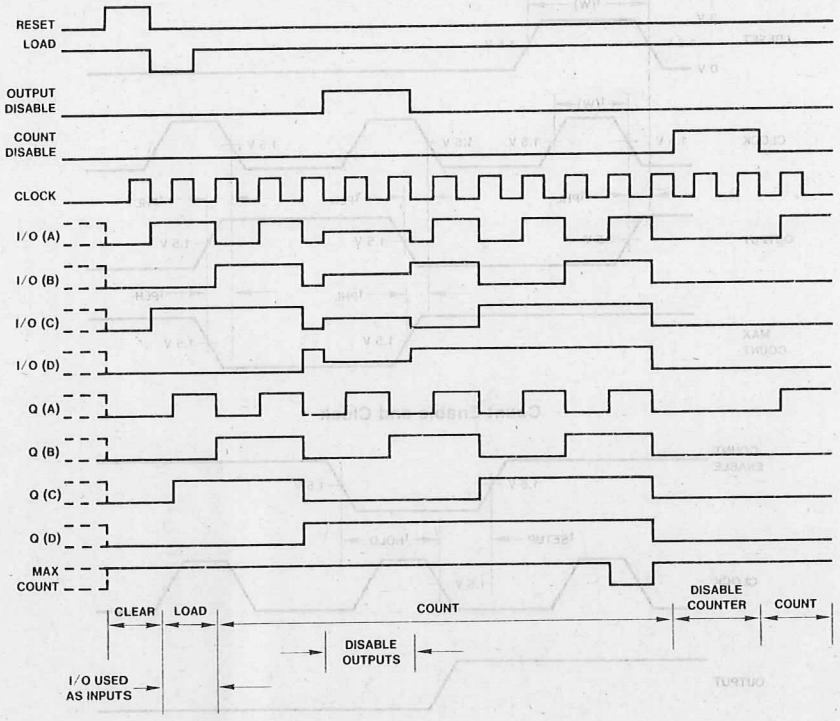



**Sequence**

(1) Clear to zero.
(2) Load BCD five.
(3) Count six, seven, eight, nine, zero, one, two, three, four.
(4) Disable TRI-STATE outputs.
(5) Disable counter.
(6) Count to six.

## Timing Diagrams (Continued)

**56 Typical Clear, Preset, Count, Inhibit Sequence**



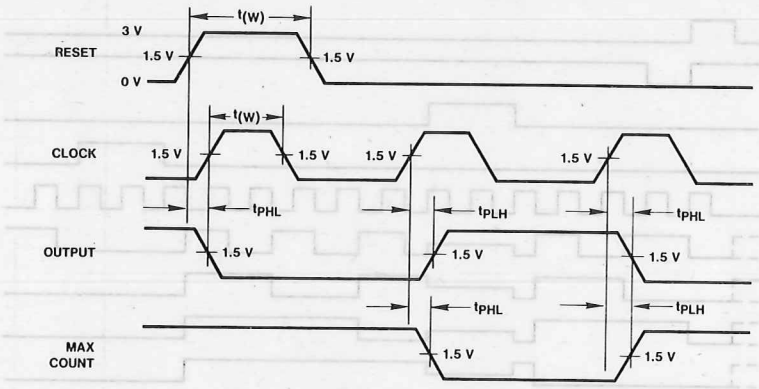

**Sequence**

(1) Clear to zero.
(2) Load binary five.
(3) Count six, seven, eight, nine, ten, eleven, twelve, thirteen, fourteen, fifteen, zero.
(4) Disable TRI-STATE outputs.
(5) Disable counter.
(6) Count to one.

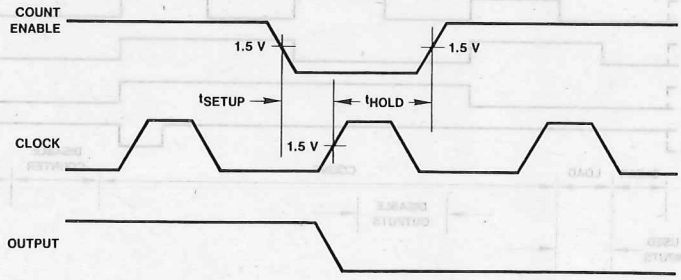
7

## Switching Time Waveforms

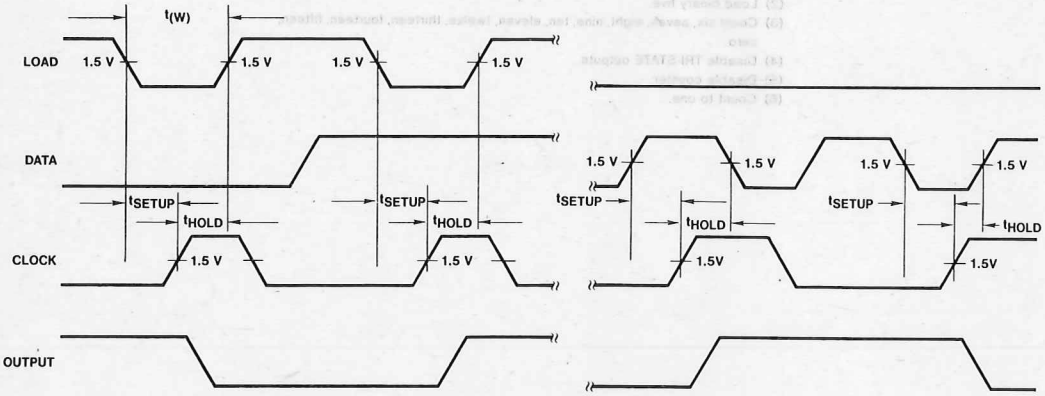
### Clock and Reset Voltage



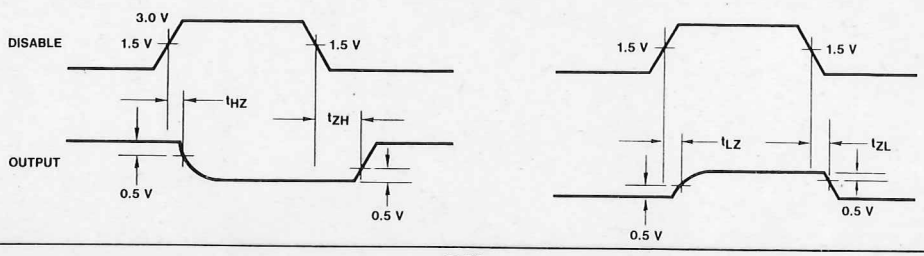

### Count Enable and Clock




### Load, Data and Clock




### Output Disable



# Synchronous 4-Bit Up/Down Decade/Binary Counters

## General Description

These circuits are synchronous up/down counters; the 60 and L60 circuits are BCD counters and the 63 and L63 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed, while the other count input is held high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

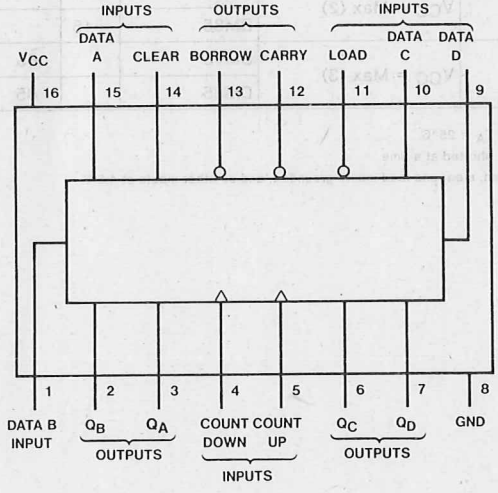
A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

## Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset for each flip-flop

| Type | Typical Count Frequency | Typical Power Dissipation |
|---|---|---|
| 60, 63 | 25 MHz | 325 mW |
| L60, L63 | 12 MHz | 40 mW |

## Connection Diagram




**7560 (J,W)**
**75L60 (J,W)**
**7563 (J,W)**
**75L63 (J,W)**

**8560 (N)**
**85L60 (N)**
**8563 (N)**
**85L63 (N)**

## Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM75/85 60, 63 | | | DM75/85 L60, L63 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | | | 0.7 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | N/A | V |
| $I_{OH}$ | High Level Output Current | | | | | −400 | | | −200 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | DM75 | | | 16 | | | 2.0 | mA |
| | | | DM85 | | | 16 | | | 3.6 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OL}$ = Max | DM75 | | | 0.4 | | 0.15 | 0.3 | V |
| | | | DM85 | | | 0.4 | | 0.2 | 0.4 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | | | 0.1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | | <1 | 10 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.3 V | | | | | −0.10 | −0.18 | mA |
| | | | $V_I$ = 0.4 V | | | −1.6 | | | | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | DM75 | −20 | | −55 | −3 | −9 | −15 | mA |
| | | | DM85 | −18 | | −55 | −3 | −9 | −15 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | DM75 | | 65 | 89 | | 8 | 13 | mA |
| | | | DM85 | | 65 | 102 | | 8 | 13 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time.

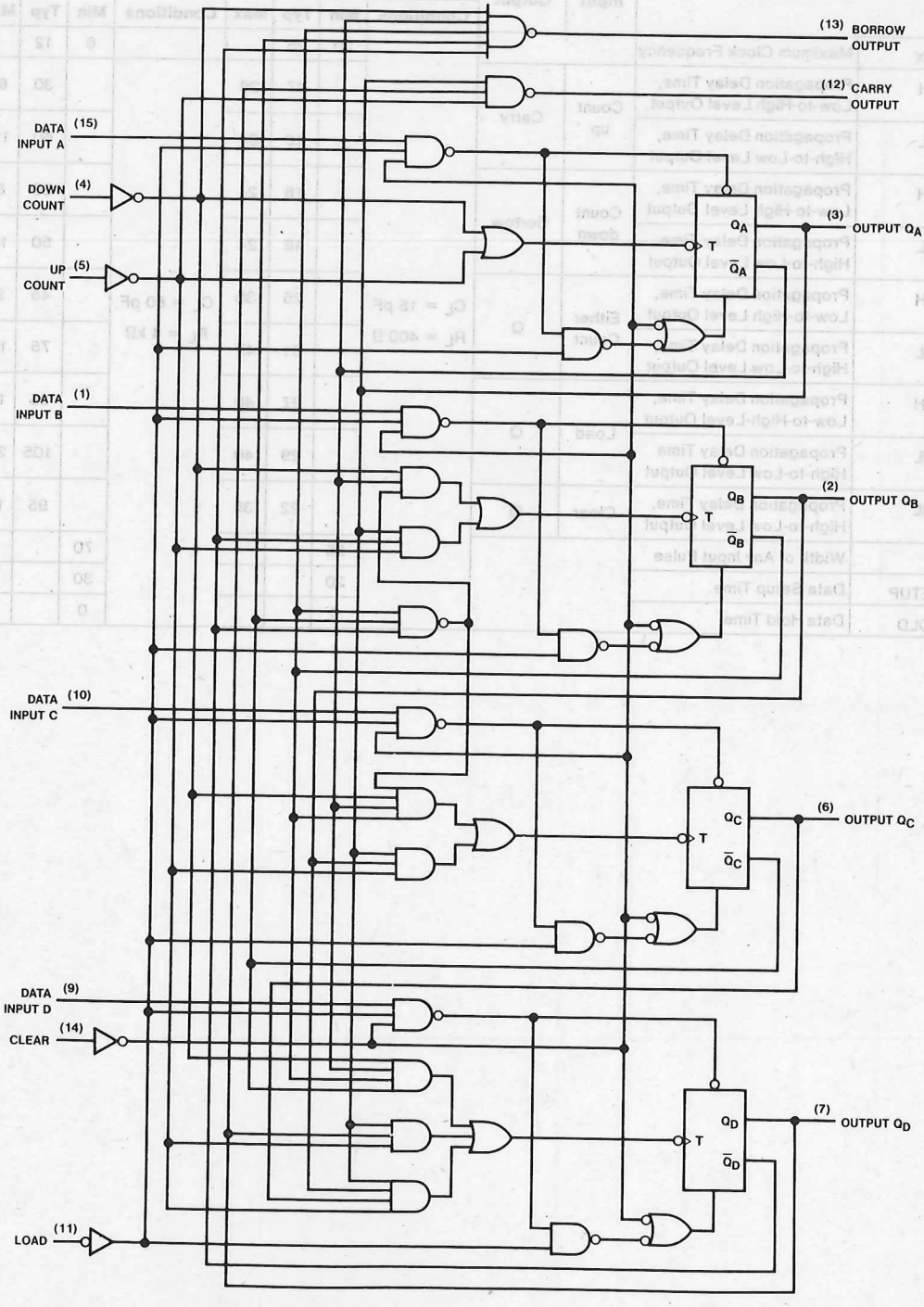
**Note 3:** $I_{CC}$ is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From Input | To Output | DM75/85 60, 63 | | | | DM75/85 L60, L63 | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Conditions | Min | Typ | Max | Conditions | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | | $C_L$ = 15 pF, $R_L$ = 400 Ω | 20 | 25 | | $C_L$ = 50 pF, $R_L$ = 4 kΩ | 6 | 12 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Count up | Carry | | | 17 | 26 | | | 30 | 60 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 16 | 24 | | | 60 | 120 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Count down | Borrow | | | 16 | 24 | | | 30 | 60 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 16 | 24 | | | 50 | 100 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Either Count | Q | | | 25 | 38 | | | 45 | 90 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 31 | 47 | | | 75 | 150 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High-Level Output | Load | Q | | | 27 | 40 | | | 55 | 110 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | | | | | 29 | 40 | | | 105 | 200 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Clear | Q | | | 22 | 35 | | | 95 | 190 | ns |
| $t_W$ | Width of Any Input Pulse | | | | 25 | | | | 70 | | | ns |
| $t_{SETUP}$ | Data Setup Time | | | | 20 | | | | 30 | | | ns |
| $t_{HOLD}$ | Data Hold Time | | | | 0 | | | | 0 | | | ns |

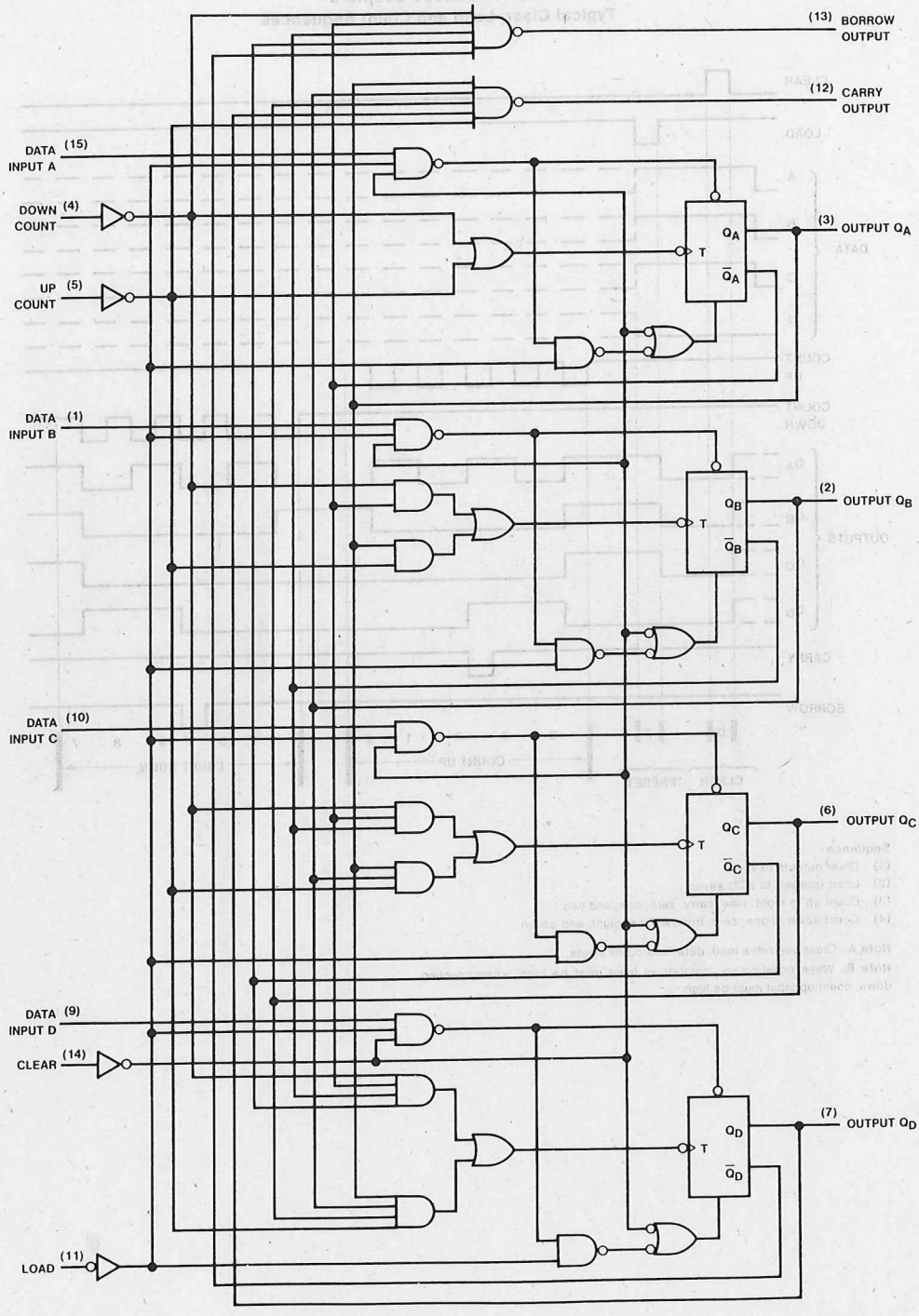
## Logic Diagrams

60, L60



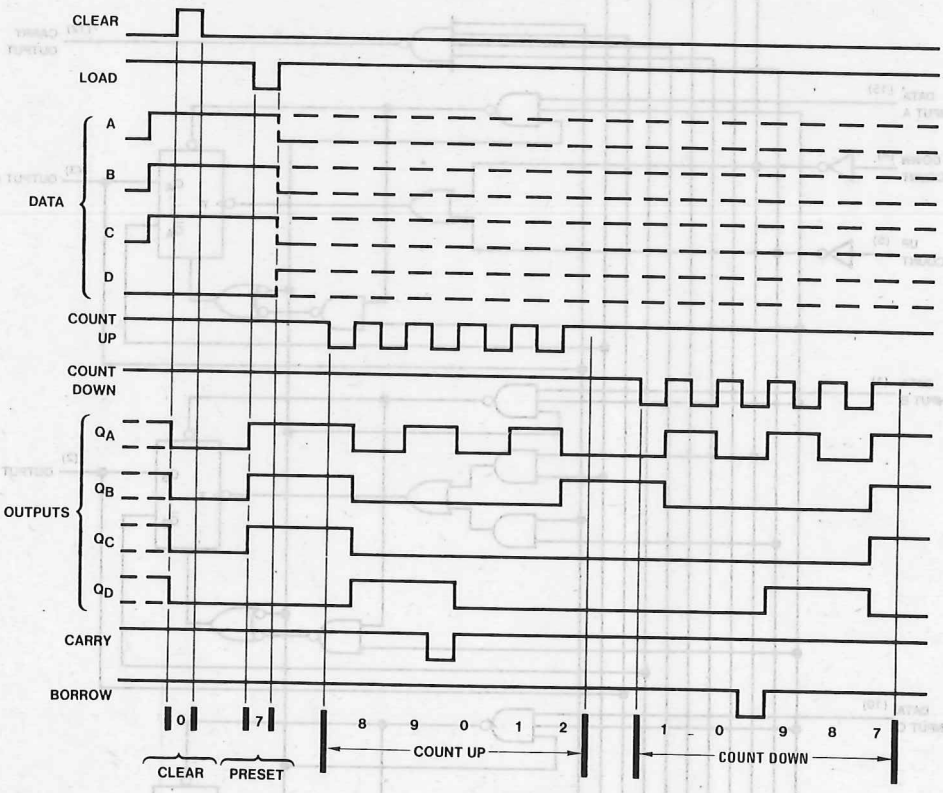
## Logic Diagrams (Continued)

**63, L63**



## Timing Diagrams

**60, L60 Decade Counters**
**Typical Clear, Load and Count Sequences**



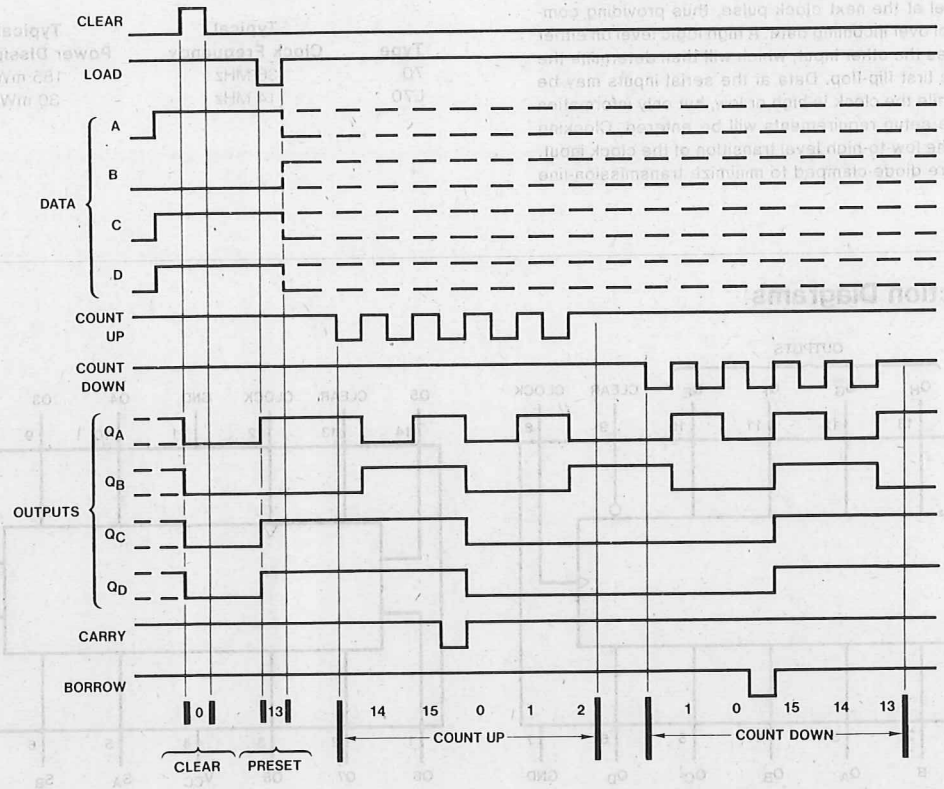

**Sequence:**
(1) Clear outputs to zero.
(2) Load (preset) to BCD seven.
(3) Count up to eight, nine, carry, zero, one, and two.
(4) Count down to one, zero, borrow, nine, eight, and seven.

**Note A:** Clear overrides load, data, and count inputs.

**Note B:** When counting up, count-down input must be high; when counting down, count-up input must be high.

## Timing Diagrams (Continued)

**63, L63 Binary Counters**
**Typical Clear, Load and Count Sequences**




**Sequence:**
(1) Clear outputs to zero.
(2) Load (preset) to binary thirteen.
(3) Count up to fourteen, fifteen, carry, zero, one, and two.
(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

**Note A:** Clear overrides load, data, and count inputs.

**Note B:** When counting up, count-down input must be high; when counting down, count-up input must be high.

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# 8-Bit Serial In/Parallel Out Shift Registers

## General Description

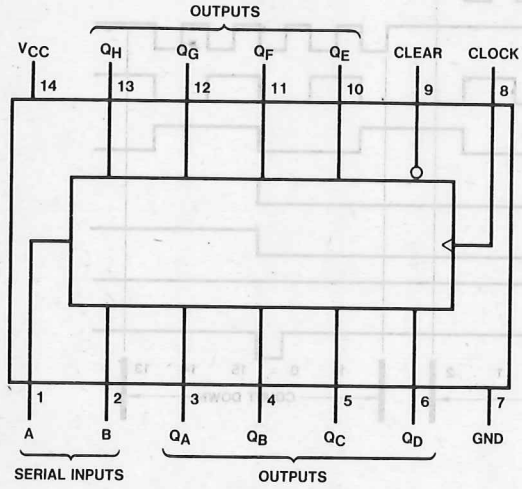
These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

## Features

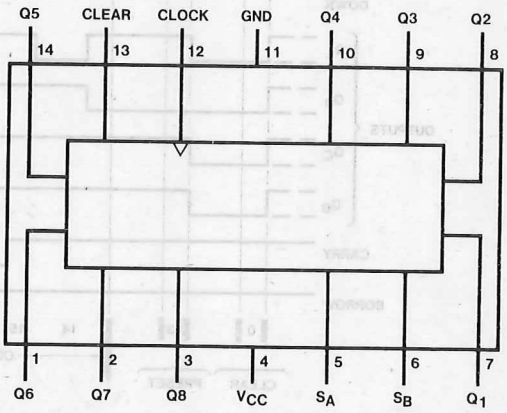
- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear

| Type | Typical Clock Frequency | Typical Power Dissipation |
|---|---|---|
| 70 | 36 MHz | 185 mW |
| L70 | 14 MHz | 30 mW |

## Connection Diagrams




7570 (J,W); 8570 (N)




76L70/86L70 (W)

## Truth Table

| Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| Clear | Clock | A | B | $Q_A$ | $Q_B$ | ... | $Q_H$ |
| L | X | X | X | L | L | ... | L |
| H | L | X | X | $Q_{A0}$ | $Q_{B0}$ | ... | $Q_{H0}$ |
| H | ↑ | H | H | H | $Q_{An}$ | ... | $Q_{Gn}$ |
| H | ↑ | L | X | L | $Q_{An}$ | ... | $Q_{Gn}$ |
| H | ↑ | X | L | L | $Q_{An}$ | ... | $Q_{Gn}$ |

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from low to high level
$Q_{A0}$, $Q_{B0}$, $Q_{H0}$ = The level of $Q_A$, $Q_B$, or $Q_H$, respectively, before the indicated steady state input conditions were established.
$Q_{An}$, $Q_{Gn}$ = The level of $Q_A$ or $Q_G$ before the most recent ↑ transition of the clock; indicates a one-bit shift.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM75/85 70 | | | DM76/86 L70 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | | | 0.7 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | N/A | V |
| $I_{OH}$ | High Level Output Current | | | | | −400 | | | −200 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | 2.4 | 3.2 | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | DM75, 76L | | | 8 | | | 2 | mA |
| | | | DM85, 86L | | | 8 | | | 3.6 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OL}$ = Max | DM75, 76L | | 0.2 | 0.4 | | | 0.3 | V |
| | | | DM85, 86L | | 0.2 | 0.4 | | | 0.4 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | Clear | | | 1 | | | 0.2 | mA |
| | | | Other | | | 1 | | | 0.1 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | Clear | | | 40 | | | 20 | μA |
| | | | Other | | | 40 | | | 10 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.3 V (DM76L, 86L) $V_I$ = 0.4 V (DM75, 85) | Clear | | | −1.6 | | | −0.36 | mA |
| | | | Other | | | −1.6 | | | −0.18 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | DM75, 76L | −10 | | −27.5 | −3 | −9 | −15 | mA |
| | | | DM85, 86L | −9 | | −27.5 | −3 | −9 | −15 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | | 37 | 54 | | 6 | 9 | mA |

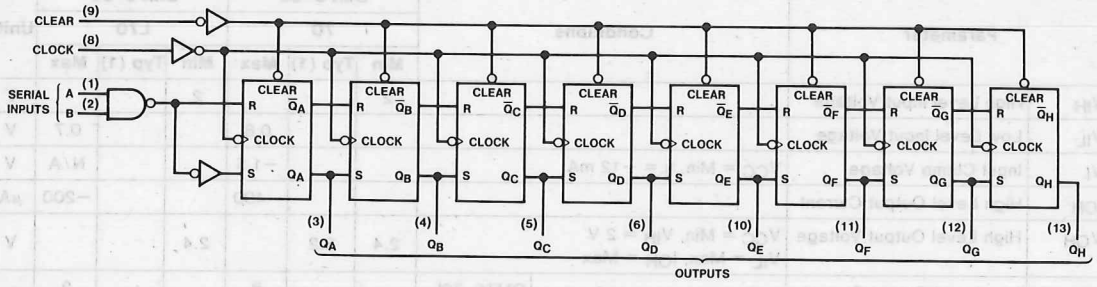
**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.
**Note 3:** $I_{CC}$ is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V, applied to clear.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | | DM75/85 70 | | | DM76/86 L70 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | $R_L$ = 800 Ω (DM75, 85) $R_L$ = 4 kΩ (DM76L, 86L) | $C_L$ = 15 pF | 25 | 36 | | 6 | 14 | | MHz |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Outputs From Clear Input | | $C_L$ = 15 pF | | 24 | 36 | | | | ns |
| | | | $C_L$ = 50 pF | | 28 | 42 | | 75 | 120 | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Outputs From Clock Input | | $C_L$ = 15 pF | 8 | 17 | 27 | | | | ns |
| | | | $C_L$ = 50 pF | 10 | 20 | 30 | | 50 | 85 | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Outputs From the Clock Input | | $C_L$ = 15 pF | 10 | 21 | 32 | | | | ns |
| | | | $C_L$ = 50 pF | 10 | 25 | 37 | | 90 | 135 | |
| $t_W$ | Width of Clock or Clear Input Pulse | | | 20 | | | 60 | 40 | | ns |
| $t_{SETUP}$ | Data Setup Time | | | 15 | | | 40 | 20 | | ns |
| $t_{HOLD}$ | Data Hold Time | | | 5 | | | 20 | −5 | | ns |

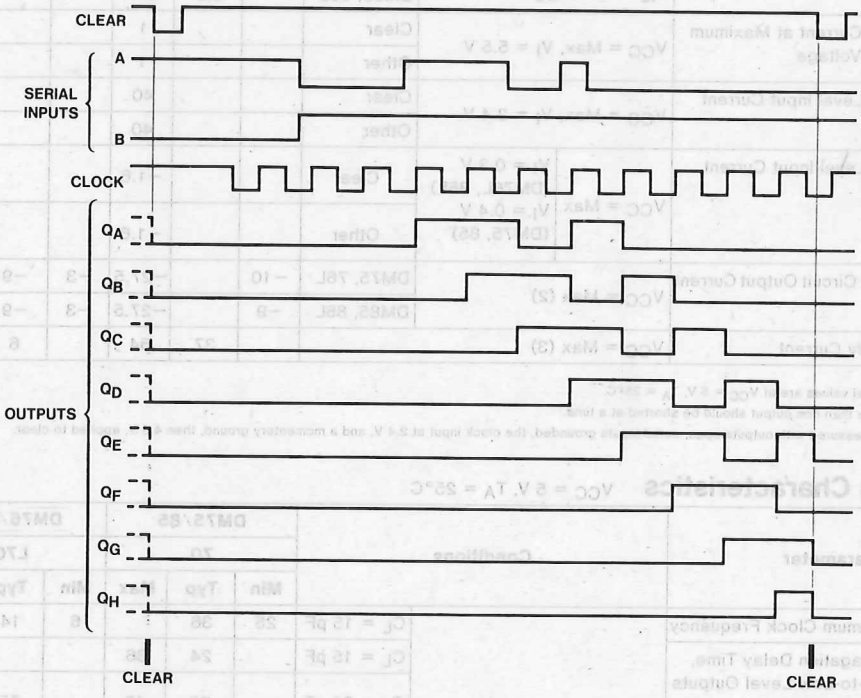
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## Logic Diagram




## Timing Diagram

**Typical Clear, Shift, and Clear Sequences**



# 8-Bit Parallel In/Serial Out Shift Registers

## General Description

These are 8-bit serial shift registers which shift the data in the direction of $Q_A$ toward $Q_H$ when clocked. Parallel-in access is made available by eight individual direct data inputs, which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

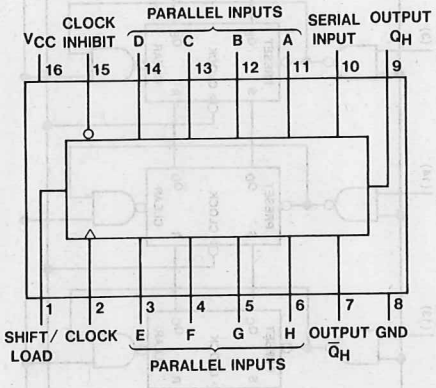
Clocking is accomplished through a 2-input NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input, regardless of the logic levels on the clock, clock inhibit, or serial inputs.

## Features

- Complementary outputs
- Direct overriding load (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion

| Type | Typical Frequency | Typical Power Dissipation |
|---|---|---|
| 90 | 20 MHz | 200 mW |
| L90 | 14 MHz | 30 mW |

## Connection Diagram




**7590 (J,W)**
**76L90 (J,W)**

**8590 (N)**
**86L90 (N)**

## Truth Table

| Inputs | | | | | Internal Outputs | | Output |
|---|---|---|---|---|---|---|---|
| Shift/ Load | Clock Inhibit | Clock | Serial | Parallel A...H | $Q_A$ | $Q_B$ | $Q_H$ |
| L | X | X | X | a...h | a | b | h |
| H | L | L | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |
| H | L | ↑ | H | X | H | $Q_{An}$ | $Q_{Gn}$ |
| H | L | ↑ | L | X | L | $Q_{An}$ | $Q_{Gn}$ |
| H | H | ↑ | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low-to-high level

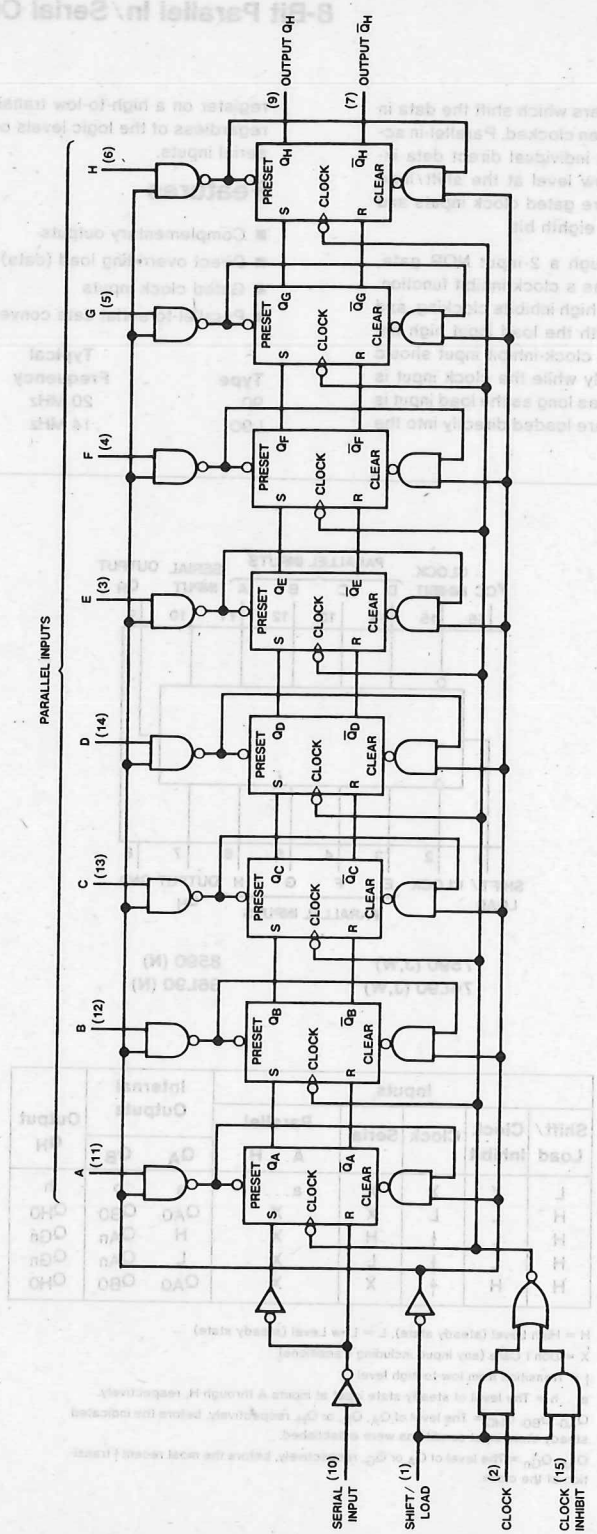
a...h = The level of steady-state input at inputs A through H, respectively.

$Q_{A0}$, $Q_{B0}$, $Q_{H0}$ = The level of $Q_A$, $Q_B$, or $Q_H$, respectively, before the indicated steady-state input conditions were established.

$Q_{An}$, $Q_{Gn}$ = The level of $Q_A$ or $Q_G$, respectively, before the most recent ↑ transition of the clock.

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## Logic Diagram



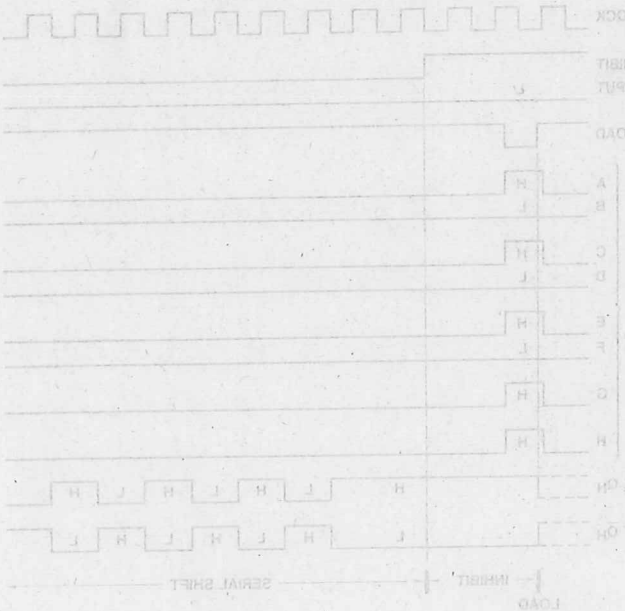
## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | DM75/85 90 | | | DM76/86 L90 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.8 | | | 0.7 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | N/A | V |
| $I_{OH}$ | High Level Output Current | | | | | | −800 | | | −200 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OH}$ = Max | | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | DM75, DM76 | | | 16 | | | 2 | mA |
| | | | | DM85, DM86 | | | 16 | | | 3.6 | |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = Max, $I_{OL}$ = Max | DM75, DM76 | | 0.2 | 0.4 | | | 0.3 | V |
| | | | | DM85, DM86 | | 0.2 | 0.4 | | | 0.4 | |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | | | 0.1 | mA |
| $I_{IH}$ | High Level Input Current | Load Input | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 80 | | | 30 | μA |
| | | Other Inputs | | | | | 40 | | | 10 | |
| $I_{IL}$ | Low Level Input Current | Load Input | $V_{CC}$ = Max | $V_I$ = 0.3 V (DM76/86) | | | −3.2 | | | −0.54 | mA |
| | | Other Inputs | | $V_I$ = 0.4 V (DM75/85) | | | −1.6 | | | −0.18 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | DM75, DM76 | −20 | | −55 | −3 | −9 | −15 | mA |
| | | | | DM85, DM86 | −18 | | −55 | −3 | −9 | −15 | |
| $V_{CC}$ | Supply Current | | $V_{CC}$ = Max (3) | | | 40 | 63 | | | 9.5 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time.

**Note 3:** With the outputs open, clock inhibit and shift/load at 4.5 V, and a clock pulse applied to the clock input, $I_{CC}$ is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

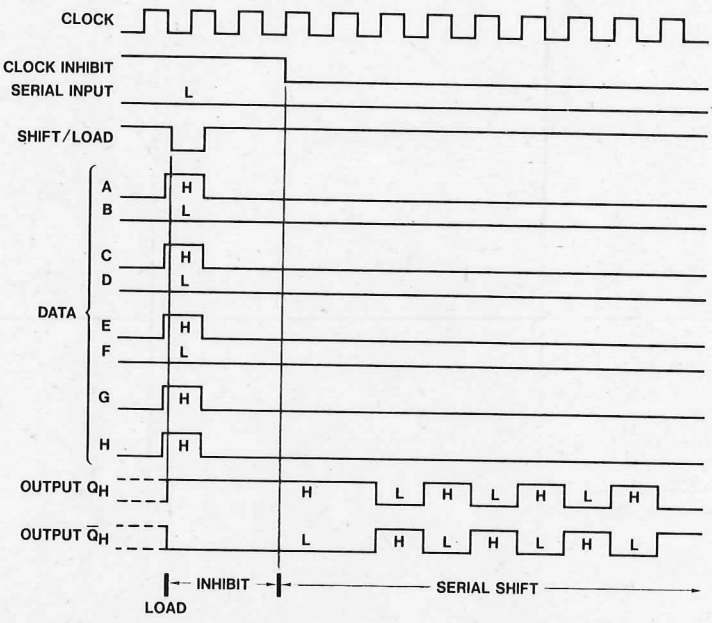


## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

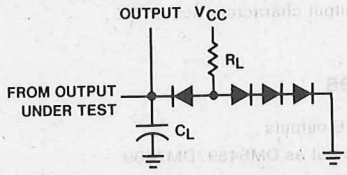
| Parameter | | From (Input) | To (Output) | DM75/85 90 Conditions | DM75/85 90 Min | DM75/85 90 Typ | DM75/85 90 Max | DM76/86 L90 Conditions | DM76/86 L90 Min | DM76/86 L90 Typ | DM76/86 L90 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | | | $C_L$ = 15 pF, $R_L$ = 400 Ω | 14 | 20 | | $C_L$ = 50 pF, $R_L$ = 4 kΩ | 6 | 14 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Load | Any | | | 34 | 50 | | | 44 | 88 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 42 | 60 | | | 62 | 124 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Clock | Any | | | 26 | 40 | | | 35 | 70 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 35 | 50 | | | 50 | 100 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | H | $Q_H$ | | | 25 | 40 | | | 33 | 66 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 36 | 50 | | | 56 | 112 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | H | $\overline{Q}_H$ | | | 25 | 40 | | | 33 | 66 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 36 | 50 | | | 56 | 112 | ns |
| $t_{W(CLOCK)}$ | Width of Clock Input Pulse | | | | 35 | 25 | | | 100 | | | ns |
| $t_{W(LOAD)}$ | Width of Load Input Pulse | | | | 35 | 24 | | | 100 | | | ns |
| $t_{SETUP}$ | Parallel Input Setup Time | | | | 25 | 10 | | | 44 | 22 | | ns |
| $t_{SETUP}$ | Serial Input Setup Time | | | | 40 | 23 | | | 44 | 22 | | ns |
| $t_{HOLD}$ | Hold Time at Any Input | | | | 5 | | | | 10 | | | ns |

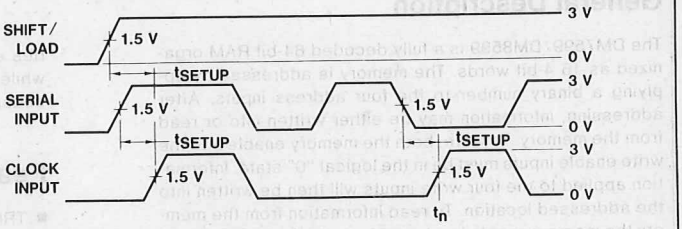
## Timing Diagram

**Typical Shift, Load and Inhibit Sequences**

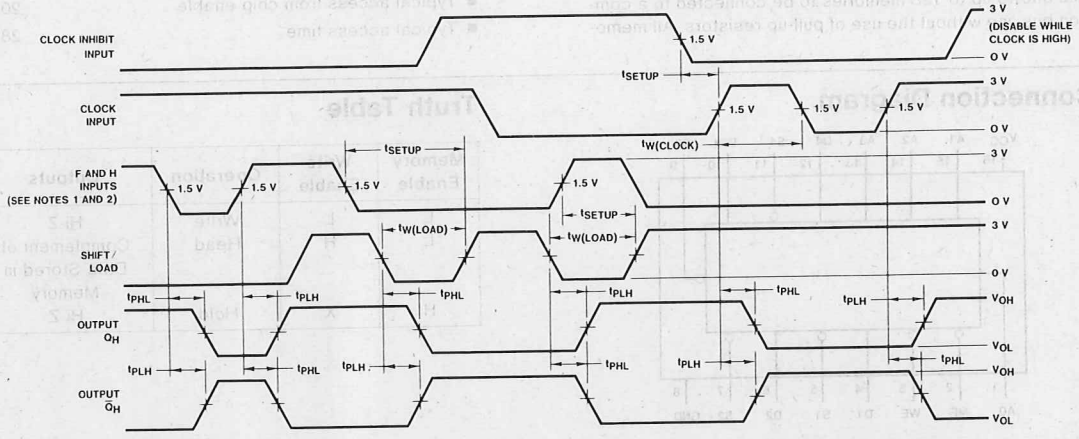


## AC Test Circuit and Switching Time Waveforms




**Note 1:** The eight data inputs and the clock inhibit input are low.
Results are monitored at output $Q_H$ at $t_n+7$.
**Note 2:** The input pulse generators have the following characteristics:
$t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR $\leq 1$ MHz, duty cycle $\leq 50\%$, $Z_{OUT} \approx 50\ \Omega$.




**Note 1:** The remaining six data inputs and the serial input are low.
**Note 2:** Prior to test, high level data is loaded into H input.
**Note 3:** The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR $\leq 1$ MHz, duty cycle $\leq 50\%$, $Z_{OUT} \approx 50\ \Omega$. When testing $f_{MAX}$, vary clock PRR.

7

# TRI-STATE® 64-Bit Random Access Memories

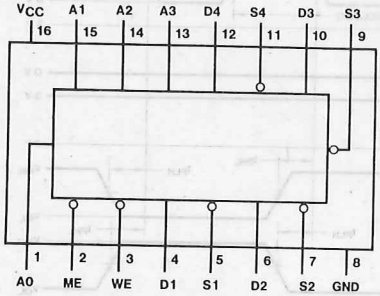
## General Description

The DM7599/DM8599 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four address inputs. After addressing, information may be either written into or read from the memory. To write, both the memory enable and the write enable inputs must be in the logical "0" state. Information applied to the four write inputs will then be written into the addressed location. To read information from the memory the memory enable input must be in the logical "0" state and the write enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the memory enable input is in the logical "1" state, the outputs will go to the high-impedance state. This allows up to 128 memories to be connected to a common bus line without the use of pull-up resistors. All memories except one are gated into the high impedance state while the one selected memory exhibits the normal low impedance output characteristics of TTL.

## Features

- TRI-STATE outputs
- Same pin-out as DM5489/DM7489
- Organized as 16, 4-bit words
- Expandable to 2048, 4-bit words without additional resistors (DM8599 only)
- Typical access from chip enable 20 ns
- Typical access time 28 ns

## Connection Diagram

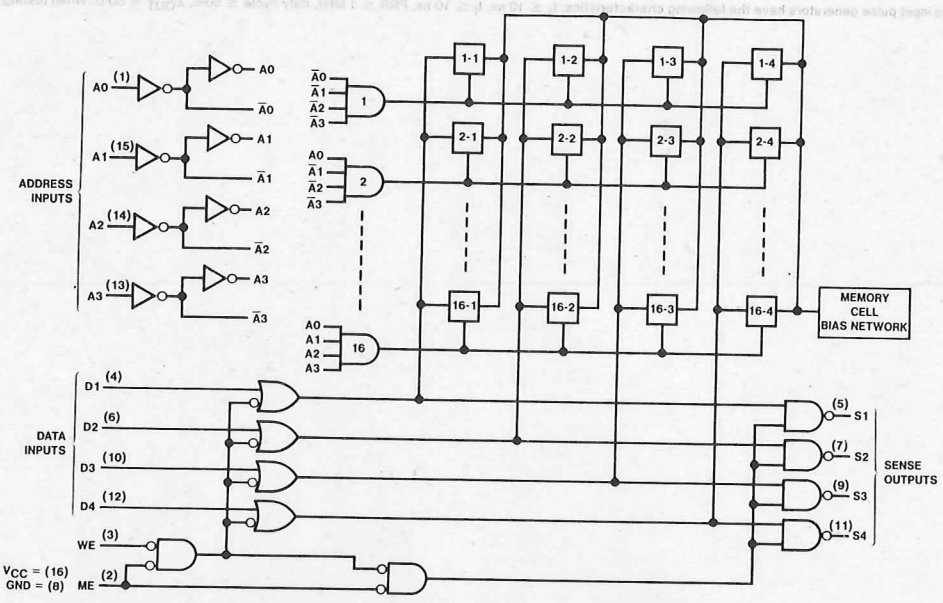



7599 (J); 8599 (N)

## Truth Table

| Memory Enable | Write Enable | Operation | Outputs |
|---|---|---|---|
| L | L | Write | Hi-Z |
| L | H | Read | Complement of Data Stored in Memory |
| H | X | Hold | Hi-Z |

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM75/85 99 Min | DM75/85 99 Typ (1) | DM75/85 99 Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | $V_{CC}$ = Min | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | $V_{CC}$ = Min | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | DM75 | | | −2.0 | mA |
| | | | DM85 | | | −5.2 | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | | | 2.4 | V |
| $I_{OL}$ | Low Level Output Current | | | | | 12 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 12 mA | | | | 0.4 | V |
| $I_{O(OFF)}$ | Off State (High Impedance State) Output Current | $V_{CC}$ = Max | $V_O$ = 0.4 V | | | −40 | μA |
| | | | $V_O$ = 2.4 V | | | 40 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −30 | | −70 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | 80 | 120 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.

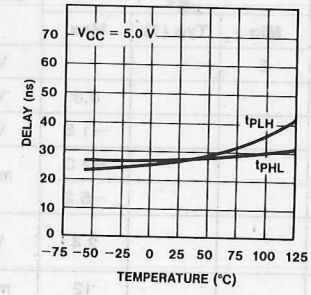
## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | To (Output) | Conditions | DM75/85 99 Min | DM75/85 99 Typ | DM75/85 99 Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Address | Output | $C_L$ = 50 pF, $R_L$ = 400 Ω | | 27 | 45 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Address | Output | | | 28 | 45 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | | ME | Output | | | 14 | 20 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | ME | Output | | | 19 | 30 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | | ME | Output | $C_L$ = 5 pF, $R_L$ = 400 Ω | | 12 | 20 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | ME | Output | | | 21 | 30 | ns |
| $t_{SETUP}$ | Setup Time | Address | | | | 0 | 17 | | ns |
| | | Data | | | | 0 | −15 | | ns |
| $t_{HOLD}$ | Hold Time | Address | | | | 5 | −7 | | ns |
| | | Data | | | | 0 | −14 | | ns |
| $t_{WP}$ | Write Enable Pulse Width | | | | | 40 | 23 | | ns |
| $t_{SR}$ | Sense Recovery Time | | | | | | 42 | 60 | ns |

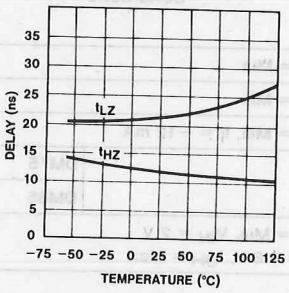
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## Typical Performance Curves

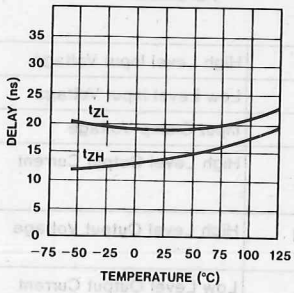
Delay From Address To Output



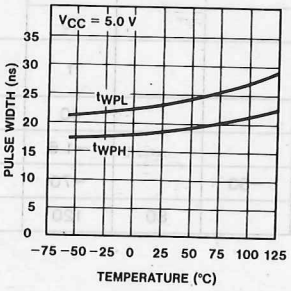

Delay From Enable To High Impedance State



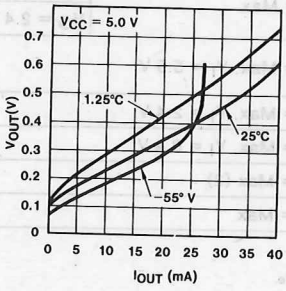

Delay From Enable To Low Impedance State



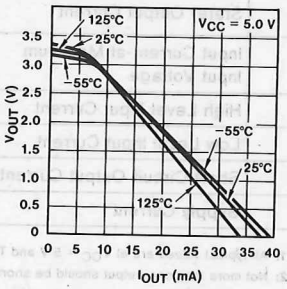

Minimum Write Pulse Width



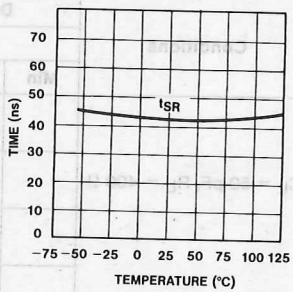

Logical "0" Output Voltage vs Sink Current



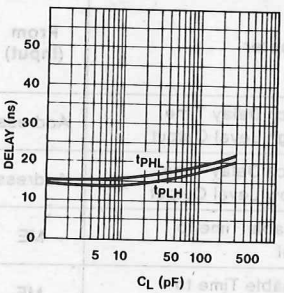

Logical "1" Output Voltage vs Source Current




Sense Recovery Time

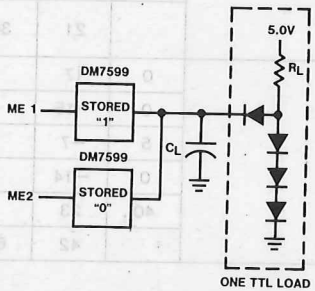



Delay From Enable To Output vs Load Capacitance



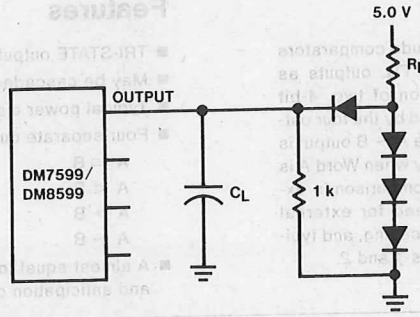

## Test Circuit

Test Circuit For Delay Vs Load Capacitance

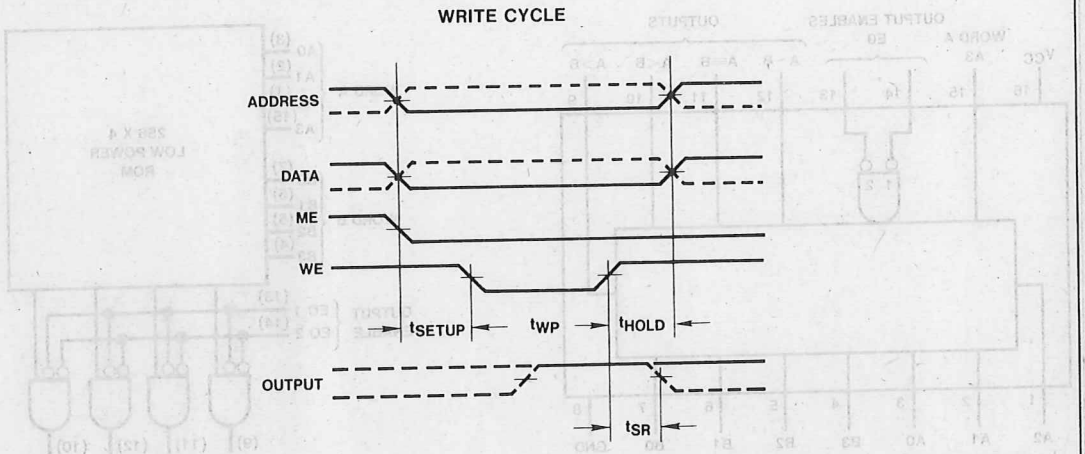


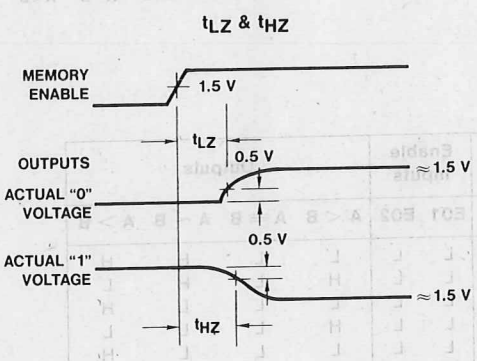

**Note:** In a typical application the output of the TRI-STATE memories might be wired together and one would be switching to the low impedance state at the same time the circuit previously selected would be switching back into the high impedance state. The measurements of delay versus load capacitance were made under conditions which simulate actual operating conditions in an application. (See test circuit.)

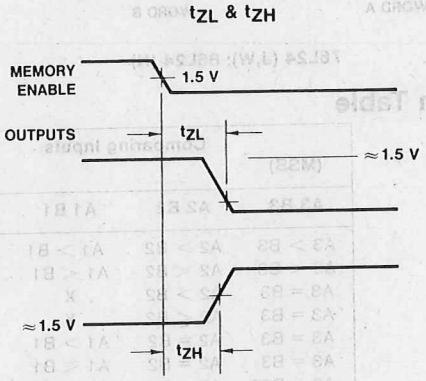
## AC Test Circuit




## Switching Time Waveforms




**Note:** The pulse generator has the following characteristics: V = 3.0 V, $t_r$ = 15 ns, $t_f$ = 5.0 ns, f = 500 kHz, duty cycle = 50%, $Z_{OUT}$ = 50 Ω, $V_t$ = 1.3 V @ 25°C.

# TRI-STATE® Magnitude Comparators with A almost equal B

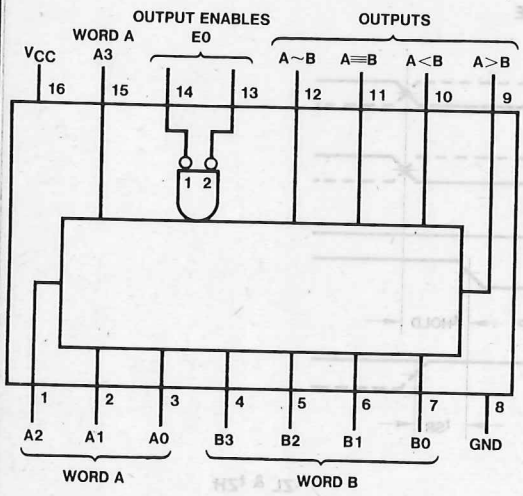
## General Description

These circuits are low power, 4-bit, magnitude comparators which provide both standard totem-pole TTL outputs as well as TRI-STATE outputs. A comparison of two, 4-bit words is performed, and the result indicated by the four outputs: A > B, A < B, A ≡ B, and A ~ B. The A ~ B output is unique with this device, and is enabled only when Word A is within one binary count of Word B. The comparison is expandable to any number, without the need for external gates. The maximum speed method of cascading, and typical comparison times are shown in *Figures 1* and *2*.

## Features

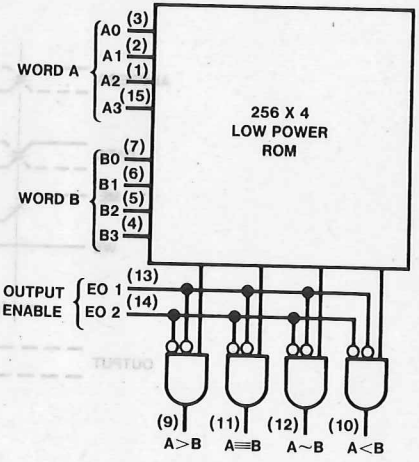
- TRI-STATE outputs
- May be cascaded to compare words of greater length
- Typical power dissipation 75 mW
- Four separate outputs
  - A ≡ B
  - A < B
  - A > B
  - A ~ B
- A almost equal to B (A ~ B) output permits look-ahead and anticipation of a match (A ≡ B)

## Connection Diagram




76L24 (J,W); 86L24 (N)

## Logic Diagram




## Truth Table

| Comparing Inputs (MSB) | | | (LSB) | Enable Inputs | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|
| A3 B3 | A2 B2 | A1 B1 | B0 B0 | E01 | E02 | A < B | A ≡ B | A ~ B | A > B |
| A3 > B3 | A2 > B2 | A1 > B1 | A0 > B0 | L | L | L | L | H | H |
| A3 < B3 | A2 < B2 | A1 < B1 | A0 < B0 | L | L | H | L | H | L |
| A3 = B3 | A2 > B2 | X | X | L | L | L | L | L | H |
| A3 = B3 | A2 < B2 | X | X | L | L | H | L | L | L |
| A3 = B3 | A2 = B2 | A1 > B1 | X | L | L | L | L | L | H |
| A3 = B3 | A2 = B2 | A1 < B1 | X | L | L | H | L | L | L |
| A3 = B3* | A2 = B2 | A1 = B1 | A0 > B0 | L | L | L | L | H | H |
| A3 = B3** | A2 = B2 | A1 = B1 | A0 < B0 | L | L | H | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | L | L | H | L | L |
| X | X | X | X | H | X | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| X | X | X | X | X | H | Hi-Z | Hi-Z | Hi-Z | Hi-Z |

*Word A > Word B By 1

**Word A < Word B By 1

H = High Level, L = Low Level, X = Don't Care

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM76 L24 | | | DM86 L24 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.7 | | | 0.7 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −1.0 | | | −1.0 | mA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.7 V, $I_{OH}$ = −1.0 mA | | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 2.0 | | | 3.6 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.7 V, $I_{OL}$ = Max | | | | 0.3 | | | 0.4 | V |
| $I_{O(OFF)}$ | Off State (High Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.7 V | $V_O$ = 0.3 V | | | −40 | | | −40 | μA |
| | | | $V_O$ = 2.4 V | | | 40 | | | 40 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_{IH}$ = 5.5 V | | | | 100 | | | 100 | μA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 10 | | | 10 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.3 V | | | | −180 | | | −180 | μA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −6 | | −30 | −6 | | −30 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max, $V_I$ = 0 V | | | 15 | 20 | | 15 | 20 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From | To | Conditions | DM76L/86L L24 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Output | $C_L$ = 50 pF, $R_L$ = 4 kΩ | | 86 | 130 | ns |
| $t_{PHL}$ | PropagationDelay Time, High-to-Low Level Output | Data | Output | | | 55 | 85 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | Output Enable | Output | | | 34 | 51 | ns |
| $T_{ZL}$ | Output Enable Time to Low Level | Output Enable | Output | | | 47 | 70 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | Output Enable | Output | $C_L$ = 5 pF, $R_L$ = 4 kΩ | | 15 | 23 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | Output Enable | Output | | | 57 | 86 | ns |

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## Typical Applications

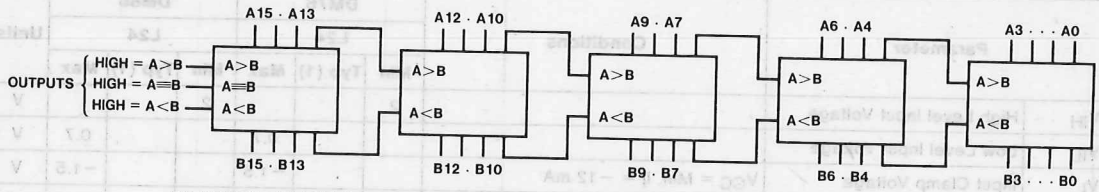



FIGURE 1. 16-BIT Comparator, Maximum Logic Expansion (Not Suitable for A ~ B)

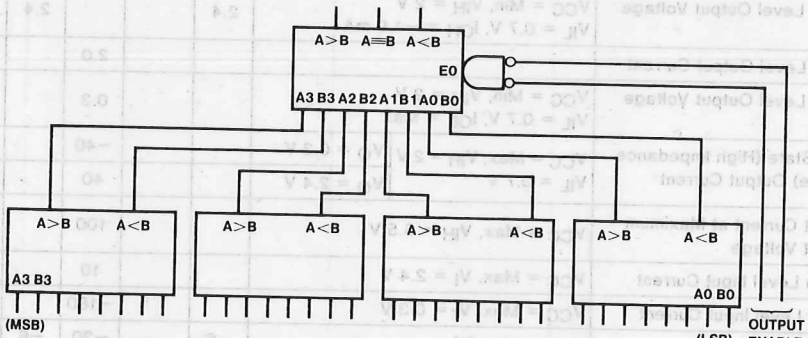
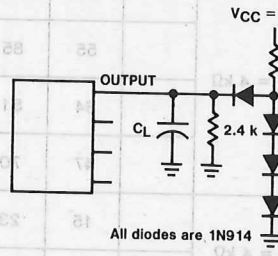
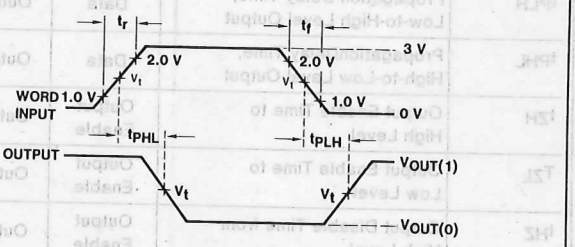


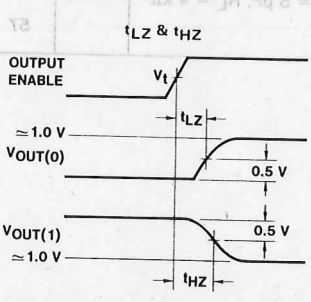

FIGURE 2. Maximum Speed Expansion (Not Suitable for A ~ B)

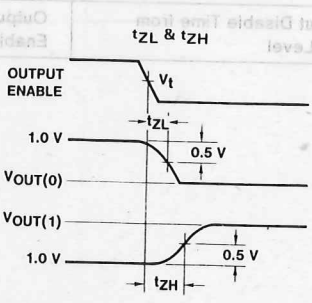
| Compare *(Figure 2)* | Circuit Delay | Number Of Circuits |
|---|---|---|
| 1-4 Bits | 1 Delay | 1 |
| 5-7 Bits | 2 Delays | 2 |
| 8-10 Bits | 2 Delays | 3 |
| 11-13 Bits | 2 Delays | 4 |
| 14-16 Bits | 2 Delays | 5 |

## AC Test Circuit and Switching Time Waveforms




**Note:** The pulse generator has the following characteristics: V = 3.0 V, $t_r$ = 15 ns, $t_f$ = 5.0 ns, f = 500 kHz, duty cycle = 50%, $Z_{OUT}$ = 50 Ω, $V_t$ = 1.3 V @ 25°C.

# TRI-STATE® 7-Segment to BCD Decoder

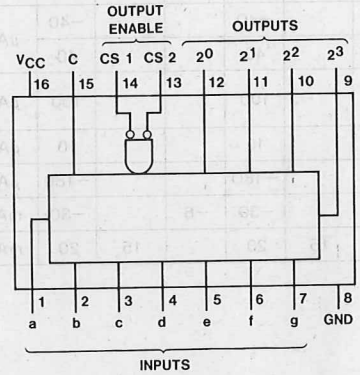
## General Description

These circuits are low power converters which accept 7-segment data on the inputs, and provide binary-coded decimal (BCD) data on the outputs. An input control line is also provided, in the event that the 7-segment input data is presented in inverted form. The BCD outputs are normally of the standard totem-pole TTL type, however they may also be converted to high-impedance (TRI-STATE) types by applying a high logic level to either of the two output enable pins.

## Features

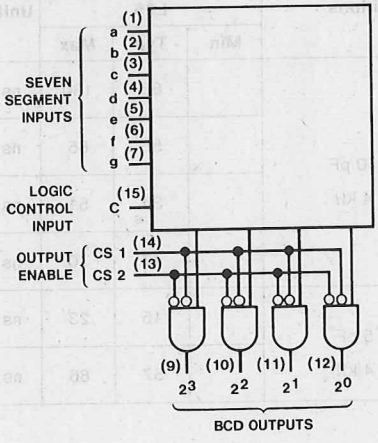
- TRI-STATE outputs
- Typical power dissipation — 75 mW
- Typical propagation delay — 70 ns

## Connection Diagram




76L25(J,W); 86L25 (N)

## Logic Diagram




## Segment Identification




## Truth Table

| Digit | a | b | c | d | e | f | g | CTL | CS 1 | CS 2 | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | H | H | H | H | H | H | L | H | L | L | L | L | L | L |
| 1 | L | H | H | L | L | L | L | H | L | L | L | L | L | H |
| 2 | H | H | L | H | H | L | H | H | L | L | L | L | H | L |
| 3 | H | H | H | H | L | L | H | H | L | L | L | L | H | H |
| 4 | L | H | H | L | L | H | H | H | L | L | L | H | L | L |
| 5 | H | L | H | H | L | H | H | H | L | L | L | H | L | H |
| 6 | L | L | H | H | H | H | H | H | L | L | L | H | H | L |
| 7 | H | L | H | H | H | H | H | H | L | L | L | H | H | L |
| 8 | H | H | H | L | L | L | L | H | L | L | L | H | H | H |
| 9 | H | H | H | H | H | H | H | H | L | L | H | L | L | L |
| 9 | H | H | H | L | L | H | H | H | L | L | H | L | L | H |
| BLANK | L | L | L | L | L | L | L | H | L | L | H | H | H | H |
| L | L | L | L | H | H | H | L | H | L | L | H | H | L | H |
| E | H | L | L | H | H | H | H | H | L | L | H | H | H | L |
| A | H | H | H | L | H | H | H | H | L | L | H | L | H | L |
| P | H | H | L | L | H | H | H | H | L | L | H | L | H | H |
| - | L | L | L | L | L | L | H | H | L | L | H | H | L | L |
| 0 | L | L | L | L | L | L | H | L | L | L | L | L | L | L |
| 1 | H | L | L | H | H | H | H | L | L | L | L | L | L | H |
| 2 | L | L | H | L | L | H | L | L | L | L | L | L | H | L |
| 3 | L | L | L | L | H | H | L | L | L | L | L | L | H | H |
| 4 | H | L | L | H | H | L | L | L | L | L | L | H | L | L |
| 5 | L | H | L | L | H | L | L | L | L | L | L | H | L | H |
| 6 | H | H | L | L | L | L | L | L | L | L | L | H | H | L |
| 6 | L | H | L | L | L | L | L | L | L | L | L | H | H | L |
| 7 | L | L | L | H | H | H | H | L | L | L | L | H | H | H |
| 8 | L | L | L | L | L | L | L | L | L | L | H | L | L | L |
| 9 | L | L | L | H | H | L | L | L | L | L | H | L | L | H |
| 9 | L | L | L | L | H | L | L | L | L | L | H | L | L | H |
| BLANK | H | H | H | H | H | H | H | L | L | L | H | H | H | H |
| L | H | H | H | L | L | L | H | L | L | L | H | H | L | H |
| E | L | H | H | L | L | L | L | L | L | L | H | H | H | L |
| A | L | L | L | H | L | L | L | L | L | L | H | L | H | L |
| P | L | L | H | H | L | L | L | L | L | L | H | L | H | H |
| - | H | H | H | H | H | H | L | L | L | L | H | H | L | L |
| | X | X | X | X | X | X | X | X | H | X | Z | Z | Z | Z |
| | X | X | X | X | X | X | X | X | X | H | Z | Z | Z | Z |
| | All Other Input Combinations | | | | | | | | L | L | H | H | H | H |

H = High Level (Steady State)
L = Low Level (Steady State)
Z = High Impedance
X = Don't Care

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## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM76 L25 | | | DM86 L25 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.7 | | | 0.7 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −1.0 | | | −1.0 | mA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.7 V, $I_{OH}$ = −1.0 mA | | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 2.0 | | | 3.6 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.7 V, $I_{OL}$ = Max | | | | 0.3 | | | 0.4 | V |
| $I_{O(OFF)}$ | Off State (High Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.7 V | $V_O$ = 0.3 V | | | −40 | | | −40 | μA |
| | | | $V_O$ = 2.4 V | | | 40 | | | 40 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 100 | | | 100 | μA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 10 | | | 10 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.3 V | | | | −180 | | | −180 | μA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −6 | | −30 | −6 | | −30 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max, $V_I$ = 0 V | | | 15 | 20 | | 15 | 20 | mA |

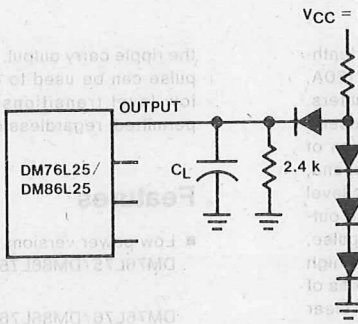
**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time.

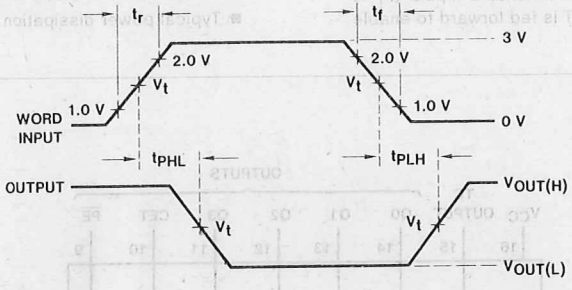
## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

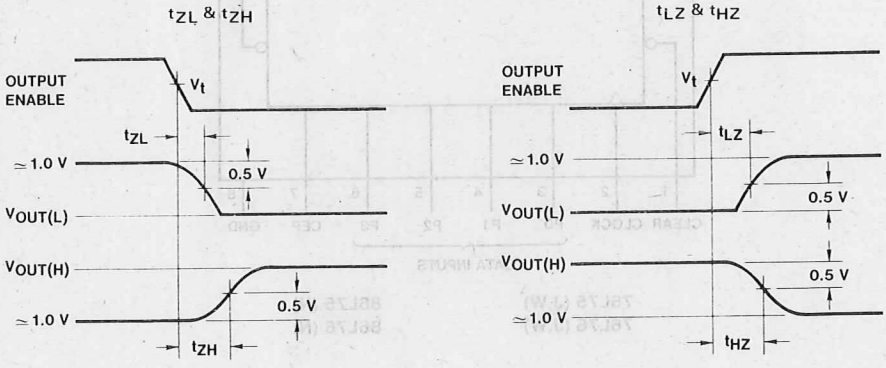
| Parameter | | From (Input) | To (Output) | Conditions | DM76/86 L25 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Output | $C_L$ = 50 pF, $R_L$ = 4 kΩ | | 86 | 130 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Data | Output | | | 55 | 85 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | | | | | 34 | 51 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | | | 47 | 70 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | | | $C_L$ = 5 pF, $R_L$ = 4 kΩ | | 15 | 23 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | | | | 57 | 86 | ns |

## AC Test Circuit




## Switching Time Waveforms




**Note:** The pulse generator has the following characteristics: V = 3.0 V, $t_r$ = 15 ns, $t_f$ = 5.0 ns, F = 500 kHz, duty cycle = 50%, $Z_{OUT}$ = 50Ω, $V_t$ = 1.3 V @ 25°C.

# Presettable Decade/Binary Counters

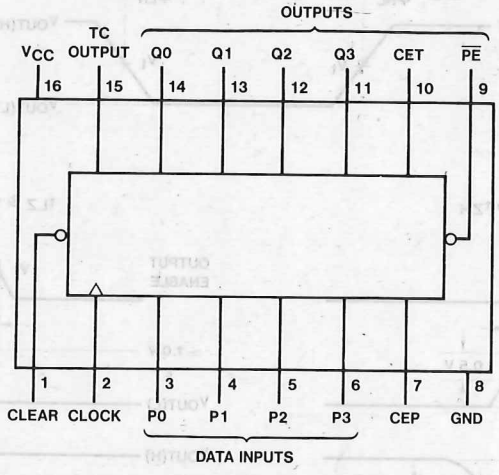
## General Description

These synchronous, presettable counters are true tenth-power versions of the popular DM54160A/DM74160A, DM54161A/DM74161A, DM9310, and DM9316 counters. They feature an internal carry/look ahead for high-speed cascading, and trigger on the positive-going transition of the clock pulse. The counters are fully programmable; and, since presetting is synchronous, applying a low logic level to the load input disables the counter and forces the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs. Low-to-high transitions at the load inputs are acceptable, regardless of the logic levels on the clock or enable inputs. The clear (reset) function is asynchronous, and a low level applied to the clear input sets all four outputs low regardless of the levels on the clock, load, or enable inputs. In high-speed cascading arrangements, both count-enable inputs (P, T) must be high to count, and input T is fed forward to enable the ripple carry output. This high-level overflow ripple carry pulse can be used to enable successive stages. High-to-low level transitions at the P or T enable inputs are permitted, regardless of the logic level on the clock.

## Features

- Low power versions popular counters
  - DM76L75/DM86L75 = DM54160A/DM74160A, DM9310—decade counter
  - DM76L76/DM86L76 = DM54161A/DM74161A, DM9316—binary counter
- Internal look-ahead for fast cascading
- Counters are fully synchronous and presettable
- Typical power dissipation 33 mW

## Connection Diagram




**76L75 (J,W)** **86L75 (N)**
**76L76 (J,W)** **86L76 (N)**

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM76 L75, L76 | | | DM86 L75, L76 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.7 | | | 0.7 | V |
| $I_{OH}$ | High Level Output Current | | | | | −200 | | | −200 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.7 V, $I_{OH}$ = −200 μA | | 2.4 | 3.1 | | 2.4 | 3.1 | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 2.0 | | | 3.6 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.7 V, $I_{OL}$ = Max | | | 0.2 | 0.3 | | 0.2 | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | CET Input | | | 200 | | | 200 | μA |
| | | | Others | | | 100 | | | 100 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | CET Input | | | 20 | | | 20 | μA |
| | | | Others | | | 10 | | | 10 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.3 V | CET Input | | | −360 | | | −360 | μA |
| | | | Others | | | −180 | | | −180 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −3 | −9 | −15 | −3 | −9 | −15 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | 6.5 | 9 | | 6.5 | 9 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.

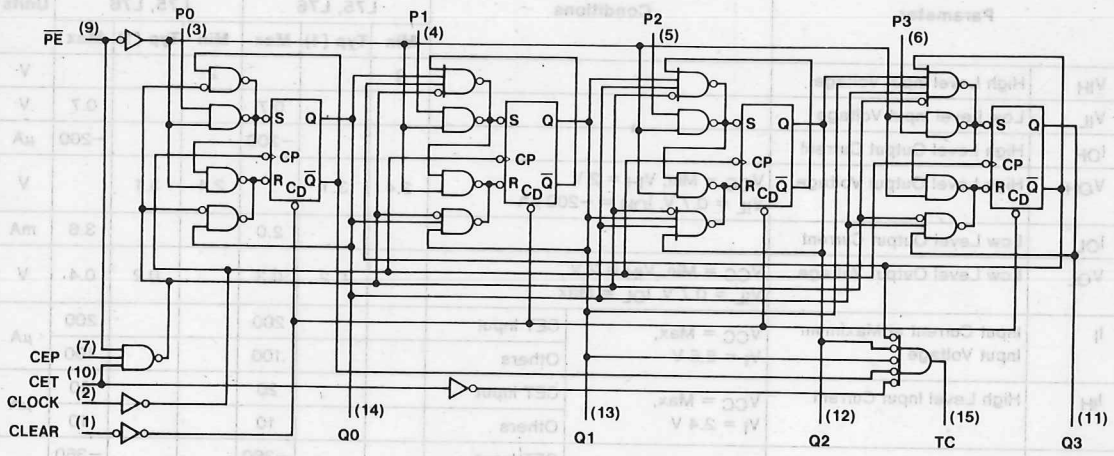
## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | To (Output) | Conditions | DM76/86 L75, L76 Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | | | | $C_L$ = 50 pF, $R_L$ = 4 kΩ | 6 | 13 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock | Q Output | | | 45 | 75 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clock | Q Output | | | 65 | 110 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock | TC Output | | | 70 | 115 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clock | TC Output | | | 85 | 140 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | CET | TC Output | | | 35 | 60 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | CET | TC Output | | | 35 | 60 | ns |
| $t_{W(CLOCK)}$ | Minimum Pulse Width | | | | | 60 | 25 | | ns |
| $t_{W(RESET)}$ | Minimum Pulse Width | | | | | 80 | 30 | | ns |
| $t_{SETUP}$ | Setup Time | CE | | | | 65 | 40 | | ns |
| | | P Inputs | | | | 30 | 15 | | |
| | | Parallel Entry | | | | 65 | 40 | | |
| $t_{HOLD}$ | Hold Time | CE | | | | 80 | 50 | | ns |
| | | P Inputs | | | | 30 | 15 | | |
| | | Parallel Entry | | | | 65 | 40 | | |

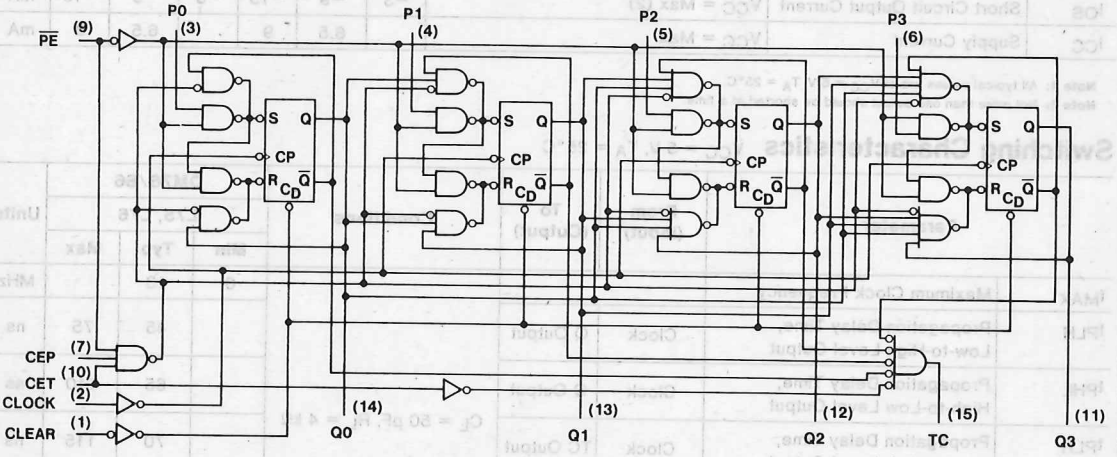
7

## Logic Diagrams

76L75/86L75 (Decade)




76L76/86L76 (Binary)




$V_{CC}$ = (16)
GND = (8)

# TRI-STATE® 7 by 9 Character Generators

## General Description

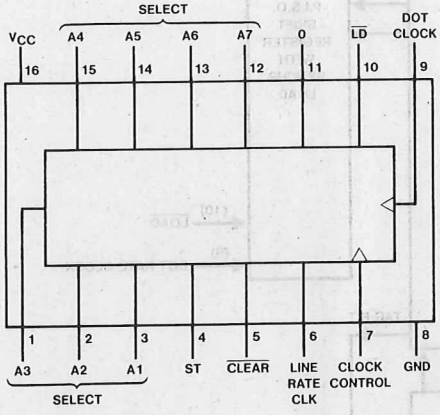
The DM7678/8678 and DM7679/DM8679 are bipolar character generators. A maximum of 64 characters can be displayed in a 7 x 9 dot matrix. Shifted characters can be generated by the on-chip subtractor. On-chip line counter and parallel-in-serial-out shift register reduce package pin-out.

The clear input and the load input are active low. $\overline{\text{Load}}$ is synchronous with the Dot Rate Clock. Both the line rate clock and the dot rate clock are positive triggered. When the strobe input receives a low signal, the character address will be held at the inputs.

## Features

- TRI-STATE outputs
- On-chip input latches
- On-chip line counter
- On-chip shift register
- Serial output
- 20 MHz typical clock rate
- Shifted characters

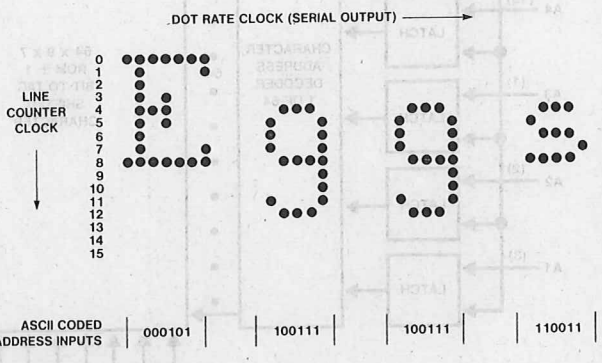
## Connection Diagram




**7678 (J)**
**7679 (J)**

**8678 (J,N)**
**8679 (J,N)**

## Character Display Example




## Electrical Characteristics

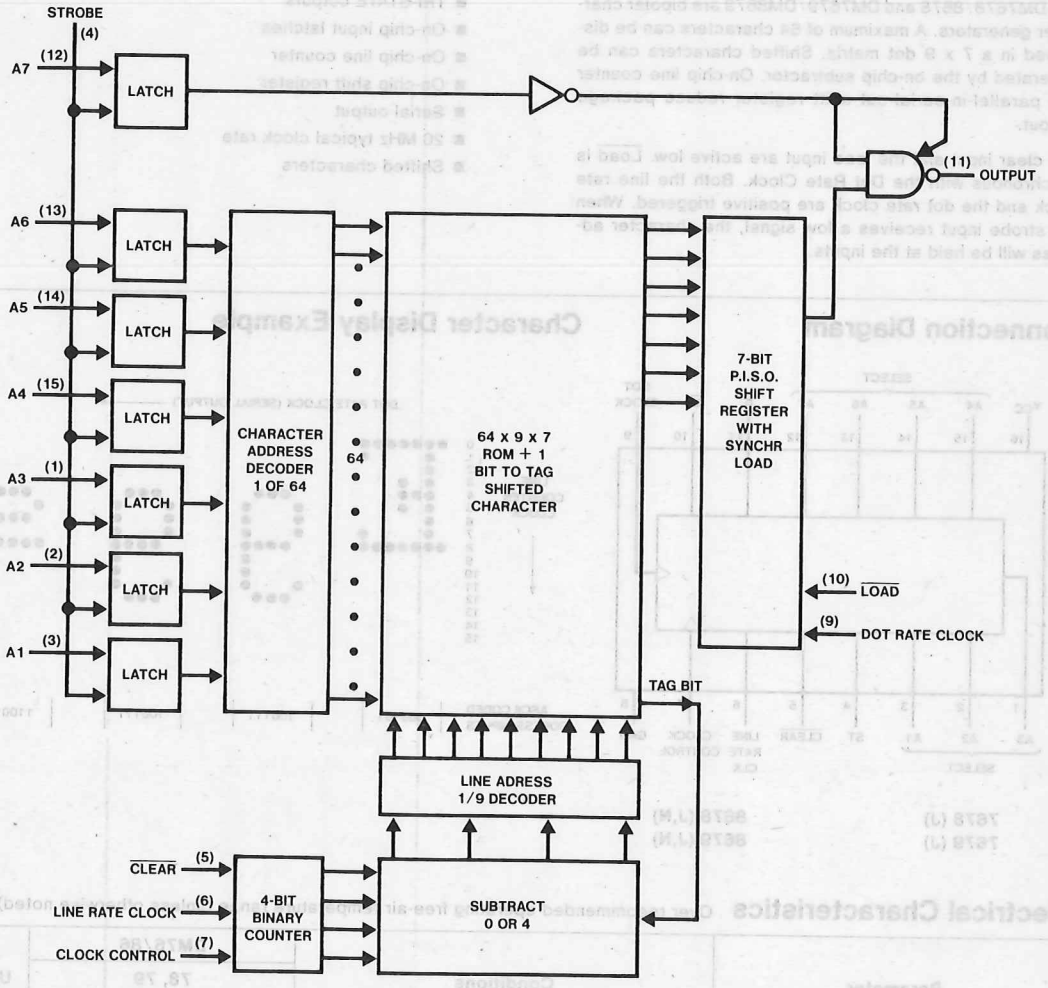
Over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | DM76/86 78, 79 Min | DM76/86 78, 79 Typ (1) | DM76/86 78, 79 Max | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = −2 mA | 2.4 | | | V |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = 16 mA | | | 0.4 | V |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | −0.8 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | 100 | | mA |
| $f_{MAX}$ | Maximum Clock Frequency | $V_{CC}$ = 5 V, $T_A$ = 25°C | | 20 | | MHz |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

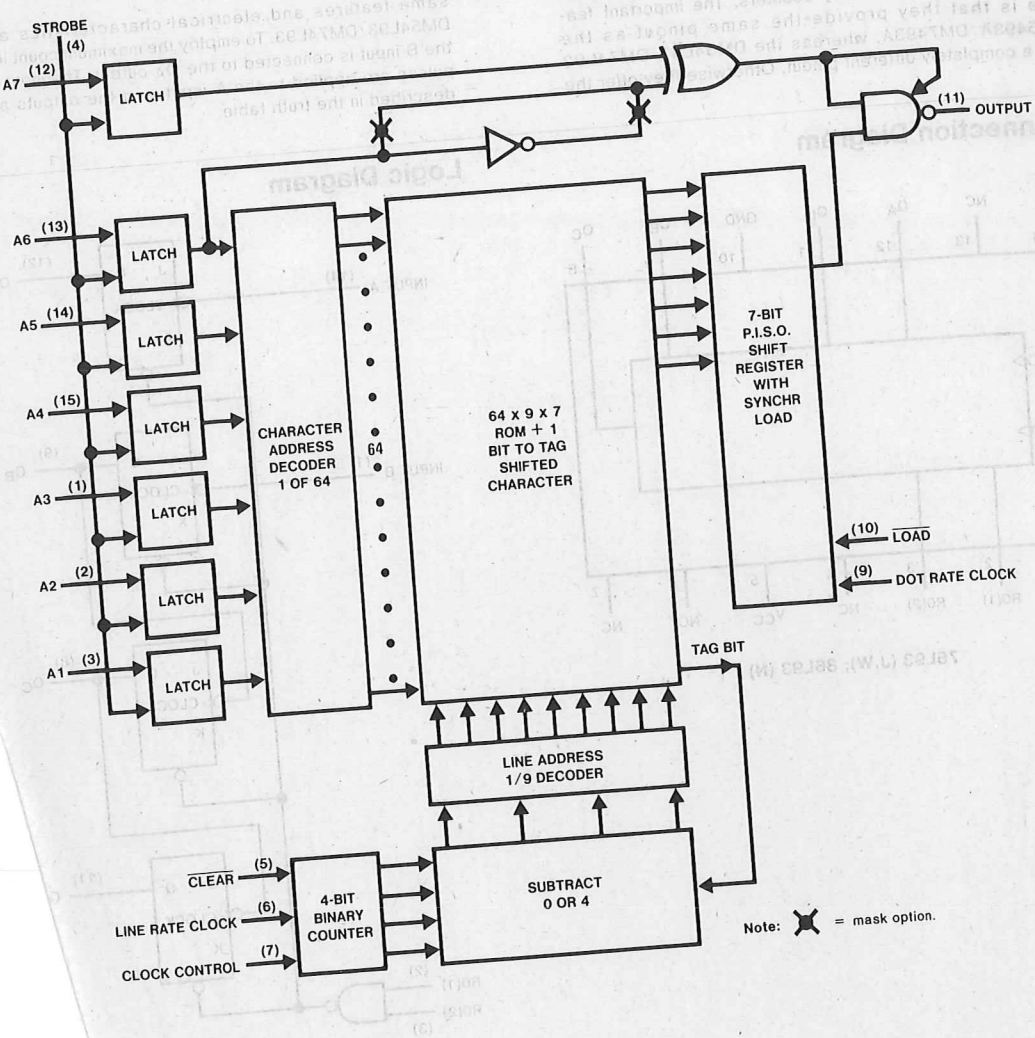
## Logic Diagrams

78



## Logic Diagrams (Continued)

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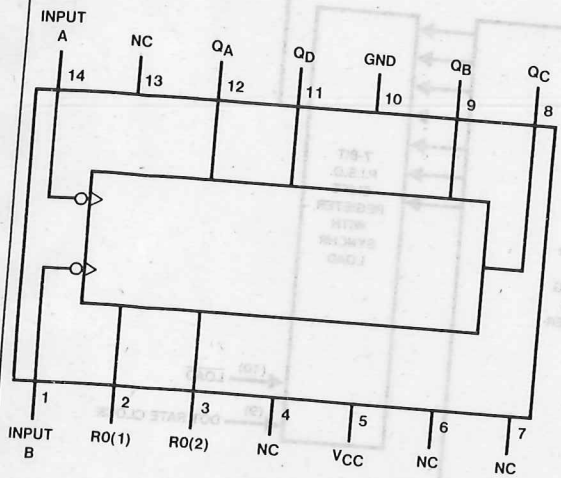


# DM76/DM86L93 Binary Counters

## General Description

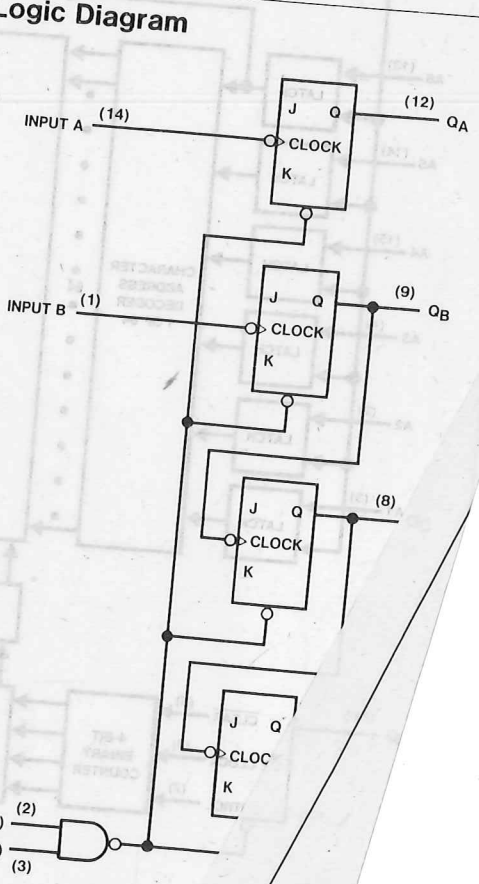
These circuits are full tenth-power versions of the popular DM5493A/DM7493A binary counters. The important feature is that they provide the same pinout as the DM5493A/DM7493A, whereas the DM54L93/DM74L93 has a completely different pinout. Otherwise they offer the same features and electrical characteristics as the DM54L93/DM74L93. To employ the maximum count length, the B input is connected to the $Q_A$ output. The input count pulses are applied to the A input, and the outputs are as described in the truth table.

## Connection Diagram




76L93 (J,W); 86L93 (N)

## Logic Diagram



## Truth Tables

**Reset/Count Truth Table**

| Reset Inputs | | Output | | | |
|---|---|---|---|---|---|
| R0(1) | R0(2) | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | L | L | L |
| L | X | COUNT | | | |
| X | L | COUNT | | | |

**Count Sequence Table**

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

Output $Q_A$ is connected to Input B

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM76 L93 | | | DM86 L93 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.7 | | | 0.7 | V |
| $I_{OH}$ | High Level Output Current | | | | | −200 | | | −200 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.7 V, $I_{OH}$ = −200 μA | | 2.4 | 2.8 | | 2.4 | 2.8 | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 2.0 | | | 3.6 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.7 V, $I_{OL}$ = Max | | | 0.15 | 0.3 | | 0.2 | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max<br>$V_I$ = 5.5 V | Reset | | | 100 | | | 100 | μA |
| | | | A Input | | | 200 | | | 200 | |
| | | | B Input | | | 200 | | | 200 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max<br>$V_I$ = 2.4 V | Reset | | | 10 | | | 10 | μA |
| | | | A Input | | | 20 | | | 20 | |
| | | | B Input | | | 20 | | | 20 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max<br>$V_I$ = 0.3 V | Reset | | | −180 | | | −180 | μA |
| | | | A Input | | | −360 | | | −360 | |
| | | | B Input | | | −360 | | | −360 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (3) | | −3 | −9 | −15 | −3 | −9 | −15 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (2) | | | | 5.5 | | | 5.5 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** $I_{CC}$ is measured with all outputs open, both $R_0$ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

**Note 3:** No more than one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Conditions | DM76/86 L93 Min | DM76/86 L93 Typ | DM76/86 L93 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | | | $C_L$ = 50 pF, $R_L$ = 4 kΩ | 6 | 15 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | A | $Q_D$ | | | 210 | 400 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | A | $Q_D$ | | | 230 | 400 | ns |
| $t_W$ | Pulse Width (All Inputs) | | | | 200 | | | ns |
| $t_{SETUP}$ | Reset Inactive State Setup Time | | | | 200 | | | ns |

# TRI-STATE® 1024-Bit Read Only Memories

## General Description

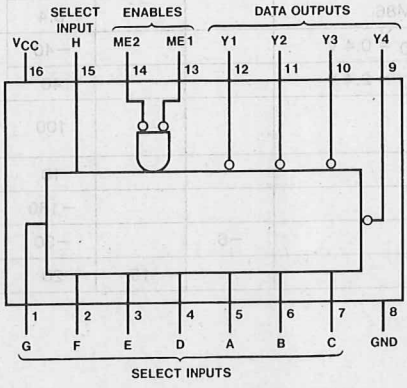
The DM76L97/DM86L97 is a custom-programmed Read Only Memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight select inputs.

Two overriding memory enable inputs are provided which when mask-programmed in one of the three options described will cause all four outputs to read either the normal memory contents or go to the high impedance state.

## Features

- Full tenth-power technology
- Pin compatible with SN54187/SN74187
- Typical power dissipation 75 mW
- Typical access time 70 ns
- Custom-programmed memory enable inputs
- TRI-STATE outputs

## Connection Diagram



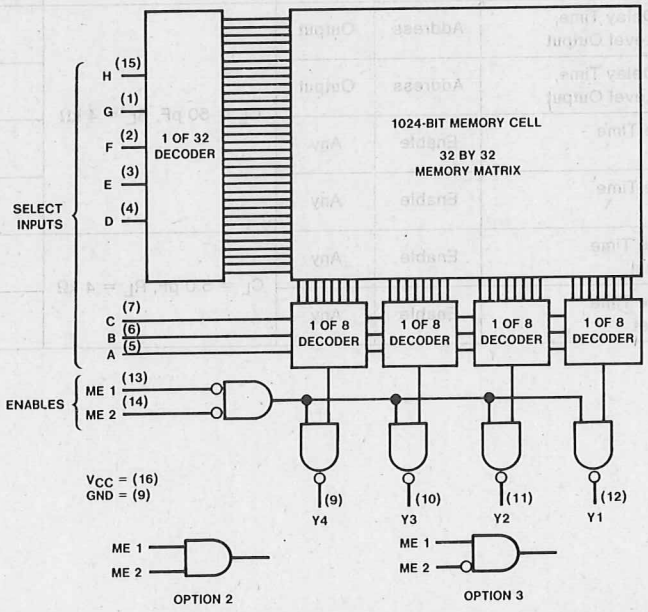

76L97 (J,W); 86L97 (N)

## Truth Table

| Option | ME1 | ME2 | Outputs |
|---|---|---|---|
| 1 | L | L | Normal |
| | H | X | High Impedance |
| | X | H | High Impedance |
| 2 | H | H | Normal |
| | L | X | High Impedance |
| | X | L | High Impedance |
| 3 | H | L | Normal |
| | X | H | High Impedance |
| | L | X | High Impedance |

X = Don't Care

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM76/86 L97 Min | DM76/86 L97 Typ (1) | DM76/86 L97 Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | $V_{CC}$ = Min | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | $V_{CC}$ = Min | | | | 0.7 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −1.0 | mA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = −1.0 mA | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | DM76 | | | 2.0 | mA |
| | | | DM86 | | | 3.6 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max | DM76 | | | 0.3 | V |
| | | | DM86 | | | 0.4 | |
| $I_{O(OFF)}$ | Off State (High Impedance State) Output Current | $V_{CC}$ = Max | $V_O$ = 0.4 V | | | −40 | μA |
| | | | $V_O$ = 2.4 V | | | 40 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 100 | μA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 10 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.3 V | | | | −180 | μA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −6 | | −30 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | 15 | 20 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | To (Output) | Conditions | DM76/86 L97 Min | DM76/86 L97 Typ | DM76/86 L97 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Address | Output | $C_L$ = 50 pF, $R_L$ = 4 kΩ | | 86 | 130 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Address | Output | | | 55 | 85 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | Enable | Any | | | 34 | 51 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | Enable | Any | | | 47 | 70 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | Enable | Any | $C_L$ = 5.0 pF, $R_L$ = 4 kΩ | | 15 | 23 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | Enable | Any | | | 57 | 86 | ns |

## Ordering Instructions

Programming instructions for the DM76L97 or DM86L97 are solicited in the form of a sequenced deck of 32 standard 80-column data cards providing the information requested under data card format, accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete truth table of the requested part. This truth table, showing output conditions for each of the 256 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the truth table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the eight words specified and describes the conditions at the four outputs for each of the eight words. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

## Supplementary Ordering Data

Submit the following information with the data cards:

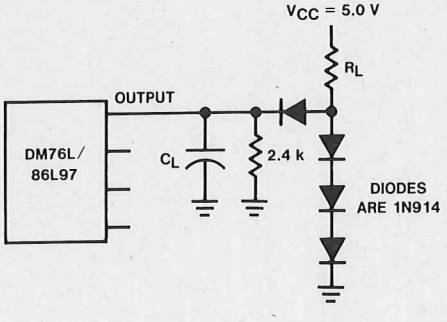
a. Customer's name and address
b. Customer's purchase order number
c. Customer's drawing number.

## Data Card Format

**Column**

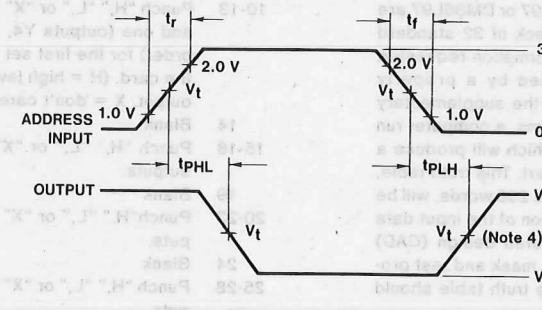
| | |
|---|---|
| 1-3 | Punch a right-justified integer representing the binary input address (000-248) for the first set of outputs described on the card. |
| 4 | Punch a "−" (Minus sign) |
| 5-7 | Punch a right-justified integer representing the binary input address (007-255) for the last set of outputs described on the card. |
| 8-9 | Blank |
| 10-13 | Punch "H," "L," or "X" for bits four, three, two, and one (outputs Y4, Y3, Y2, and Y1 in that order) for the first set of outputs specified on the card. (H = high level output, L = low level output, X = don't care.) |
| 14 | Blank |
| 15-18 | Punch "H," "L," or "X" for the second set of outputs. |
| 19 | Blank |
| 20-23 | Punch"H," "L," or "X" for the third set of outputs. |
| 24 | Blank |
| 25-28 | Punch "H," "L," or "X" for the fourth set of outputs. |
| 29 | Blank |
| 30-33 | Punch "H," "L," or "X" for the fifth set of outputs. |
| 34 | Blank |
| 35-38 | Punch "H," "L," or "X" for the sixth set of outputs. |
| 39 | Blank |
| 40-43 | Punch "H," "L," or "X" for the seventh set of outputs. |
| 44 | Blank |
| 45-48 | Punch "H," "L," or "X" for the eighth set of outputs. |
| 49 | Blank |
| 50-51 | Punch a right-justified integer representing the current calendar day of the month. |
| 52 | Blank |
| 53-55 | Punch an alphabetic abbreviation representing the current month. |
| 56 | Blank |
| 57-58 | Punch the last two digits of the current year. |
| 59 | Blank |
| 60-61 | Punch "DM" |
| 62-67 | Punch the National Semiconductor part number 76L97 or 86L97. |
| 68-70 | Blank |

## AC Test Circuit



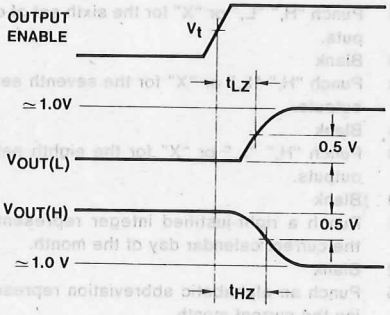

7

## Switching Time Waveforms

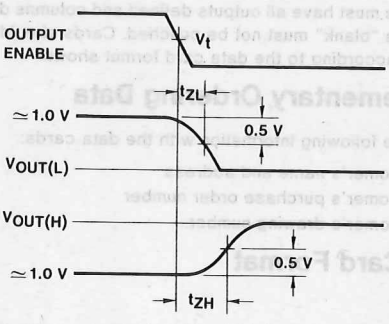



**Memory Enable**

$t_{LZ}$ & $t_{HZ}$




$t_{ZL}$ & $t_{ZH}$




**Note:** The pulse generator has the following characteristics: V = 3.0 V, $t_r$ = 15 ns, $t_f$ = 5.0 ns, f = 500 kHz, duty cycle = 50%, $Z_{OUT}$ = 50 Ω, $V_t$ = 1.3 V @ 25°C.

# TRI-STATE® 64-Bit Random Access Memories

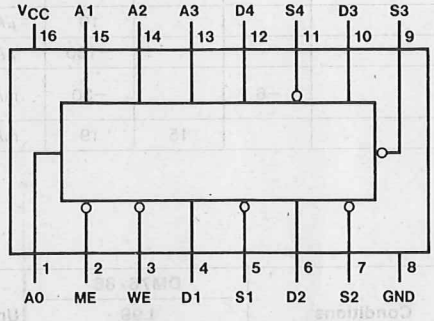
## General Description

The DM76L99/DM86L99 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory, the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the high-impedance state. This allows up to 75 memories to be connected to a common bus-line without the use of pull-up resistors. All memories except one are gated into the high-impedance state while the one selected memory exhibits the normal totem-pole, low impedance output characteristics of TTL.

## Features

- Same pin-out as SN5489/SN7489, 3101, MM5501
- Organized as 16, 4-bit words
- Expandable to 1200, 4-bit words without additional resistors
- Typical access from chip enable 50 ns
- Typical access time 80 ns
- Typical power dissipation 75 mW

## Connection Diagram

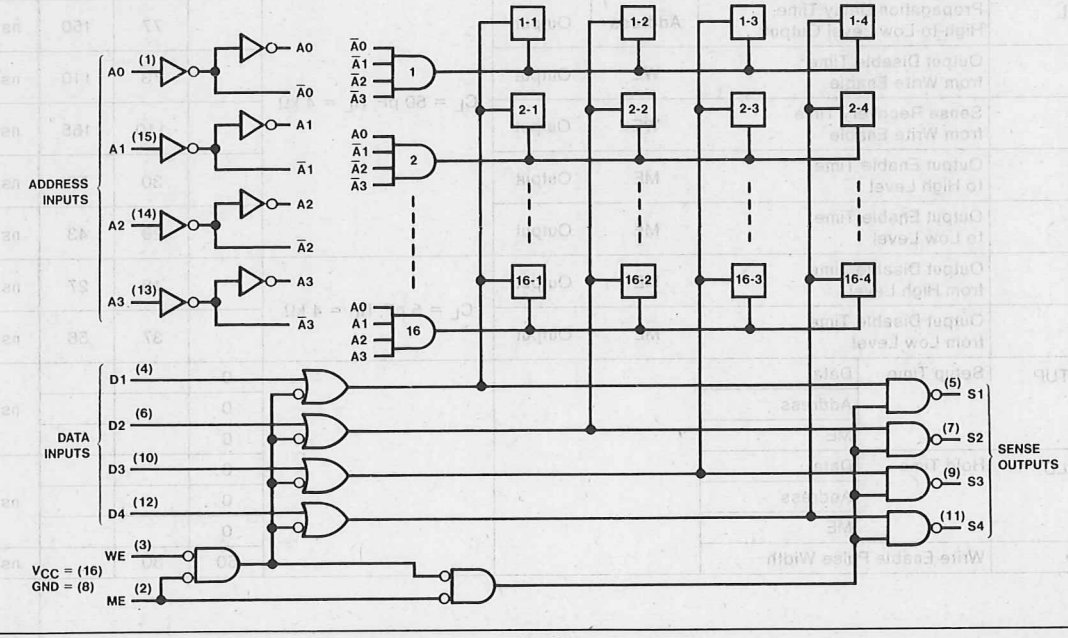



76L99 (J,W); 86L99 (N)

## Truth Table

| Memory Enable | Write Enable | Operation | Outputs |
|---|---|---|---|
| L | L | Write | Hi-Z |
| L | H | Read | Complement of Data Stored in Memory |
| H | X | Hold | Hi-Z |

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM76/86 L99 Min | DM76/86 L99 Typ (1) | DM76/86 L99 Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | $V_{CC}$ = Min | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | $V_{CC}$ = Min | | | | 0.7 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −1.0 | mA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = −1.0 mA | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | DM76L | | | 2.0 | mA |
| | | | DM86L | | | 3.6 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max | DM76L | | | 0.3 | V |
| | | | DM86L | | | 0.4 | |
| $I_{O(OFF)}$ | Off State (High Impedance State) Output Current | $V_{CC}$ = Max | $V_O$ = 0.3 V | | | −40 | μA |
| | | | $V_O$ = 2.4 V | | | 40 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 100 | μA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 10 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.3 V | | | | −180 | μA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −6 | | −30 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | 15 | 19 | mA |

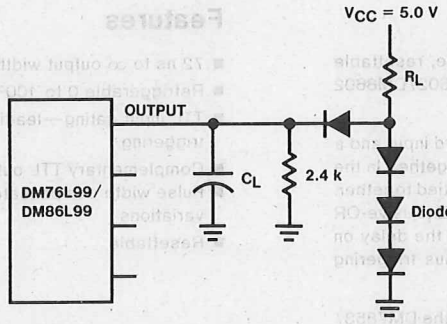
**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time.

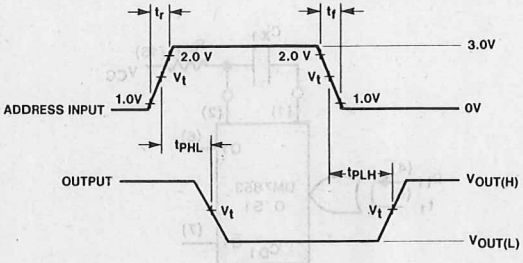
## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From | To | Conditions | DM76/86 L99 Min | DM76/86 L99 Typ (1) | DM76/86 L99 Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Address | Output | $C_L$ = 50 pF, $R_L$ = 4 kΩ | | 51 | 120 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Address | Output | | | 77 | 150 | ns |
| $t_{\overline{EN}}$ | Output Disable Time from Write Enable | | WE | Output | | | 73 | 110 | ns |
| $t_{SR}$ | Sense Recovery Time from Write Enable | | WE | Output | | | 110 | 165 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | | ME | Output | | | 30 | 50 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | ME | Output | | | 29 | 43 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | | ME | Output | $C_L$ = 5 pF, $R_L$ = 4 kΩ | | 18 | 27 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | ME | Output | | | 37 | 56 | ns |
| $t_{SETUP}$ | Setup Time | Data | | | | 0 | | | ns |
| | | Address | | | | 0 | | | |
| | | ME | | | | 0 | | | |
| $t_{HOLD}$ | Hold Time | Data | | | | 0 | | | ns |
| | | Address | | | | 0 | | | |
| | | ME | | | | 0 | | | |
| $t_{WP}$ | Write Enable Pulse Width | | | | | 50 | 30 | | ns |

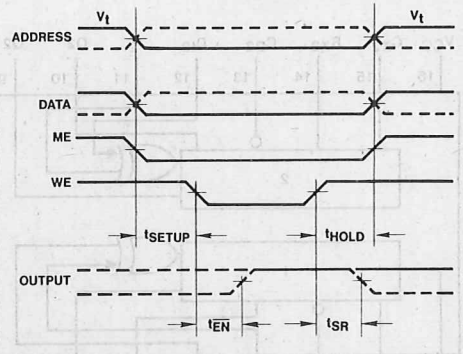
## AC Test Circuit



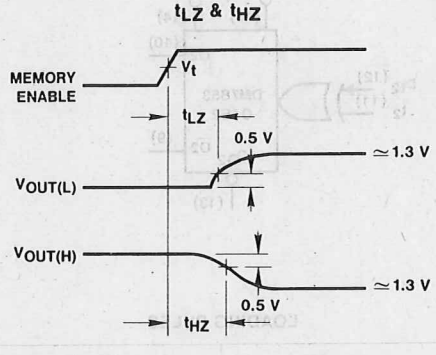

## Switching Time Waveforms

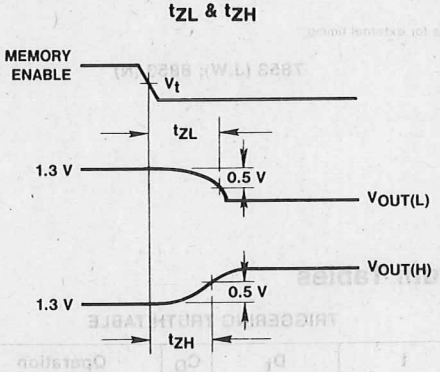



### WRITE CYCLE




### MEMORY ENABLE




Note: The pulse generator has the following characteristics: V = 3.0 V, $t_r$ = 15 ns, $t_f$ = 5.0 ns, f = 500 kHz, duty cycle = 50%, $Z_{OUT}$ = 50 Ω, $V_t$ = 1.3 V @ 25°C.

# Dual Retriggerable Resettable One Shots

## General Description

The DM7853/DM8853 is a dual, retriggerable, resettable monostable multivibrator similar to the DM9602/DM8602 but with a unique input triggering logic.

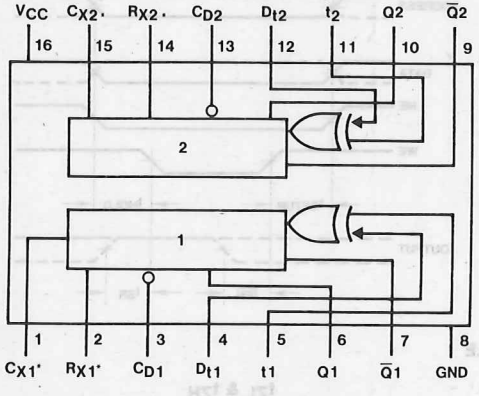
This device has two trigger inputs—a standard input and a delayed input—which are Exclusive OR'ed together. In the dual-edge triggering mode, the two inputs are tied together. On either a positive or negative transition the Exclusive-OR logic is satisfied for a length of time equal to the delay on the delayed input—approximately 15 ns—thus triggering or retriggering the one-shot.

Once fired, the accuracy and performance of the DM7853/DM8853 is identical to that of the DM9602/DM8602.

## Features

- 72 ns to ∞ output width range
- Retriggerable 0 to 100% duty cycle
- TTL input gating—leading AND/OR trailing edge triggering
- Complementary TTL outputs
- Pulse width compensated for $V_{CC}$ and temperature variations
- Resettable

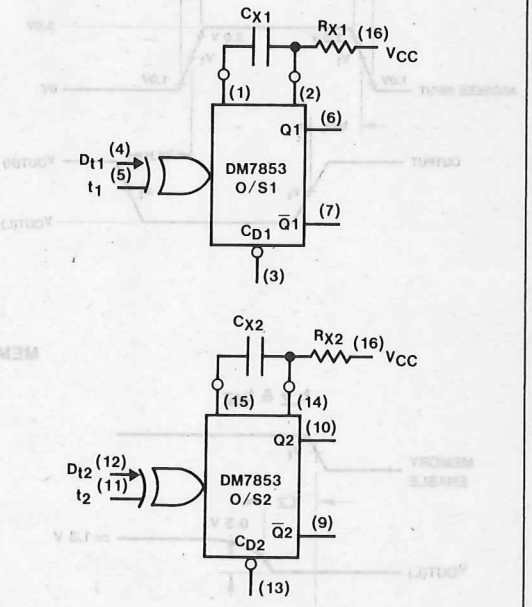
## Connection Diagram




*Pins for external timing

7853 (J,W); 8853 (N)

## Logic Diagrams




## Truth Tables

TRIGGERING TRUTH TABLE

| t | $D_t$ | $C_D$ | Operation |
|---|---|---|---|
| L → H | L | H | Trigger |
| H | H → L | H | Trigger |
| H → L | H | H | Trigger |
| L | L → H | H | Trigger |
| H → L | Same as t | H | Trigger |
| L → H | Same as t | H | Trigger |
| X | X | L | Reset |

LOADING RULES

| Inputs | Load | |
|---|---|---|
| | High | Low |
| 3, 4, 5, 11, 12, 13 | 1 U.L. | 1 U.L. |

| Outputs | Drive Factor | |
|---|---|---|
| | High | Low |
| 6, 7, 9, 10 | 16 U.L. | 8 U.L. |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions (2) | DM78 | | | DM88 | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 53 | | | 53 | | | |
| | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | −800 | | | −800 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −800 μA (3) | 2.4 | 3.3 | | 2.4 | 3.4 | | V |
| $I_{OL}$ | Low Level Output Current | | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA (3) | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 4.5 V | | 10 | 60 | | 10 | 60 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | −1.1 | −1.6 | | | | mA |
| | | $V_{CC}$ = Max, $V_I$ = 0.45 V | | | | | −1.0 | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max, $V_{OUT}$ = 1.0 V (3) | | | −25 | | | −35 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | 55 | 72 | | 55 | 72 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

**Note 2:** Unless otherwise noted, 10 kΩ resistor placed between $R_X$ and $V_{CC}$ for all tests.

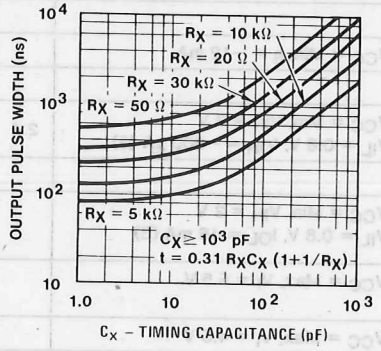
**Note 3:** Ground Pin 1 (15) for $V_{OL}$ on Pin 7 (9), or for $V_{OH}$ on Pin 6 (10), or for $I_{OS}$ on Pin 6 (10); also, apply momentary ground to Pin 4 (12). Open Pin 1 (15) for $V_{OL}$ on Pin 6 (10), or for $V_{OH}$ on Pin 7 (9), or for $I_{OS}$ on Pin 7 (9).

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

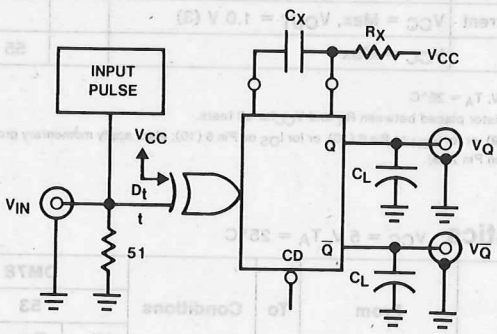
| Parameter | | From | To | Conditions | DM78 | | | DM88 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 53 | | | 53 | | | |
| | | | | | Min | Typ | Max | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Standard Trigger Input | Q | $C_L$ = 15 pF, $R_X$ = 5 kΩ, $C_X$ = 0 | | 25 | 35 | | 25 | 40 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Standard Trigger Input | $\overline{Q}$ | | | 29 | 43 | | 29 | 48 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Delayed Trigger Input | Q | | | 40 | 53 | | 40 | 58 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Delayed Trigger Input | $\overline{Q}$ | | | 44 | 61 | | 44 | 66 | ns |
| $t_{W(MIN)}$ | Minimum Possible Output Pulse | | Q | | | 72 | 90 | | 72 | 100 | ns |
| | | | $\overline{Q}$ | | | 78 | 100 | | 78 | 110 | |
| $t_W$ | Pulse Width Tolerance | | | $C_X$ = 1000 pF, $R_X$ = 10 kΩ | 3.08 | 3.42 | 3.76 | 3.08 | 3.42 | 3.76 | μs |
| $C_{STRAY}$ | Maximum Allowable Wiring Capacitance | | | Pins (2) and (14) to GND | | | 50 | | | 50 | pF |
| $R_X$ | Timing Resistor | | | | 5 | | 25 | 5 | | 50 | kΩ |

## Typical Performance Characteristics

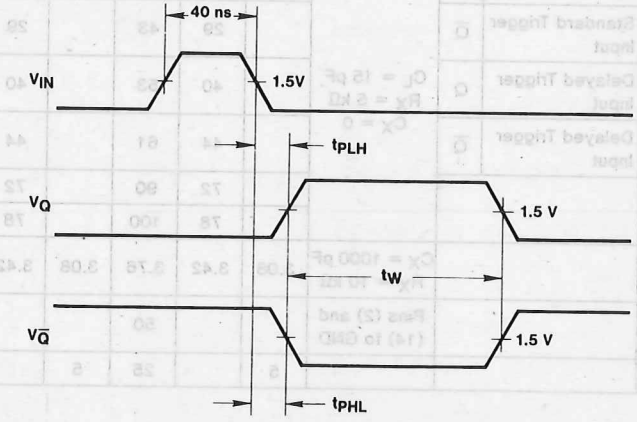
**Output Pulse Width vs Timing Resistance and Capacitance for $C_X < 10^3$ pF**




## Switching Circuit




## Switching Time Waveforms




Input Pulses
$f \simeq 100$ kHz
Amp $\simeq 3.0$ V
Width $\simeq 40$ ns
$t_r = t_f \leq 10$ ns

# TRI-STATE® 4-Bit Parallel Binary Multipliers

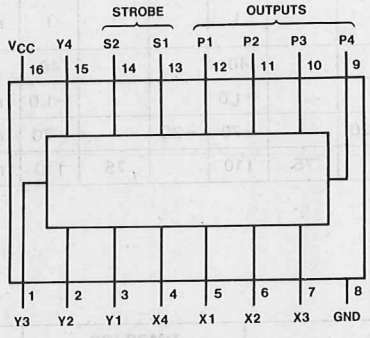
## General Description

These circuits are capable of multiplying together two 4-bit binary numbers when used together in pairs. The DM7875A/8875A provides the most significant four bits, and the DM7875B/8875B provides the least significant four bits. Since the largest number that can be obtained by multiplying two 4-bit numbers is 225 (15 x 15), the eight output pins (four from each package) are sufficient to produce this number. Both the multiplier and the multiplicand must be connected to the eight input pins of each device. These devices are pin compatible with the SN54284/74284, and SN54285/74285; but have the advantage that these circuits provide either standard totem-pole TTL or TRI-STATE outputs. A gated two-input strobe control is provided. When either one, or both, of the strobe inputs is raised to a high logic level the outputs are forced into the high-impedance state. Thus, multiple devices may be connected to a common bus line.

## Features

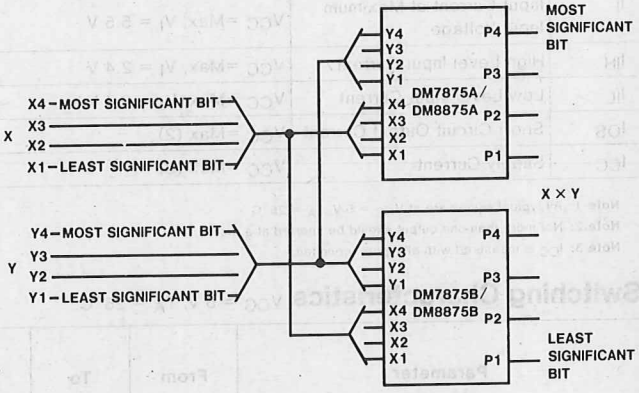
- Pin compatible replacements for
  SN54284/74284 (DM7875A/8875A)
  SN54285/74285 (DM7875B/8875B)
- TRI-STATE outputs
- Typical propagation delay 35 ns

## Connection Diagram

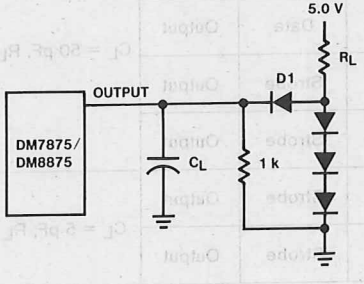



**7875A (J,W); 8875A (N)**
**7875B (J,W); 8875B (N)**

## Typical Application




## AC Test Circuit



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

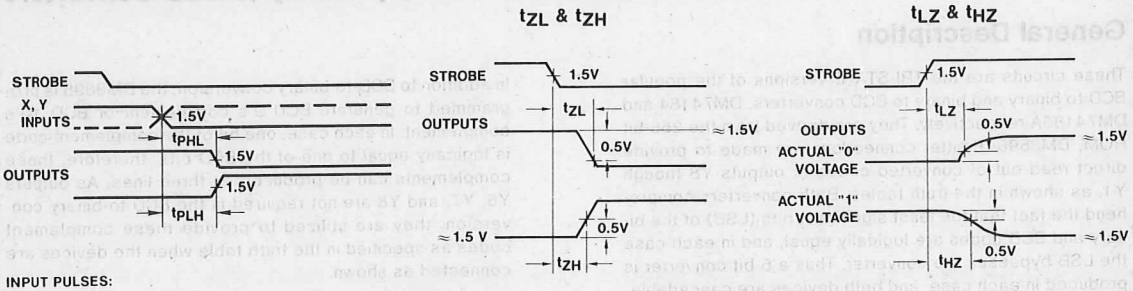
| Parameter | | Conditions | | DM78 75A, 75B | | | DM88 75A, 75B | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −2.0 | | | −5.2 | mA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | | 0.4 | | | 0.4 | V |
| $I_{O(OFF)}$ | Off State (High Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $V_O$ = 0.4 V | | | −40 | | | −40 | µA |
| | | | $V_O$ = 2.4 V | | | 40 | | | 40 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | | | 40 | µA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −1.0 | | | −1.0 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −20 | | −70 | −20 | | −70 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | | 75 | 110 | | 75 | 110 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.
**Note 3:** $I_{CC}$ is measured with all inputs grounded.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C.

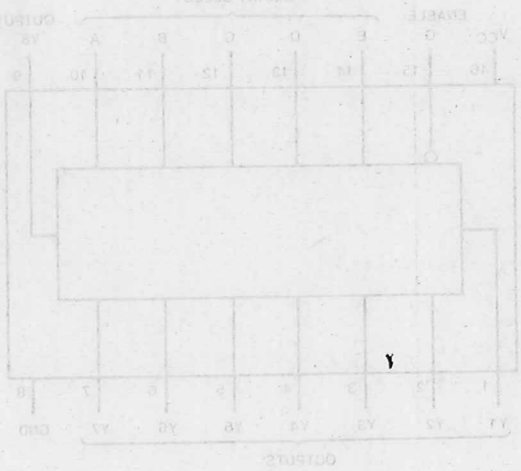
| Parameter | | From | To | Conditions | DM78/88 75A, 75B | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Output | $C_L$ = 50 pF, $R_L$ = 400 Ω | | 35 | 60 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Data | Output | | | 35 | 60 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | Strobe | Output | | | 20 | 30 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | Strobe | Output | | | 20 | 30 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | Strobe | Output | $C_L$ = 5 pF, $R_L$ = 400 Ω | | 20 | 30 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | Strobe | Output | | | 20 | 30 | ns |

## Switching Time Waveforms




**INPUT PULSES:**

$t_r = t_f \leq 10$ ns
f = 1 MHz



7

# TRI-STATE® BCD to Binary/Binary to BCD Converters

## General Description

These circuits are the TRI-STATE versions of the popular BCD to binary and binary to BCD converters, DM74184 and DM74185A respectively. They are derived from the 256-bit ROM, DM8598. Emitter connections are made to provide direct read out of converted codes at outputs Y8 though Y1, as shown in the truth tables. Both converters comprehend the fact that the least significant bits (LSB) of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter. Thus a 6-bit converter is produced in each case, and both devices are cascadable.

An overriding enable input is provided on each converter which, when taken high, inhibits the function, causing all outputs to go into the high-impedance state. For this reason, and to minimize power consumption, unused outputs Y7 and Y8 of the 185A and all "don't care" conditions of the 184 are programmmed high.

### DM8898 BCD-TO-BINARY CONVERTERS

The 6-bit BCD-to-binary function of the DM8898 is analogous to the algorithm:

a. Shift BCD number right one bit and examine each decade. Subtract three from each 4-bit decade containing a binary value greater than seven.

b. Shift right, examine, and correct after each shift until the least significant decade contains a number smaller than eight and all other converted decades contain zeros.

In addition to BCD-to-binary conversion, the DM8898 is programmed to generate BCD 9's complement or BCD 10's complement. In each case, one bit of the complement code is logically equal to one of the BCD bits; therefore, these complements can be produced on three lines. As outputs Y6, Y7, and Y8 are not required in the BCD-to-binary conversion, they are utilized to provide these complement codes as specified in the truth table when the devices are connected as shown.

### DM8899 BINARY-TO-BCD CONVERTERS

The function performed by these 6-bit binary-to-BCD converters is analogous to the algorithm:

a. Examine the three most significant bits. If the sum is greater than four, add three and shift left one bit.

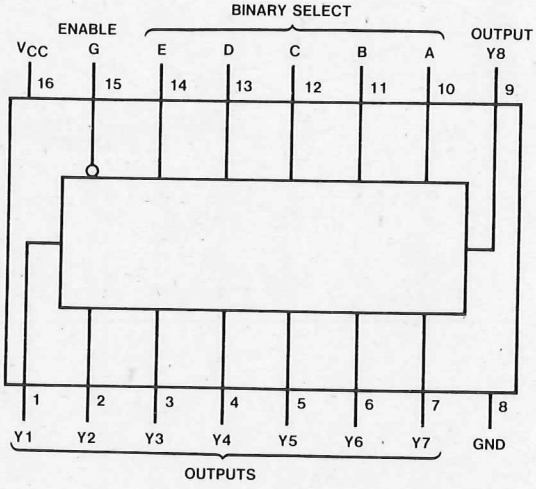
b. Examine each BCD decade. If the sum is greater than four, add three and shift left one bit.

c. Repeat step b until the least-significant binary bit is in the least-significant BCD location.

## Features

- TRI-STATE versions of DM74184, DM74185A
- Typical propagation delay 30 ns

## Connection Diagram




8898 (N); 8899 (N)

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM88 98, 99 Min | DM88 98, 99 Typ (1) | DM88 98, 99 Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −5.2 | mA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OH}$ = −5.2 mA | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 12 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 12 mA | | | | 0.4 | V |
| $I_{O(OFF)}$ | Off State (High Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V | $V_O$ = 0.4 V | | | −40 | μA |
| | | | $V_O$ = 2.4 V | | | 40 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −20 | | −70 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max, $V_I$ = 0 V | | | 70 | 99 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From | To | Conditions | DM88 98, 99 Min | DM88 98, 99 Typ | DM88 98, 99 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Binary Select | Output | $C_L$ = 50 pF, $R_L$ = 400 Ω | | 29 | 50 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Binary Select | Output | | | 33 | 50 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | Enable | Output | | | 16 | 25 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | Enable | Output | | | 26 | 40 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | Enable | Output | $C_L$ = 5 pF, $R_L$ = 400 Ω | | 13 | 20 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | Enable | Output | | | 24 | 36 | ns |

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## Truth Tables

### BCD-TO-BINARY CONVERTER

| BCD WORDS | | Inputs (See Note A) | | | | | | Outputs (See Note B) | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | E | D | C | B | A | G | Y5 | Y4 | Y3 | Y2 | Y1 |
| 0 | 1 | L | L | L | L | L | L | L | L | L | L | L |
| 2 | 3 | L | L | L | L | H | L | L | L | L | L | H |
| 4 | 5 | L | L | L | H | L | L | L | L | L | H | L |
| 6 | 7 | L | L | L | H | H | L | L | L | L | H | H |
| 8 | 9 | L | L | H | L | L | L | L | L | H | L | L |
| 10 | 11 | L | H | L | L | L | L | L | L | H | L | H |
| 12 | 13 | L | H | L | L | H | L | L | L | H | H | L |
| 14 | 15 | L | H | L | H | L | L | L | L | H | H | H |
| 16 | 17 | L | H | L | H | H | L | L | H | L | L | L |
| 18 | 19 | L | H | H | L | L | L | L | H | L | L | H |
| 20 | 21 | H | L | L | L | L | L | L | H | L | H | L |
| 22 | 23 | H | L | L | L | H | L | L | H | L | H | H |
| 24 | 25 | H | L | L | H | L | L | L | H | H | L | L |
| 26 | 27 | H | L | L | H | H | L | L | H | H | L | H |
| 28 | 29 | H | L | H | L | L | L | L | H | H | H | L |
| 30 | 31 | H | H | L | L | L | L | L | H | H | H | H |
| 32 | 33 | H | H | L | L | H | L | H | L | L | L | L |
| 34 | 35 | H | H | L | H | L | L | H | L | L | L | H |
| 36 | 37 | H | H | L | H | H | L | H | L | L | H | L |
| 38 | 39 | H | H | H | L | L | L | H | L | L | H | H |
| ANY | | X | X | X | X | X | H | Z | Z | Z | Z | Z |

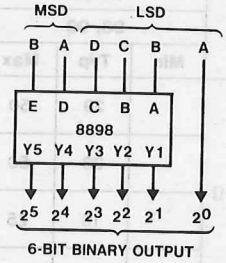
H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

### BCD 9'S OR BCD 10'S COMPLEMENT CONVERTER

| BCD WORD | Inputs (See Note C) | | | | | | Outputs (See Note D) | | |
|---|---|---|---|---|---|---|---|---|---|
| | E† | D | C | B | A | G | Y8 | Y7 | Y6 |
| 0 | L | L | L | L | L | L | H | L | H |
| 1 | L | L | L | L | H | L | H | L | L |
| 2 | L | L | L | H | L | L | L | H | H |
| 3 | L | L | L | H | H | L | L | H | L |
| 4 | L | L | H | L | L | L | L | H | H |
| 5 | L | L | H | L | H | L | L | H | L |
| 6 | L | L | H | H | L | L | L | L | H |
| 7 | L | L | H | H | H | L | L | L | L |
| 8 | L | H | L | L | L | L | L | L | H |
| 9 | L | H | L | L | H | L | L | L | L |
| 0 | H | L | L | L | L | L | L | L | L |
| 1 | H | L | L | L | H | L | H | L | L |
| 2 | H | L | L | H | L | L | H | L | L |
| 3 | H | L | L | H | H | L | L | H | H |
| 4 | H | L | H | L | L | L | L | H | H |
| 5 | H | L | H | L | H | L | L | H | L |
| 6 | H | L | H | H | L | L | L | H | L |
| 7 | H | L | H | H | H | L | L | L | H |
| 8 | H | H | L | L | L | L | L | L | H |
| 9 | H | H | L | L | H | L | L | L | L |
| ANY | X | X | X | X | X | H | Z | Z | Z |

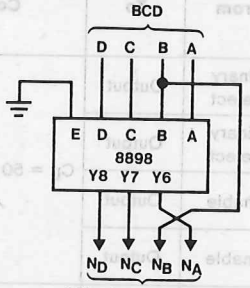
H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

### 6-BIT Converter



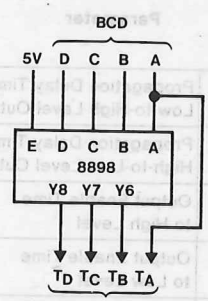

6-BIT BINARY OUTPUT

### BCD 9's Complement Converter




BCD 9's COMPLEMENT

### BCD 10's Complement Converter




BCD 10's COMPLEMENT

**Note A:** Input conditions other than those shown produce highs at outputs Y1 through Y5.

**Note B:** Outputs Y6, Y7, and Y8 are not used for BCD-to-binary conversion.

**Note C:** Input conditions other than those shown produce highs at outputs Y6, Y7, and Y8.

**Note D:** Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.

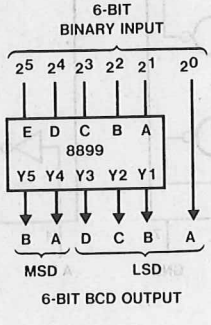
†When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated; when it is high, the BCD 10's complement is generated.

## Truth Tables (Continued)

| Binary Words | | Inputs | | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Binary Select | | | | | Enable | | | | | | | | |
| | | E | D | C | B | A | G | Y8 | Y7 | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 |
| 0 | 1 | L | L | L | L | L | L | H | H | L | L | L | L | L | L |
| 2 | 3 | L | L | L | L | H | L | H | H | L | L | L | L | L | H |
| 4 | 5 | L | L | L | H | L | L | H | H | L | L | L | L | H | L |
| 6 | 7 | L | L | L | H | H | L | H | H | L | L | L | L | H | H |
| 8 | 9 | L | L | H | L | L | L | H | H | L | L | L | H | L | L |
| 10 | 11 | L | L | H | L | H | L | H | H | L | L | H | L | L | L |
| 12 | 13 | L | L | H | H | L | L | H | H | L | L | H | L | L | H |
| 14 | 15 | L | L | H | H | H | L | H | H | L | L | H | L | H | L |
| 16 | 17 | L | H | L | L | L | L | H | H | L | L | H | L | H | H |
| 18 | 19 | L | H | L | L | H | L | H | H | L | L | H | H | L | L |
| 20 | 21 | L | H | L | H | L | L | H | H | L | H | L | L | L | L |
| 22 | 23 | L | H | L | H | H | L | H | H | L | H | L | L | L | H |
| 24 | 25 | L | H | H | L | L | L | H | H | L | H | L | L | H | L |
| 26 | 27 | L | H | H | L | H | L | H | H | L | H | L | L | H | H |
| 28 | 29 | L | H | H | H | L | L | H | H | L | H | L | H | L | L |
| 30 | 31 | L | H | H | H | H | L | H | H | L | H | H | L | L | L |
| 32 | 33 | H | L | L | L | L | L | H | H | L | H | H | L | L | H |
| 34 | 35 | H | L | L | L | H | L | H | H | L | H | H | L | H | L |
| 36 | 37 | H | L | L | H | L | L | H | H | L | H | H | L | H | H |
| 38 | 39 | H | L | L | H | H | L | H | H | L | H | H | H | L | L |
| 40 | 41 | H | L | H | L | L | L | H | H | H | L | L | L | L | L |
| 42 | 43 | H | L | H | L | H | L | H | H | H | L | L | L | L | H |
| 44 | 45 | H | L | H | H | L | L | H | H | H | L | L | L | H | L |
| 46 | 47 | H | L | H | H | H | L | H | H | H | L | L | L | H | H |
| 48 | 49 | H | H | L | L | L | L | H | H | H | L | L | H | L | L |
| 50 | 51 | H | H | L | L | H | L | H | H | H | L | H | L | L | L |
| 52 | 53 | H | H | L | H | L | L | H | H | H | L | H | L | L | H |
| 54 | 55 | H | H | L | H | H | L | H | H | H | L | H | L | H | L |
| 56 | 57 | H | H | H | L | L | L | H | H | H | L | H | L | H | H |
| 58 | 59 | H | H | H | L | H | L | H | H | H | L | H | H | L | L |
| 60 | 61 | H | H | H | H | L | L | H | H | H | H | L | L | L | L |
| 62 | 63 | H | H | H | H | H | L | H | H | H | H | L | L | L | H |
| ALL | | X | X | X | X | X | H | Z | Z | Z | Z | Z | Z | Z | Z |

H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

### 6-Bit Converter



## General Description

DM9000C series devices are designed to be used in existing systems as replacements for Fairchild 9000-type circuits. These DM9000C circuits offer several significant advantages over 9000 type circuits, some of which are:

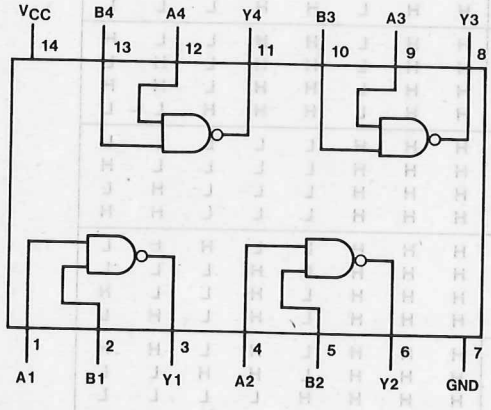
- Input clamp diodes
- Output short-circuit current specified to guarantee the high-level impedance.
- Power dissipation of DM9000C circuits is in most cases lower than that for the equivalent 9000 type.

DM9000C circuits are characterized for operation over the industrial temperature range of 0°C to 75°C.

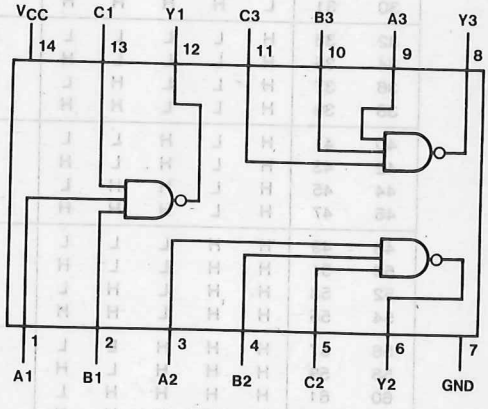
For the new designs, the 54/74 families of TTL circuits offer the industry's broadest choice of high-performance digital circuits. Series 54/74 pin-for-pin equivalents are available for the following SSI types:

| DM9000C Series | Equivalent Series 74 |
|---|---|
| DM9002C | DM7400 |
| DM9003C | DM7410 |
| DM9004C | DM7420 |
| DM9012C | DM7403 |
| DM9016C | DM7404 |
| DM9024C | DM74109 |

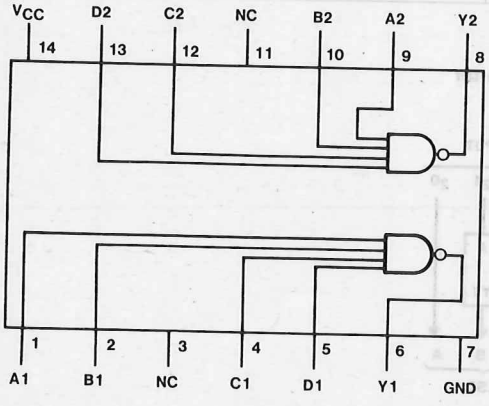
## Connection Diagrams



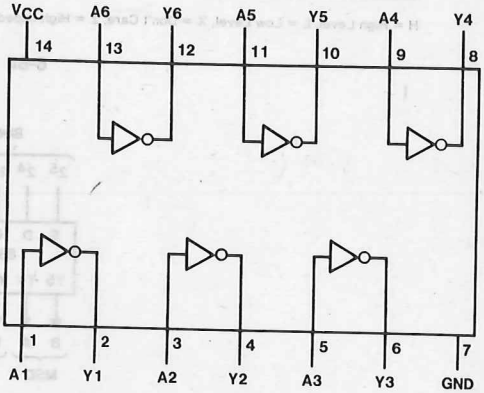

9002C (J,N); 9012C (J,N)




9003C (J,N)




9004C (J,N)




9016C (J,N)

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

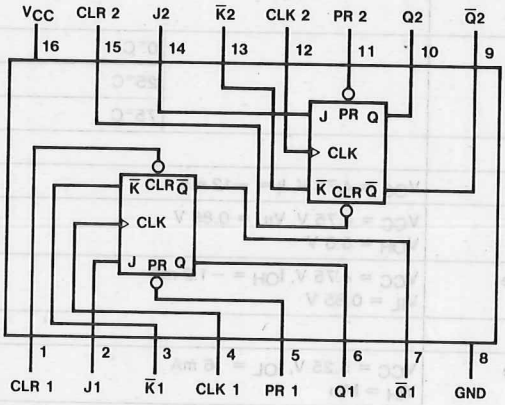
| Parameter | | Conditions | | DM90 02C, 03C 04C, 16C Min | DM90 02C, 03C 04C, 16C Max | DM90 12C Min | DM90 12C Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | 0°C | 1.9 | | 1.9 | | V |
| | | | 25°C | 1.8 | | 1.8 | | |
| | | | 75°C | 1.6 | | 1.6 | | |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.85 | | 0.85 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = 4.75 V, $I_I$ = −12 mA | | | −1.5 | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.85 V, $V_{OH}$ = 5.5 V | | | −1.2 | | 0.25 | mA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = 4.75 V, $I_{OH}$ = −1.2 mA, $V_{IL}$ = 0.85 V | | 2.4 | | | N/A | V |
| $I_{OL}$ | Low Level Output Current | | | | 50 | | 50 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = 5.25 V, $I_{OL}$ = 16 mA, $V_{IH}$ = Min | | | 0.45 | | 0.45 | V |
| | | $V_{CC}$ = 4.75 V, $I_{OL}$ = 14.1 mA, $V_{IH}$ = Min | | | 0.45 | | 0.45 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = 5.25 V, $V_I$ = 4.5 V, Other Inputs at Ground | | | 60 | | 60 | μA |
| $I_{IL}$ | Low Level Input Current | $V_I$ = 4.5 V, Other Inputs at 5.25 V | $V_{CC}$ = 5.25 V | | −1.6 | | −1.6 | mA |
| | | | $V_{CC}$ = 4.75 V | | −1.41 | | −1.41 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = 5.25 V (1) | | −18 | −55 | N/A | N/A | mA |
| $I_{CCH}$ | Supply Current, All Outputs High | $V_{CC}$ = 5 V | | | 1.7 | | 1.7 | mA |
| $I_{CCL}$ | Supply Current, All Outputs Low | $V_{CC}$ = 5 V | | | 6.1 | | 6.1 | mA |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $C_L$ = 15 pF, $R_L$ = 400 Ω (2), $V_{CC}$ = 5 V, $T_A$ = 25°C | | 3 | 13 | 3 | 45 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | 3 | 15 | 3 | 15 | |

**Note 1:** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

**Note 2:** For testing $t_{PLH}$ of DM9012C, $R_L$ = 4 kΩ.

# Dual J-K Flip-Flops with Preset and Clear

## Connection Diagram




9024 (J,W); 8024 (N)

## Truth Table

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| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| Preset | Clear | Clock | J | $\overline{K}$ | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | ↑ | L | L | L | H |
| H | H | ↑ | H | L | TOGGLE | |
| H | H | ↑ | L | H | Q0 | $\overline{Q}$0 |
| H | H | ↑ | H | H | H | L |
| H | H | L | X | X | Q0 | $\overline{Q}$0 |

H = High Level (Steady State), L = Low Level (Steady State),
X = Don't Care
↑ = Transition from low to high level
Q0 = The level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.
*This configuration is nonstable. That is, it will not persist when preset and clear inputs return to their inactive (high) level.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | | DM90 24 Min | DM90 24 Max | DM80 24 Min | DM80 24 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | $T_A$ = Min | | 2.0 | | 1.9 | | V |
| | | | | $T_A$ = 25°C | | 1.7 | | 1.8 | | |
| | | | | $T_A$ = Max | | 1.4 | | 1.6 | | |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.9 | | 0.85 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | | −1.2 | | −1.2 | mA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = Min<br>$V_{IL}$ = Max, $I_{OH}$ = −1.2 mA | | | 2.4 | | 2.4 | | V |
| $I_{OL}$ | Low Level Output Current | | | | | | 12.4 | | 14.1 | mA |
| $V_{OL}$ | Low Level Output Voltage | | $V_{IH}$ = Min<br>$V_{IL}$ = Max | $V_{CC}$ = Min | $I_{OL}$ = 12.4 mA | | 0.40 | | | V |
| | | | | | $I_{OL}$ = 14.1 mA | | | | 0.45 | |
| | | | | $V_{CC}$ = Max | $I_{OL}$ = 16 mA | | 0.40 | | 0.45 | |
| $I_{IH}$ | High Level Input Current | J or $\overline{K}$ | $V_{CC}$ = Max,<br>$V_I$ = 4.5 V<br>Other Inputs at Gnd | | $T_A$ = 25°C and 125°C (DM90)<br>$T_A$ = 25°C and 75°C (DM80) | | 60 | | 60 | µA |
| | | Clock | | | | | 120 | | 120 | |
| | | Preset | | | | | 120 | | 120 | |
| | | Clear | | | | | 240 | | 240 | |
| $I_{IL}$ | Low Level Input Current | J or $\overline{K}$ | $V_I$ = 0.40 V (DM90)<br>$V_I$ = 0.45 V (DM80)<br>Other Inputs at 4.5 V | | $V_{CC}$ = Max | | −1.6 | | −1.6 | mA |
| | | Clock | | | | | −3.2 | | −3.2 | |
| | | Preset | | | | | −3.2 | | −3.2 | |
| | | Clear | | | | | −4.8 | | −4.8 | |
| | | J or $\overline{K}$ | | | $V_{CC}$ = Min | | −1.24 | | −1.41 | |
| | | Clock | | | | | −2.48 | | −2.82 | |
| | | Preset | | | | | −2.48 | | −2.82 | |
| | | Clear | | | | | −3.72 | | −4.23 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (1) | | | −30 | −85 | −30 | −85 | mA |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = 5 V, $T_A$ = 25°C (2) | | | | 28 | | 28 | mA |

**Note 1:** Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

**Note 2:** $I_{CC}$ is measured with all outputs open, first with preset at 4.5 V and all other inputs grounded, then with clear at 4.5 V and all other inputs grounded.

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## Switching Characteristics $V_{CC} = 5\ V,\ T_A = 25°C$

| Parameter | | From (Input) | To (Output) | Conditions | DM90/80 24 Min | DM90/80 24 Typ | DM90/80 24 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | | | | 30 | 40 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Preset | Q | $C_L = 15\ pF,\ R_L = 400\ \Omega$ | | 9 | 14 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Preset | $\overline{Q}$ | $C_L = 15\ pF,\ R_L = 400\ \Omega$ | | 18 | 29 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Clear | $\overline{Q}$ | $C_L = 15\ pF,\ R_L = 400\ \Omega$ | | 9 | 14 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Clear | Q | $C_L = 15\ pF,\ R_L = 400\ \Omega$ | | 17 | 25 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Clock | Q or $\overline{Q}$ | $C_L = 15\ pF,\ R_L = 400\ \Omega$ | | 12 | 18 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Clock | Q or $\overline{Q}$ | $C_L = 15\ pF,\ R_L = 400\ \Omega$ | | 19 | 28 | ns |
| $t_W$ | Pulse Width, Clock High | | | | 20 | | | ns |
| | Pulse Width, Clock Low | | | | 20 | | | ns |
| | Pulse Width, Preset or Clear Low | | | | 20 | | | ns |
| $t_{SETUP}$ | Input Setup Time (3) | | | | 15↑ | | | ns |
| $t_{HOLD}$ | Input Hold Time (3) | | | | 10↑ | | | ns |

**Note 3:** ↑ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge.

# 4-Bit Parallel-Access Shift Registers

## General Description

These 4-bit registers feature parallel inputs, parallel outputs, $J\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation: parallel (broadside) load and shift (in direction $Q_A$ toward $Q_D$).

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flops, and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

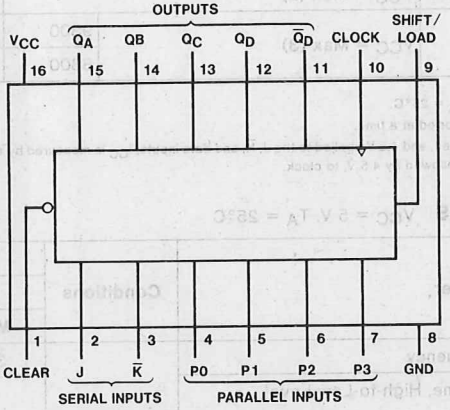
Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the $J\overline{K}$ inputs. These inputs permit the first stage to perform as a $J\overline{K}$, D or T-type flip-flop as shown in the truth table.

These shift registers are fully compatible with most other TTL and DTL families. All inputs, including the clock, are buffered to lower the drive requirements to one normalized Series 54/74 load.

## Features

- Direct replacement for Fairchild 9300
- Fully buffered inputs
- Direct overriding clear
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
- Positive edge-triggered clocking
- J and $\overline{K}$ inputs to first stage
- Typical shift frequency—39 MHz

## Connection Diagram




9300 (J,W); 8300 (N)

## Truth Table

| Inputs | | | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clear | Shift/ Load | Clock | Serial | | Parallel | | | | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $\overline{Q}_D$ |
| | | | J | $\overline{K}$ | P0 | P1 | P2 | P3 | | | | | |
| L | X | X | X | X | X | X | X | X | L | L | L | L | H |
| H | L | ↑ | X | X | a | b | c | d | a | b | c | d | $\overline{d}$ |
| H | H | L | X | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $\overline{Q}_{D0}$ |
| H | H | ↑ | L | H | X | X | X | X | $Q_{A0}$ | $Q_{A0}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |
| H | H | ↑ | L | L | X | X | X | X | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |
| H | H | ↑ | H | H | X | X | X | X | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |
| H | H | ↑ | H | L | X | X | X | X | $\overline{Q}_{An}$ | $Q_{An}$ | $Q_{Bn}$ | $Q_{Bn}$ | $\overline{Q}_{Cn}$ |

H = High Level (Steady State)
L = Low Level (Steady State)
X = Don't Care
↑ = Transition from low-to-high level
a, b, c, d = The level of steady state input at P0, P1, P2, or P3, respectively.
$Q_{A0}$, $Q_{B0}$, $Q_{C0}$, $Q_{D0}$ = The level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the indicated steady state input conditions were established.
$Q_{An}$, $Q_{Bn}$, $Q_{Cn}$ = The level of $Q_A$, $Q_B$ or $Q_C$, respectively, before the most recent ↑ transition of the clock.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM93/83 00 Min | DM93/83 00 Typ | DM93/83 00 Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −800 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −800 μA | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −18 | | −55 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | 9300 | | | 86 | mA |
| | | | 8300 | | | 92 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more that one output should be shorted at a time.

**Note 3:** With all outputs open, shift/load grounded, and 4.5 V applied to the J, $\overline{K}$, and data inputs, $I_{CC}$ is measured by applying a momentary ground, followed by 4.5 V, to clear, and then applying a momentary ground, followed by 4.5 V, to clock.

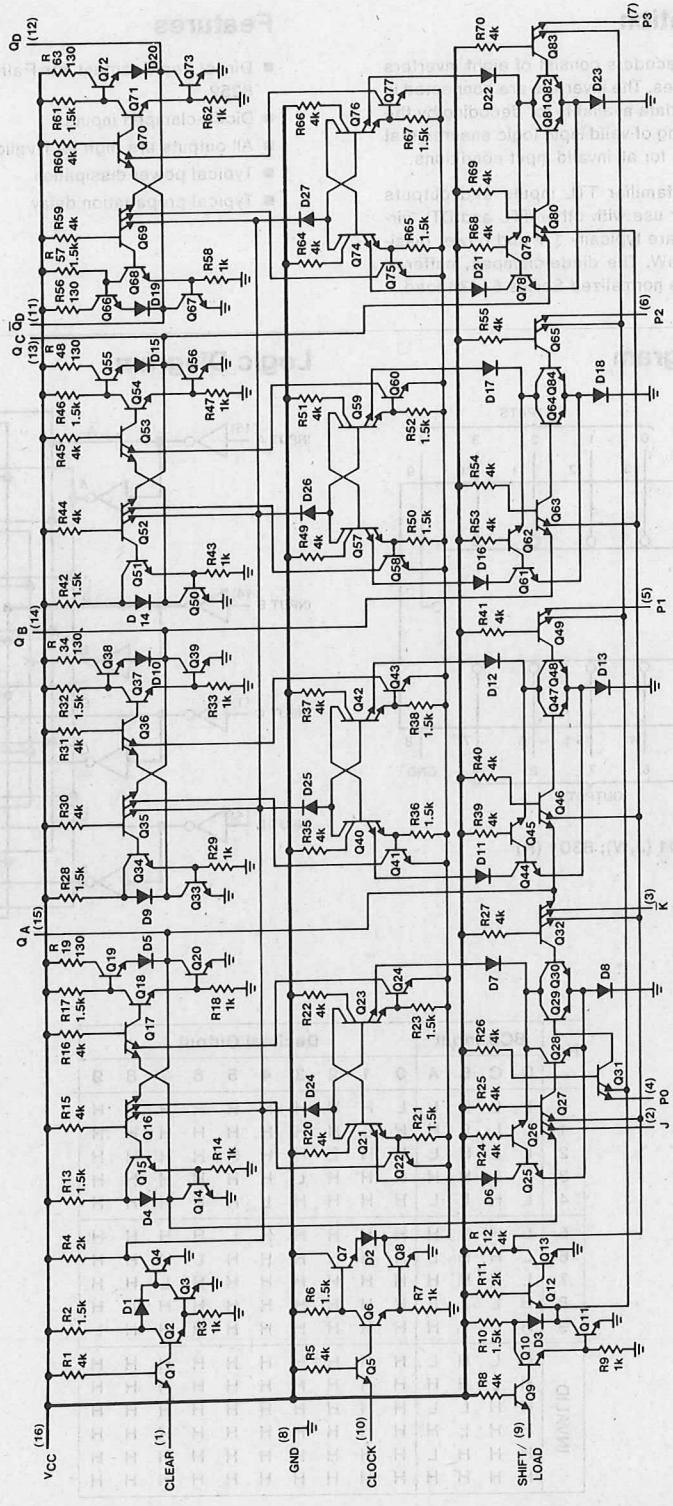
## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | Conditions | DM93/83 00 Min | DM93/83 00 Typ | DM93/83 00 Max | Units |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | | $C_L$ = 15 pF, $R_L$ = 400 Ω | 30 | 39 | | MHz |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level (Q) Output from Clear | | | | 19 | 30 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output from Clock | | | | 14 | 22 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output from Clock | | | | 17 | 26 | ns |
| $t_{W(CLOCK)}$ | Width of Clock Input Pulse | | | 16 | 11 | | ns |
| $t_{W(CLEAR)}$ | Width of Clear Input Pulse | | | 30 | 15 | | ns |
| $t_{SETUP}$ | Setup Time (4) | Shift/Load | | 30 | 13 | | ns |
| | | Serial and Parallel Data | | 20 | 13 | | |
| | | Clear Inactive-State | | 30 | 13 | | |
| $t_{RELEASE}$ | Shift/Load Release Time (5) | | | | | 10 | ns |
| $t_{HOLD}$ | Serial and Parallel Data Hold Time | | | 0 | −11 | | ns |

**Note 4:** SET UP TIME: $t_{SETUP}$ is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

**Note 5:** RELEASE TIME: $t_{RELEASE}$ is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) *not* to respond.

## Schematic Diagram



# 1 of 10 Decoders

## General Description

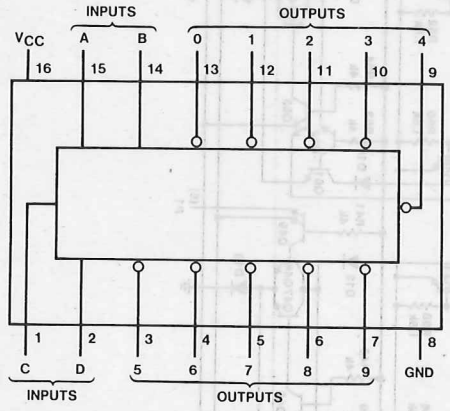
These BCD-to-decimal decoders consist of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain "OFF" for all invalid input conditions.

These circuits provide familiar TTL inputs and outputs which are compatible for use with other TTL and DTL circuits. DC noise margins are typically 1 V and power dissipation is typically 125 mW. The diode-clamped, buffered inputs represent only one normalized Series 54/74 load.

## Features

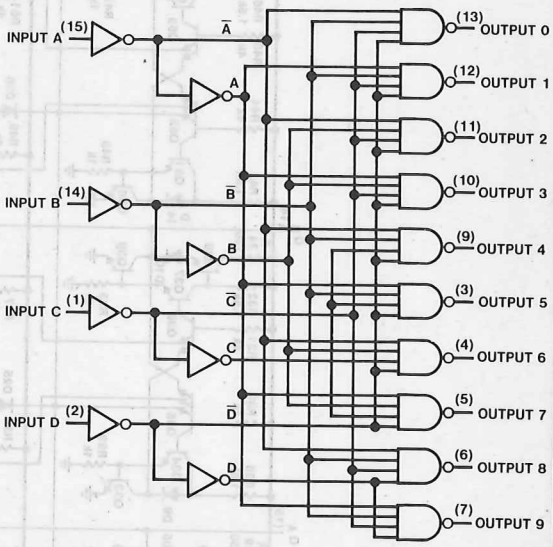
- Direct replacement for Fairchild 9301 and Signetics 8252
- Diode-clamped inputs
- All outputs are high for invalid BCD input conditions
- Typical power dissipation 125 mW
- Typical propagation delay 20 ns

## Connection Diagram




9301 (J,W); 8301 (N)

## Logic Diagram




## Truth Table

| No. | BCD Input | | | | Decimal Output | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0 | L | L | L | L | L | H | H | H | H | H | H | H | H | H |
| 1 | L | L | L | H | H | L | H | H | H | H | H | H | H | H |
| 2 | L | L | H | L | H | H | L | H | H | H | H | H | H | H |
| 3 | L | L | H | H | H | H | H | L | H | H | H | H | H | H |
| 4 | L | H | L | L | H | H | H | H | L | H | H | H | H | H |
| 5 | L | H | L | H | H | H | H | H | H | L | H | H | H | H |
| 6 | L | H | H | L | H | H | H | H | H | H | L | H | H | H |
| 7 | L | H | H | H | H | H | H | H | H | H | H | L | H | H |
| 8 | H | L | L | L | H | H | H | H | H | H | H | H | L | H |
| 9 | H | L | L | H | H | H | H | H | H | H | H | H | H | L |
| INVALID | H | L | H | L | H | H | H | H | H | H | H | H | H | H |
| | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | DM93/83 | | | Units |
|---|---|---|---|---|---|---|
| | | | 01 | | | |
| | | | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | −800 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OH}$ = −800 μA | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | −20 | | −55 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | 25 | 41 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.
**Note 3:** $I_{CC}$ is measured with the outputs open and all inputs grounded.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | DM93/83 | | | Units |
|---|---|---|---|---|---|---|
| | | | 01 | | | |
| | | | Min | Typ | Max | |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level, Any Output from A, B, C, or D | $C_L$ = 15 pF<br>$R_L$ = 400 Ω | | 19 | 30 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level, Any Output from A, B, C, or D | | | 20 | 30 | ns |

# Data Selectors/Multiplexers

## General Description

These data selectors/multiplexers contain inverter/drivers to supply full complementary, on-chip, binary decoded data selection to the AND-OR-INVERT gates.

The DM9309/8309 contains two separate 4-bit multiplexers with complementary Y and $\overline{Y}$ outputs; however, the two sections have common address select inputs.

The DM9312/8312 is a single 8-bit multiplexer with complementary outputs and a strobe control. When the strobe is low, the function is enabled. When a high logic level is applied to the strobe, the outputs are latched.

## Features

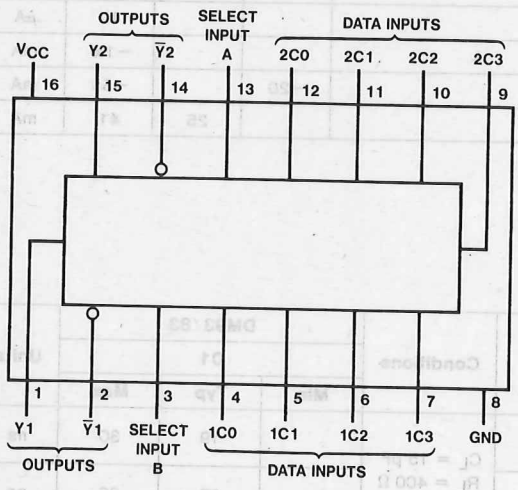
**DM9309/8309**

- Direct replacement for Fairchild 9309
- Complementary outputs
- Dual one-of-four data selectors

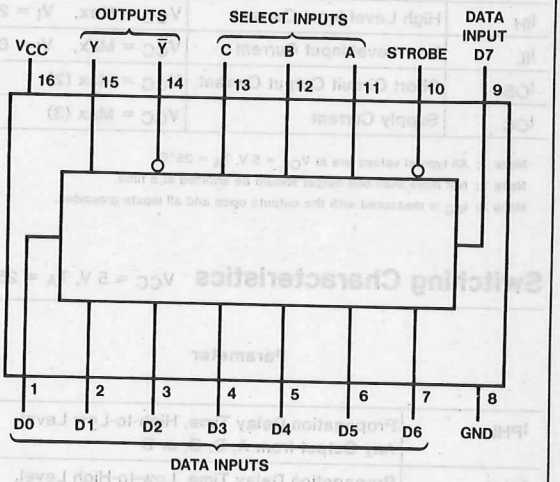
**DM9312/8312**

- Direct replacement for Fairchild 9312
- Selects one-of-eight data sources
- Performs parallel to serial conversion
- Strobe controlled outputs
- Complementary outputs

## Connection Diagrams




9309 (J,W); 8309 (N)




9312 (J,W); 8312 (N)

## Truth Tables

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| Inputs | | | | | | Outputs | |
|---|---|---|---|---|---|---|---|
| Select | | Data | | | | | |
| B | A | C0 | C1 | C2 | C3 | Y | $\overline{Y}$ |
| L | L | L | X | X | X | L | H |
| L | L | H | X | X | X | H | L |
| L | H | X | L | X | X | L | H |
| L | H | X | H | X | X | H | L |
| H | L | X | X | L | X | L | H |
| H | L | X | X | H | X | H | L |
| H | H | X | X | X | L | L | H |
| H | H | X | X | X | H | H | L |

Select inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care.

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| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| Select | | | Strobe | | |
| C | B | A | G | Y | $\overline{Y}$ |
| X | X | X | H | L | H |
| L | L | L | L | D0 | $\overline{D0}$ |
| L | L | H | L | D1 | $\overline{D1}$ |
| L | H | L | L | D2 | $\overline{D2}$ |
| L | H | H | L | D3 | $\overline{D3}$ |
| H | L | L | L | D4 | $\overline{D4}$ |
| H | L | H | L | D5 | $\overline{D5}$ |
| H | H | L | L | D6 | $\overline{D6}$ |
| H | H | H | L | D7 | $\overline{D7}$ |

H = High Level, L = Low Level, X = Don't Care.
D0, D1 . . . D7 = The level of the respective D input.

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | DM93/83 09, 12 Min | DM93/83 09, 12 Typ (1) | DM93/83 09, 12 Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | −800 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OH}$ = −800 μA | 2.4 | 3.4 | | V |
| $I_{OL}$ | Low Level Output Current | | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | 0.2 | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | −30 | | −85 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | 27 | 44 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25C.

**Note 2:** Not more than one output should be shorted at a time.

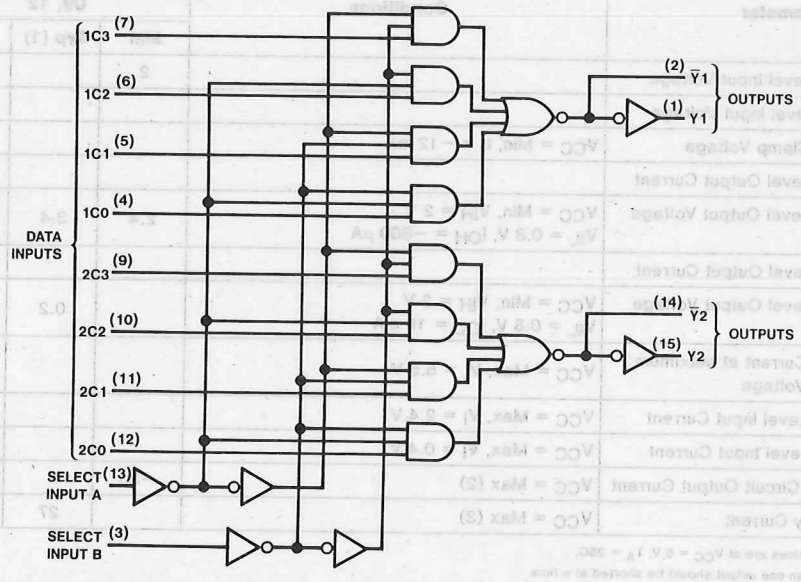
**Note 3:** $I_{CC}$ is measured with the outputs open and all inputs at 4.5 V for the DM9309/8309, and with the strobe and data select inputs at 4.5 V, all other inputs and outputs open for the DM9312/8312.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

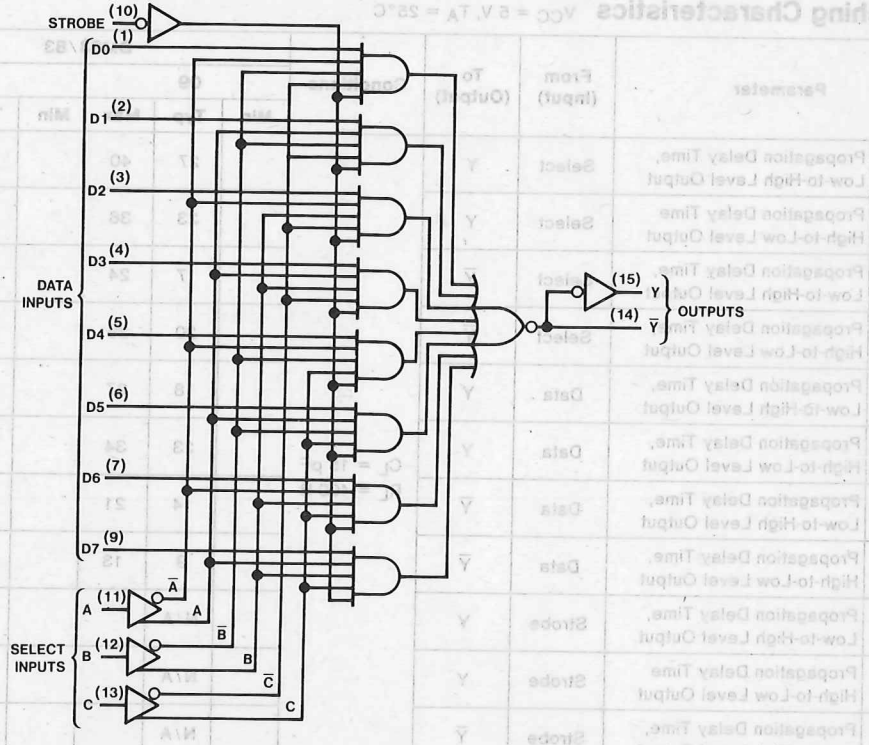
| Parameter | | From (Input) | To (Output) | Conditions | DM93/83 09 Min | 09 Typ | 09 Max | 12 Min | 12 Typ | 12 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Select | Y | $C_L$ = 15 pF<br>$R_L$ = 400 Ω | | 27 | 40 | | 22 | 33 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | Select | Y | | | 23 | 36 | | 23 | 35 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Select | $\overline{Y}$ | | | 17 | 24 | | 18 | 28 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Select | $\overline{Y}$ | | | 20 | 29 | | 16 | 25 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Y | | | 18 | 27 | | 16 | 23 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Data | Y | | | 23 | 34 | | 17 | 25 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | $\overline{Y}$ | | | 14 | 21 | | 9 | 13 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Data | $\overline{Y}$ | | | 9 | 13 | | 9 | 13 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Strobe | Y | | | N/A | | | 22 | 33 | ns |
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level Output | Strobe | Y | | | N/A | | | 21 | 32 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Strobe | $\overline{Y}$ | | | N/A | | | 13 | 19 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Strobe | $\overline{Y}$ | | | N/A | | | 15 | 21 | ns |

## Logic Diagrams

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## Synchronous 4-Bit Counters

## General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The DM9310/DM8310 are decade counters and the DM9316/DM8316 are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operating eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

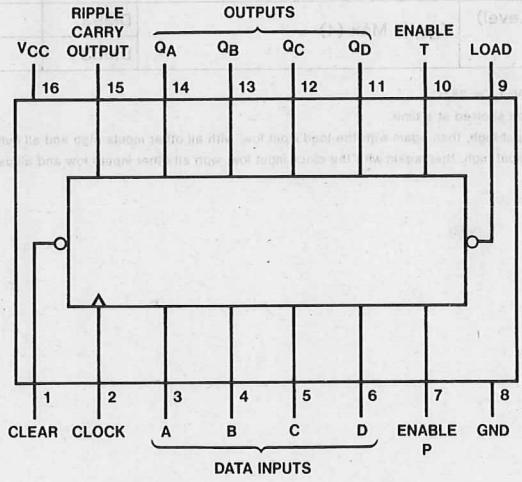
These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input. Low-to-high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs. The clear function is asynchronous and a low level at the clear input sets of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed-foward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the $Q_A$ output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs may occur regardless of the logic level in the clock.

## Features

- Direct replacement for Fairchild 9310, 9316
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical clock frequency 35 MHz
- Pin-for-pin replacements popular 54/74 counters
  9310 — 54160A/74160A (decade)
  9316 — 54161A/74161A (binary)

## Connection Diagram




9310 (J,W)
9316 (J,W)

8310 (N)
8316 (N)

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

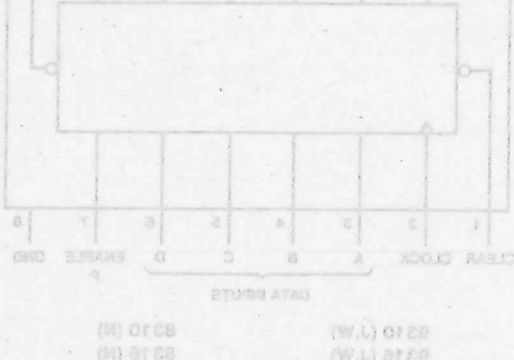
| Parameter | | | Conditions | | DM93/83 10, 16 Min | DM93/83 10, 16 Typ (1) | DM93/83 10, 16 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | | −800 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OH}$ = −800 μA | | 2.4 | 3.4 | | V |
| $I_{OL}$ | Low Level Output Current | | | | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | 0.2 | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | Clock or Enable T | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 80 | μA |
| | | Other Inputs | | | | | 40 | |
| $I_{IL}$ | Low Level Input Current | Clock or Enable T | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −3.2 | mA |
| | | Other Inputs | | | | | −1.6 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | DM93 | −20 | | −57 | mA |
| | | | | DM83 | −18 | | −57 | |
| $I_{CCH}$ | Supply Current (High Level) | | $V_{CC}$ = Max (3) | DM93 | | 59 | 85 | mA |
| | | | | DM83 | | 59 | 94 | |
| $I_{CCL}$ | Supply Current (Low Level) | | $V_{CC}$ = Max (4) | DM93 | | 63 | 91 | mA |
| | | | | DM83 | | 63 | 101 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time.

**Note 3:** $I_{CCH}$ is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

**Note 4:** $I_{CCL}$ is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.



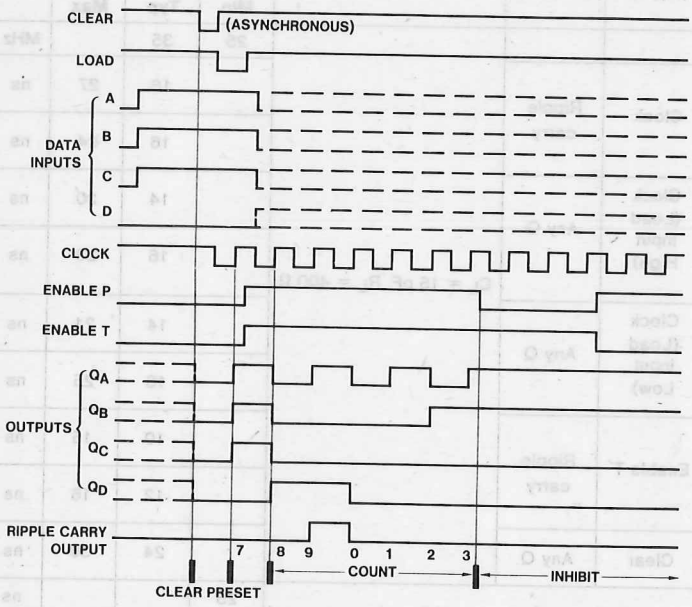
## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From (Input) | To (Output) | Conditions | DM93/83 10,16 Min | DM93/83 10,16 Typ | DM93/83 10,16 Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | | | | $C_L$ = 15 pF, $R_L$ = 400 Ω | 25 | 35 | | MHz |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock | Ripple carry | | | 18 | 27 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 16 | 24 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock (Load Input High) | Any Q | | | 14 | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 16 | 23 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Clock (Load Input Low) | Any Q | | | 14 | 21 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 18 | 25 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Enable T | Ripple carry | | | 10 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 12 | 16 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Clear | Any Q | | | 24 | 36 | ns |
| $t_{W(CLOCK)}$ | Width of Clock Pulse | | | | | 25 | | | ns |
| $t_{W(CLEAR)}$ | Width of Clear Pulse | | | | | 20 | | | ns |
| $t_{SETUP}$ | Setup Time | Data Inputs A, B, C, D | | | | 20 | | | ns |
| | | Enable P | | | | 20 | | | |
| | | Load | | | | 25 | | | |
| | | Clear | | | | 20 | | | |
| $t_{HOLD}$ | Hold Time at Any Input (5) | | | | | 0 | | | ns |

**Note 5:** The minimum hold time is as specified or as long as the clock input takes to rise from 0.8 V to 2 V, whichever is longer.

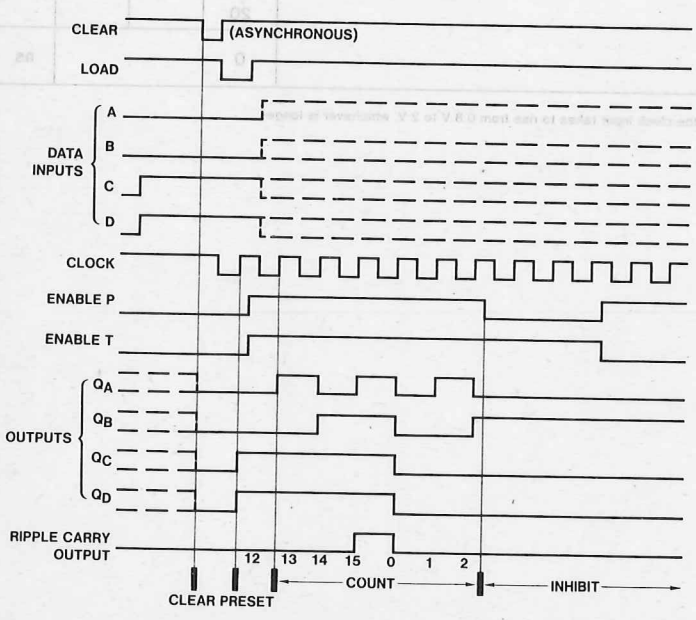
## Timing Diagrams

### 9310/8310 Synchronous Decade Counters
### Typical Clear, Preset, Count and Inhibit Sequences




**Sequence:**
(1) Clear outputs to zero
(2) Preset to BCD seven
(3) Count to eight, nine, zero, one, two, and three
(4) Inhibit

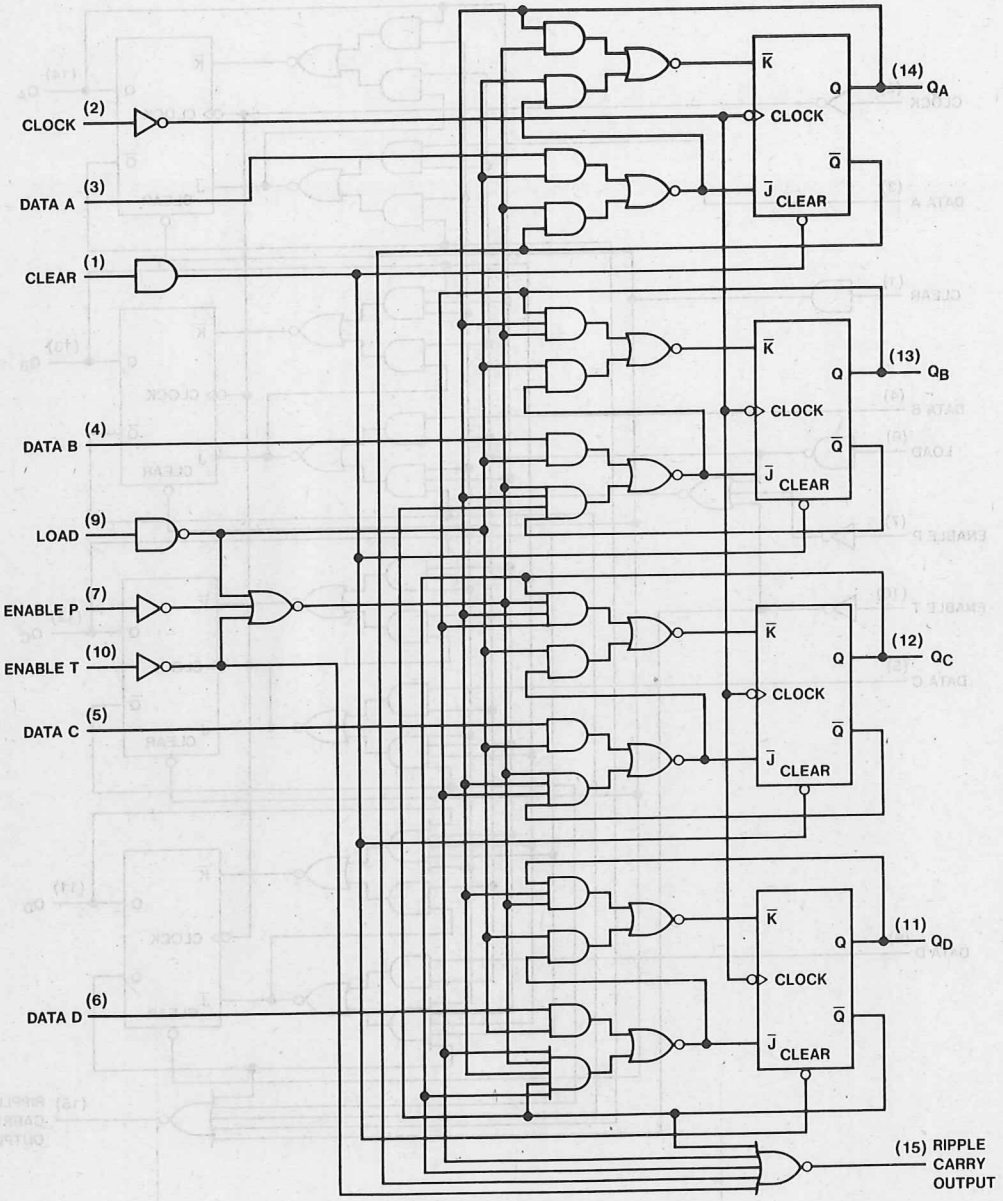
### 9316/8316 Synchronous Binary Counters
### Typical Clear, Preset, Count and Inhibit Sequences




**Sequence:**
(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one, and two
(4) Inhibit

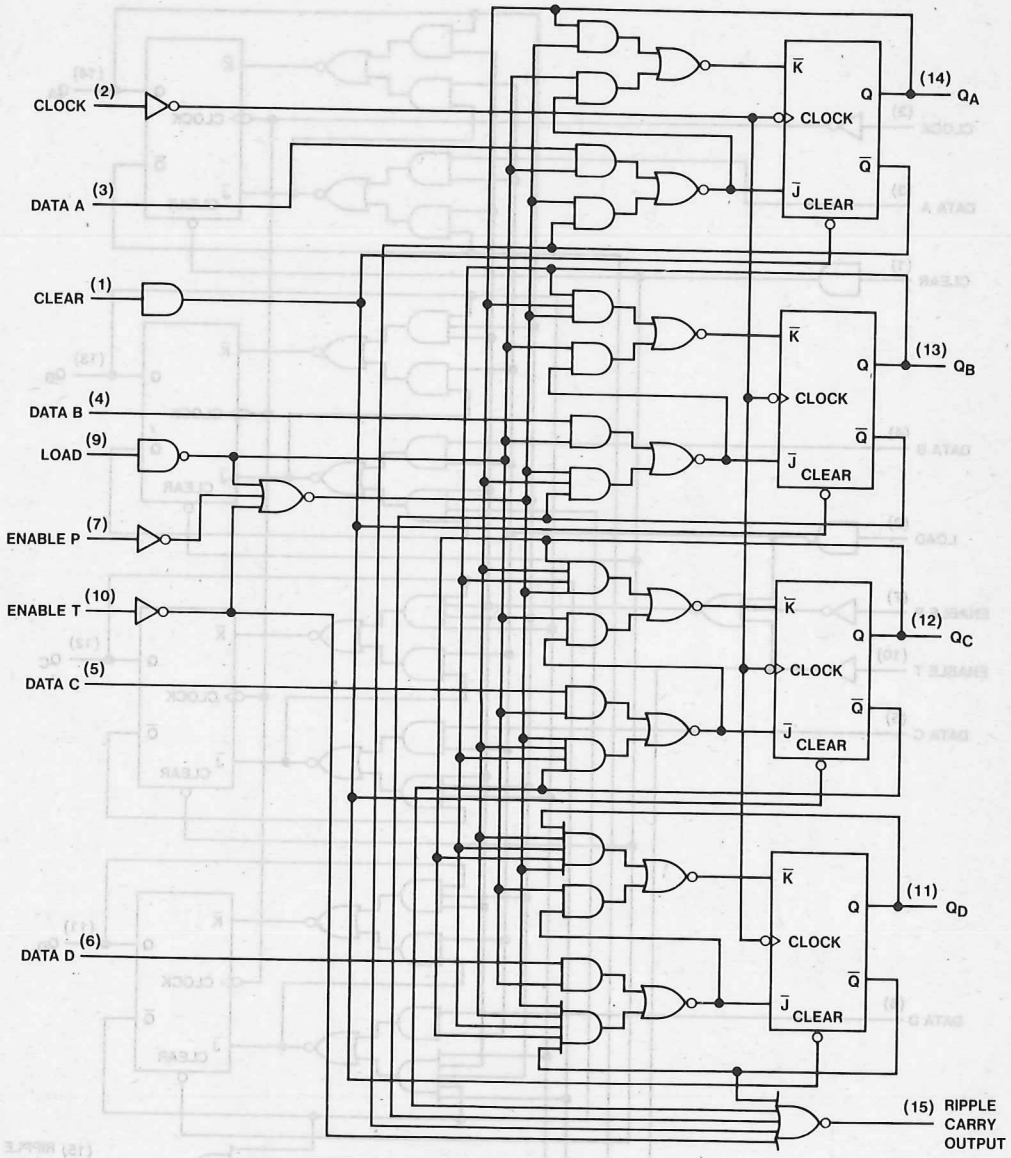
## Logic Diagrams

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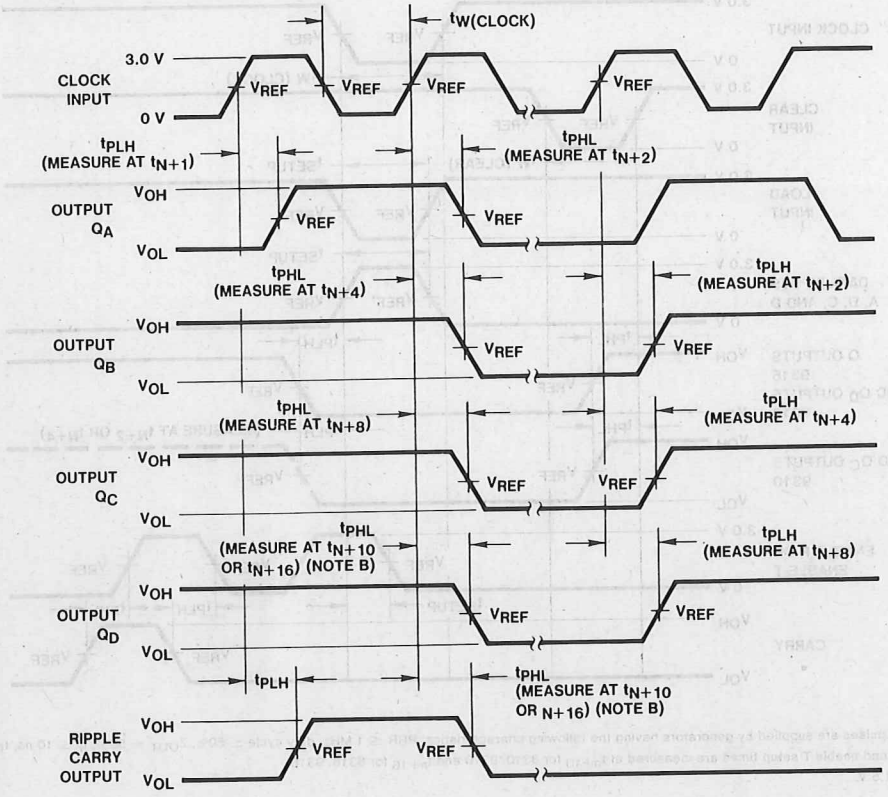
## Logic Diagrams (Continued)

16



## Parameter Measurement Information

### Switching Time Waveforms



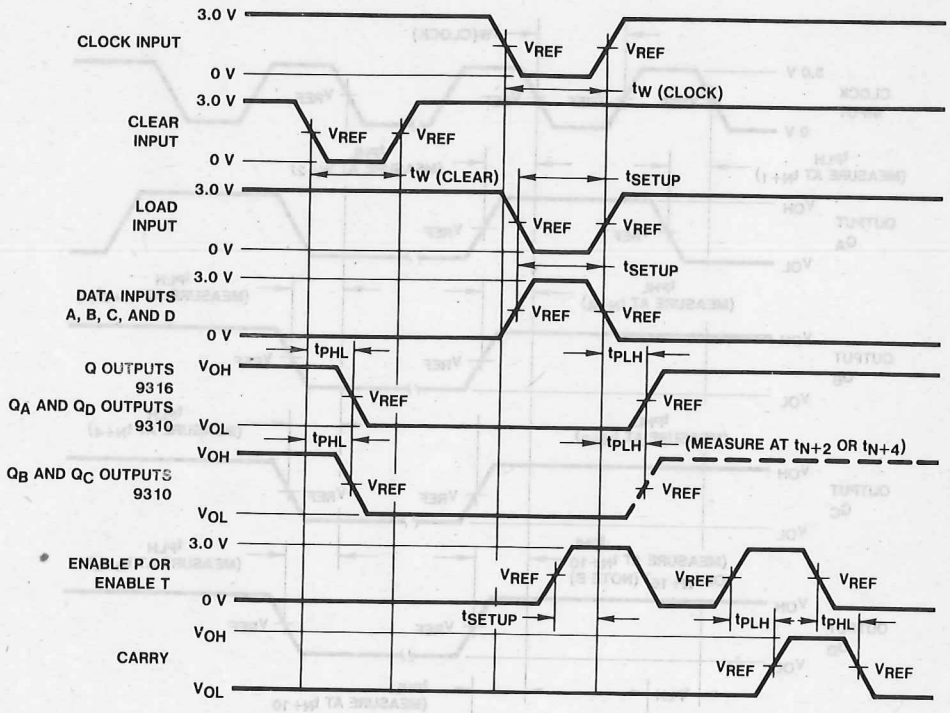

**Note A:** The input pulses are supplied by a generator having the following characteristics: PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\,\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure $f_{MAX}$.

**Note B:** Outputs $Q_D$ and carry are tested at $t_{n+10}$ for 9310/8310, and at $t_{n+16}$ for 9316/8316, where $t_n$ is the bit time when all outputs are low.

**Note C:** $V_{REF} = 1.5$ V.

## Parameter Measurement Information (Continued)

### Switching Time Waveforms




**Note A:** The input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\ \Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
**Note B:** Enable P and enable T setup times are measured at $t_{n+10}$ for 8310/9310 and $t_{n+16}$ for 8316/9316.
**Note C:** $V_{REF} = 1.5$ V.

# 4-Line to 16-Line Decoders/Demultiplexers

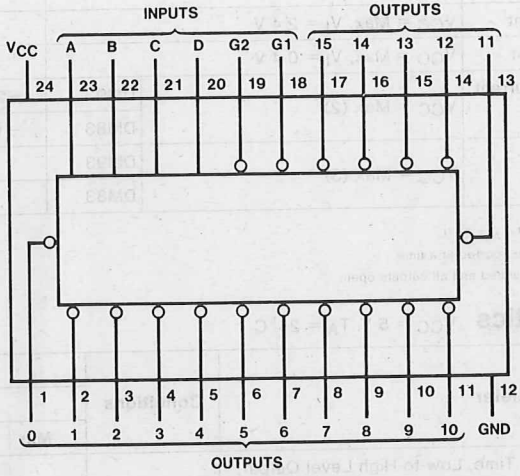
## General Description

Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

## Features

- Direct replacement for Fairchild 9311
- Pin for pin with popular 54154/74154
- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical propagation delay 19 ns
- Typical power dissipation 170 mW

## Connection Diagram




9311 (J,F); 8311 (J,N,F)

## Truth Table

| Inputs | | | | | | Outputs | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| G1 | G2 | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | L | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H |
| L | L | H | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H |
| L | L | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H |
| L | L | H | H | L | L | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H |
| L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H |
| L | L | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | L | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

H = High Level, L = Low Level, X = Don't Care

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

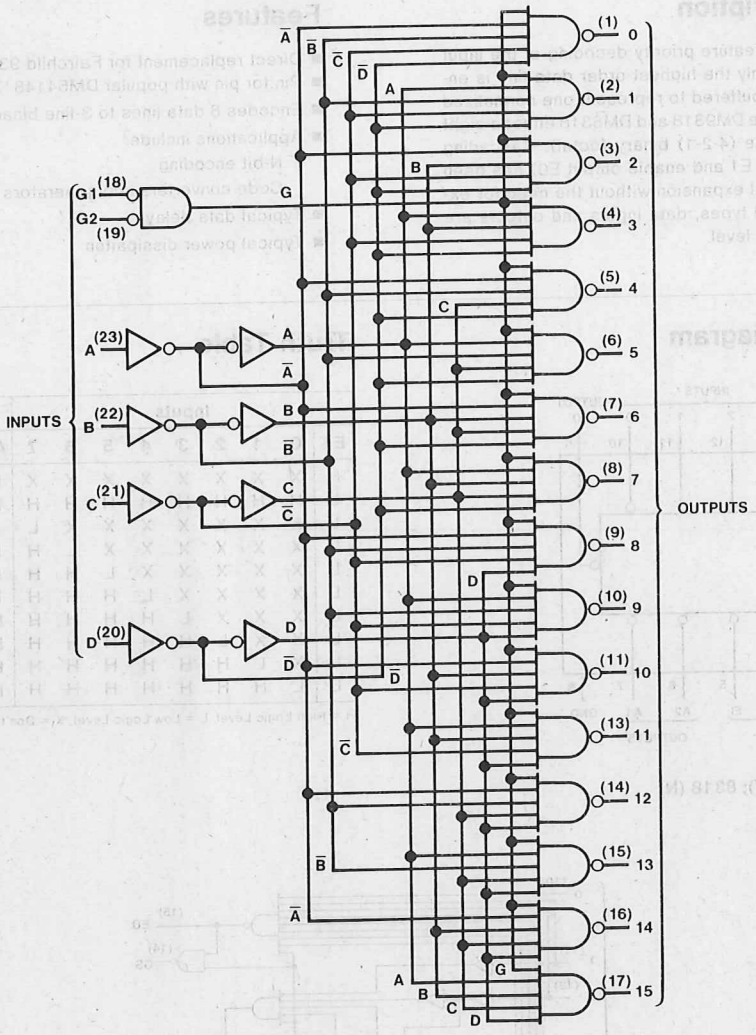
| Parameter | | Conditions | | DM93/83 | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | 11 | | | |
| | | | | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −800 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OH}$ = −800 μA | | 2.4 | 3.4 | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | 0.25 | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | DM93 | −20 | | −55 | mA |
| | | | DM83 | −18 | | −57 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | DM93 | | 34 | 49 | mA |
| | | | DM83 | | 34 | 56 | |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.
**Note 3:** $I_{CC}$ is measured with all inputs grounded and all outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | DM93/83 | | | Units |
|---|---|---|---|---|---|---|
| | | | 11 | | | |
| | | | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output, From A, B, C, or D Inputs Through 3 Levels of Logic | $C_L$ = 15 pF<br>$R_L$ = 400 Ω | | 18 | 27 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output, From A, B, C, or D Inputs Through 3 Levels of Logic | | | 21 | 30 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output, From Either Strobe Input | | | 17 | 25 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output, From Either Strobe Input | | | 18 | 27 | ns |

## Logic Diagram



# Priority Encoders

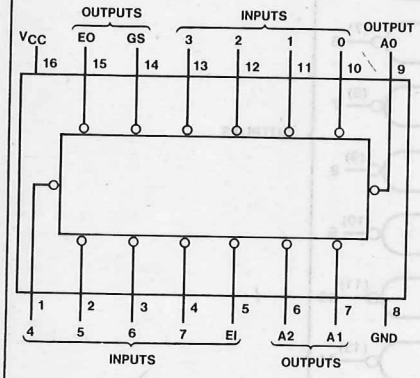
## General Description

These TTL encoders feature priority decoding of the input data to ensure that only the highest-order data line is encoded. All inputs are buffered to represent one normalized Series 54/74 load. The DM9318 and DM8318 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input E1 and enable output E0) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level.

## Features

- Direct replacement for Fairchild 9318
- Pin for pin with popular DM54148/74148
- Encodes 8 data lines to 3-line binary (octal)
- Applications include:
  - N-bit encoding
  - Code converters and generators
- Typical data delay 10 ns
- Typical power dissipaiton 190 mW

## Connection Diagram



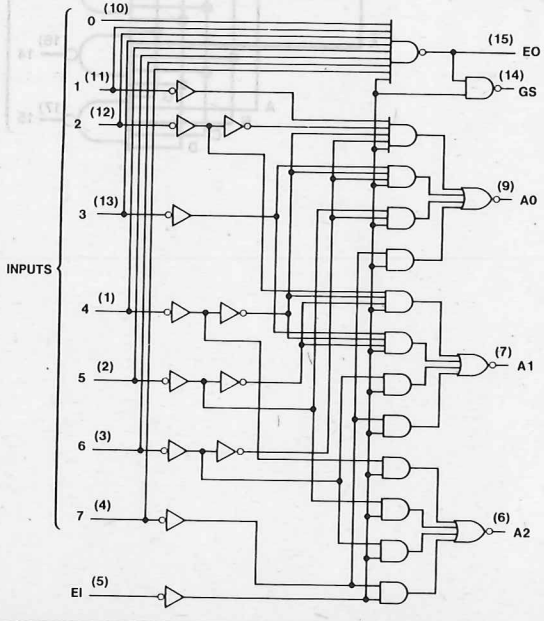

9318 (J,W); 8318 (N)

## Truth Table

| Inputs | | | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E1 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | A2 | A1 | A0 | GS | EO |
| H | X | X | X | X | X | X | X | X | H | H | H | H | H |
| L | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | X | X | X | X | X | X | X | L | L | L | L | L | H |
| L | X | X | X | X | X | X | L | H | L | L | H | L | H |
| L | X | X | X | X | X | L | H | H | L | H | L | L | H |
| L | X | X | X | X | L | H | H | H | L | H | H | L | H |
| L | X | X | X | L | H | H | H | H | H | L | L | L | H |
| L | X | X | L | H | H | H | H | H | H | L | H | L | H |
| L | X | L | H | H | H | H | H | H | H | H | L | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | L | H |

H = High Logic Level, L = Low Logic Level, X = Don't Care

## Logic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | | Conditions | | DM93/83 18 Min | DM93/83 18 Typ (1) | DM93/83 18 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | | −800 | μA |
| $V_{OH}$ | High Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OH}$ = −800 μA | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | 0 Input | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 40 | μA |
| | | Others | | | | | 80 | |
| $I_{IL}$ | Low Level Input Current | 0 Input | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | | −1.6 | mA |
| | | Others | | | | | −3.2 | |
| $I_{OS}$ | Short Circuit Output Current | | $V_{CC}$ = Max (2) | | −35 | | −85 | mA |
| $I_{CC}$ | Supply Current | | $V_{CC}$ = Max (3) | Condition 1 | | 40 | 60 | mA |
| | | | | Condition 2 | | 35 | 55 | |

**Note 1:** All typical value are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time.

**Note 3:** $I_{CC}$ (condition 1) is measured with inputs 7 and E1 grounded, other inputs and outputs open; $I_{CC}$ (condition 2) is measured with all inputs and outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| | Parameter | From (Input) | To (Output) | Waveform | Conditions | DM93/83 18 Min | DM93/83 18 Typ | DM93/83 18 Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | 0 thru 7 | A, B, C, D | In-Phase Output | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 10 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 9 | 14 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | 0 thru 7 | A, B, C, D | Out-of-Phase Output | | | 13 | 19 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 12 | 19 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | 0 thru 7 | EO | Out-of-Phase Output | | | 6 | 9 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 14 | 21 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | 0 thru 7 | GS | In-Phase Output | | | 18 | 27 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 14 | 21 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | E1 | AO, A1, or A2 | In-Phase Output | | | 10 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 10 | 15 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | E1 | GS | In-Phase Output | | | 8 | 12 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 10 | 15 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | E1 | EO | In-Phase Output | | | 10 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | | 17 | 26 | ns |

# Quad 2-Line to 1-Line Data Selectors/Multiplexers

## General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. True data is presented at the outputs.

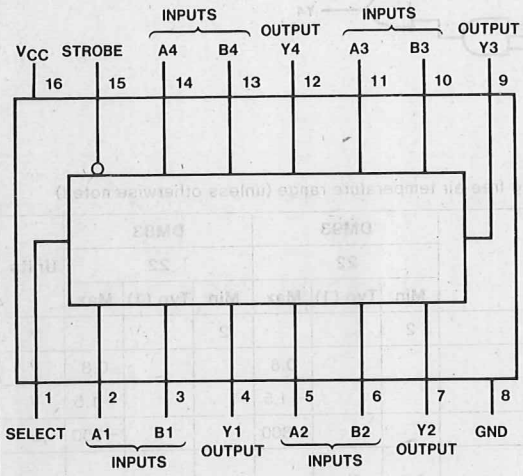
## Features

- Direct replacement for Fairchild 9322
- Pin-for-pin with popular DM54157/74157
- Buffered inputs and outputs

## Applications

- Expand any data input point
- Multiplex dual-data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

## Connection Diagram



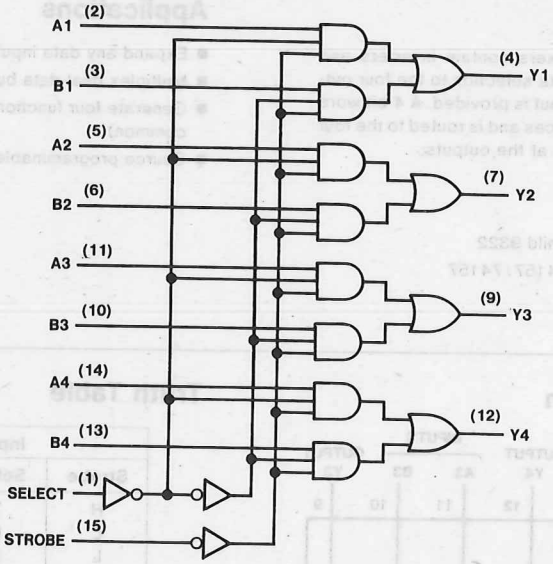

9322 (J,W); 8322 (N)

## Truth Table

| Inputs | | | | Output Y |
|---|---|---|---|---|
| Strobe | Select | A | B | |
| H | X | X | X | L |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |

H = High Level, L = Low Level, X = Don't Care

## Logic Diagram




## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | DM93 | | | DM83 | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 22 | | | 22 | | | |
| | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | −800 | | | −800 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OH}$ = −800μA | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| $I_{OL}$ | Low Level Output Current | | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V<br>$V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ =Max, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | −1.6 | | | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | −20 | | −55 | −18 | | −55 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (3) | | 30 | 48 | | 30 | 48 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C

**Note 2:** Not more than one output should be shorted at a time.

**Note 3:** $I_{CC}$ is measured with 4.5 V applied to all inputs and all outputs open.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | From (Input) | Conditions | DM93/83 22 | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 8 | 14 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | 10 | 14 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Strobe | | | 13 | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | 14 | 21 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Select | | | 15 | 23 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | 17 | 27 | ns |

# DM93/DM8334

## 8-Bit Addressable Latches

## General Description

The DM9334/DM8334 is a high speed 8-bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level high outputs. The device also incorporates an active level low common clear for resetting all latches, as well as an active level low enable.

The DM9334/DM8334 has four modes of operation which are shown in the mode selection table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the low state. In the clear mode all outputs are low and unaffected by the address and data inputs.

When operating the device as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The truth table below summarizes the operation of the product.

## Features

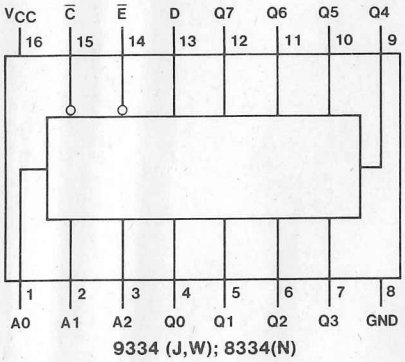
- Direct replacement for Fairchild 9334
- Common clear
- Easily expandable
- Random (addressable) data entry
- Serial to parallel capability
- 8 bits of storage/output of each bit available
- Active high demultiplexing/decoding capability

## Truth Tables

| $\overline{E}$ | $\overline{C}$ | MODE |
|---|---|---|
| L | H | Addressable Latch |
| H | H | Memory |
| L | L | Active High Eight Channel Demultiplexer |
| H | L | Clear |

X = Don't Care Condition
L = Low Voltage Level
H = High Voltage Level
$Q_{N-1}$ = Previous Output State

## Connection Diagram




9334 (J,W); 8334(N)

| Inputs | | | | | | Present Output States | | | | | | | | Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{C}$ | $\overline{E}$ | D | A0 | A1 | A2 | Q0 | Q1 | Q2 | Q3 | Q4 | Q5 | Q6 | Q7 | |
| L | H | X | X | X | X | L | L | L | L | L | L | L | L | Clear |
| L | L | L | L | L | L | L | L | L | L | L | L | L | L | Demultiplex |
| L | L | H | L | L | L | H | L | L | L | L | L | L | L | |
| L | L | L | H | L | L | L | L | L | L | L | L | L | L | |
| L | L | H | H | L | L | L | H | L | L | L | L | L | L | |
| • | • | • | | • | | | | | • | | | | | |
| • | • | • | | • | | | | | • | | | | | |
| • | • | • | | • | | | | | • | | | | | |
| L | L | H | H | H | H | L | L | L | L | L | L | L | H | |
| H | H | X | X | X | X | $Q_{N-1}$ | | | | | | | | Memory |
| H | L | L | L | L | L | L | $Q_{N-1}$ | $Q_{N-1}$ | $Q_{N-1}$ | | | | | Addressable Latch |
| H | L | H | L | L | L | H | $Q_{N-1}$ | $Q_{N-1}$ | | | | | | |
| H | L | L | H | L | L | $Q_{N-1}$ | L | $Q_{N-1}$ | | | | | | |
| H | L | H | H | L | L | $Q_{N-1}$ | H | $Q_{N-1}$ | | | | | | |
| • | • | • | | • | | | | • | | | | | | |
| • | • | • | | • | | | | • | | | | | | |
| • | • | • | | • | | | | • | | | | | | |
| H | L | L | H | H | H | $Q_{N-1}$ | | | | | | $Q_{N-1}$ | L | |
| H | L | H | H | H | H | $Q_{N-1}$ | | | | | | $Q_{N-1}$ | H | |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM93/83 34 Min | DM93/83 34 Typ (1) | DM93/83 34 Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −800 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −800 μA | | 2.4 | 3.6 | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | 0.2 | 0.4 | V |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | $\overline{E}$ Input | | 15 | 60 | μA |
| | | | Others | | 10 | 40 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | $\overline{E}$ Input | | −1.44 | −2.4 | mA |
| | | | Others | | −0.96 | −1.6 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −30 | −65 | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | 56 | 86 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

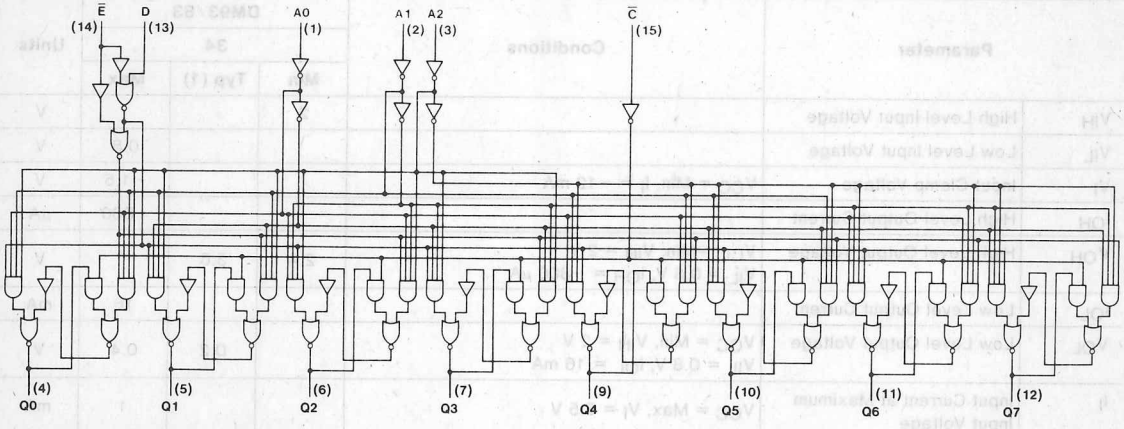
**Note 2:** Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

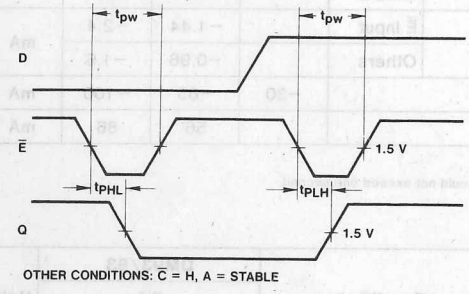
| Parameter | | From (Input) | To (Output) | Conditions | DM93/83 34 Min | DM93/83 34 Typ | DM93/83 34 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Enable | Output *(Figure 1)* | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 19 | 28 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 18 | 27 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Data | Output *(Figure 2)* | | | 24 | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 19 | 28 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Address | Output *(Figure 3)* | | | 23 | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | | | 21 | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Clear | Output *(Figure 5)* | | | 21 | 31 | ns |
| $t_W$ | Enable Pulse Width *(Figure 1)* | | | | 19 | 13 | | ns |
| $t_{SETUP}$ | High Data to Enable *(Figure 4)* | | | | 20 | 13 | | ns |
| | Low Data to Enable *(Figure 4)* | | | | 20 | 14 | | |
| | Address to Enable (3) *(Figure 6)* | | | | 10 | 5 | | |
| $t_{HOLD}$ | High Data to Enable *(Figure 4)* | | | | 0 | −10 | | ns |
| | Low Data to Enable (Figure 4) | | | | 0 | −13 | | ns |

**Note 3:** The Address to Enable Set-Up Time is the time before the High-to-Low Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

## Logic Diagram

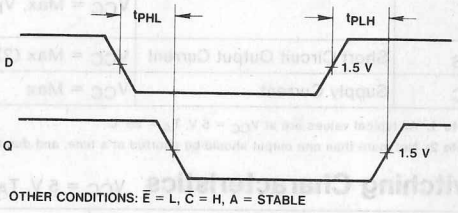



## Switching Time Waveforms



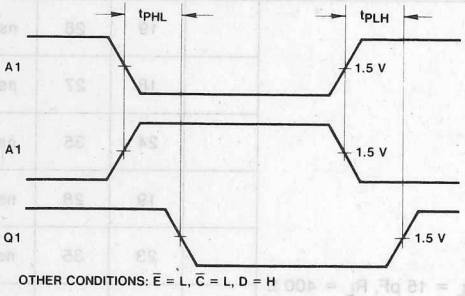

OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

FIGURE 1



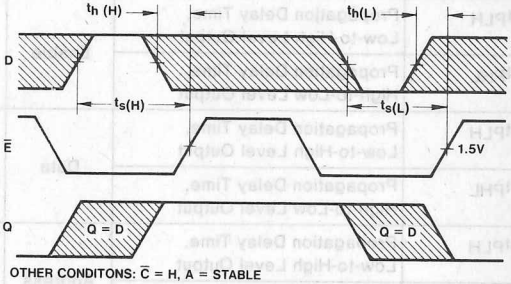

OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = H, A = STABLE

FIGURE 2



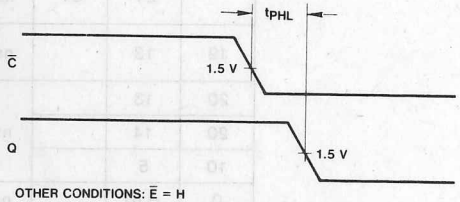

OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = L, D = H

FIGURE 3



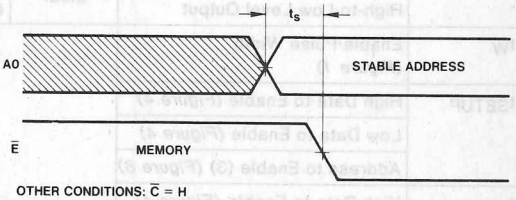

OTHER CONDITONS: $\overline{C}$ = H, A = STABLE

FIGURE 4




OTHER CONDITIONS: $\overline{E}$ = H

FIGURE 5




OTHER CONDITIONS: $\overline{C}$ = H

FIGURE 6

**Note:** The shaded areas indicate when the inputs are permitted to change for predictable output performance.

# Retriggerable One Shots

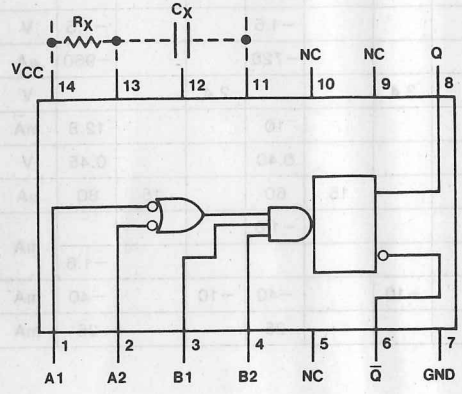
## General Description

These retriggerable one shots provide the designer with four inputs; two active high and two active low. This permits a choice of either leading-edge or trailing-edge triggering, independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge again. The retriggerable feature allows for output pulse widths to be expanded. In fact a continuous true output can be maintained by havjng an input cycle time which is shorter than the output cycle time. Retriggering may be inhibited by tying the $\overline{Q}$ output to an active low input.

## Features

- High speed operation—input repetition rate > 10 MHz
- Flexibility of operation—optional retriggering/lock-out capability
- Output pulse width range—50 ns to ∞
- Leading or trailing edge triggering
- Complementary outputs/inputs
- Input clamping diodes
- DTL/TTL compatible logic levels

## Connection Diagram

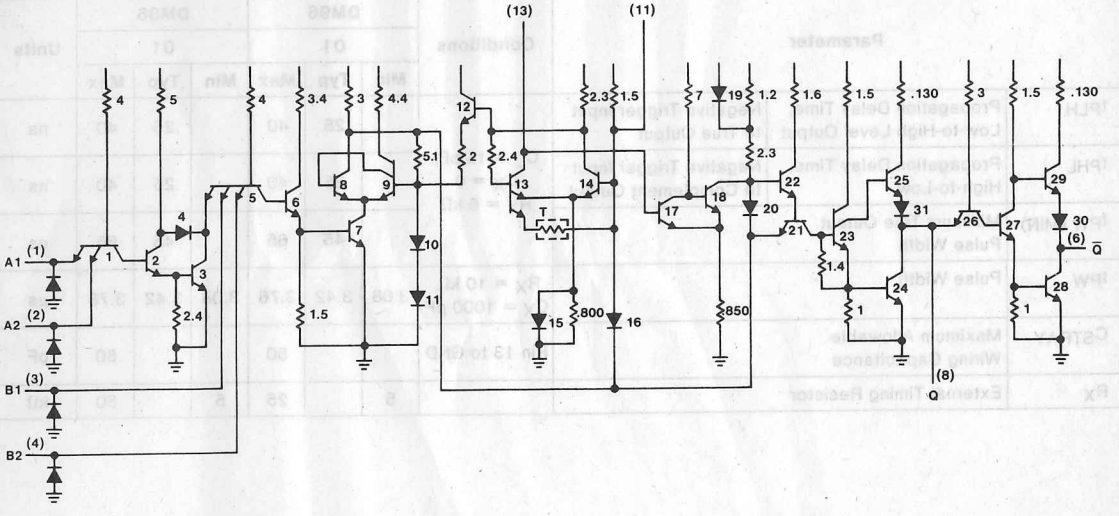



9601 (J,W); 8601 (N)

## Truth Table

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| A1 | A2 | B1 | B2 | Q | $\overline{Q}$ |
| H | H | X | X | L | H |
| X | X | L | X | L | H |
| X | X | X | L | L | H |
| L | X | H | H | L | H |
| L | X | ↑ | H | ⎍ | ⎍ |
| L | X | H | ↑ | ⎍ | ⎍ |
| X | L | H | H | L | H |
| X | L | ↑ | H | ⎍ | ⎍ |
| X | L | H | ↑ | ⎍ | ⎍ |
| H | ↓ | H | H | ⎍ | ⎍ |
| ↓ | ↓ | H | H | ⎍ | ⎍ |
| ↓ | H | H | H | ⎍ | ⎍ |

## Schematic Diagram



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM96 01 | | | DM86 01 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | $T_A = -55°C$ | | 2.0 | | | | | | V |
| | | $T_A = 0°C$ | | | | | 1.9 | | | |
| | | $T_A = 25°C$ | | 1.7 | | | 1.8 | | | |
| | | $T_A = 75°C$ | | | | | 1.6 | | | |
| | | $T_A = 125°C$ | | 1.5 | | | | | | |
| $V_{IL}$ | Low Level Input Voltage | $T_A = -55°C$ | | | | 0.85 | | | | V |
| | | $T_A = 0°C$ | | | | | | | 0.85 | |
| | | $T_A = 25°C$ | | | | 0.90 | | | 0.85 | |
| | | $T_A = 75°C$ | | | | | | | 0.85 | |
| | | $T_A = 125°C$ | | | | 0.85 | | | | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I = -12$ mA | | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −720 | | | −960 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = Max | | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 10 | | | 12.8 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max | | | | 0.40 | | | 0.45 | V |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 4.5 V | | | 15 | 60 | | 15 | 60 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.40 V | | | −1.6 | | | | mA |
| | | | $V_I$ = 0.45 V | | | | | | −1.6 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −10 | | −40 | −10 | | −40 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | | 25 | | | 25 | mA |

**Note 1:** All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

**Note 2:** Not more than one output should be shorted at a time.

**Note 3:** Unless otherwise specified, $R_X = 10$ kΩ between Pin 13 and $V_{CC}$ on all tests.

**Note 4:** Ground Pin 11 for $V_{OL}$ test on Pin 6, $V_{OH}$ test on Pin 8 and $I_{OS}$ test on Pin 8. Open Pin for $V_{OL}$ test on Pin 8, $V_{OH}$ test on Pin 6 and $I_{OS}$ test on Pin 6.

## Switching Characteristics $V_{CC} = 5$ V, $T_A = 25°C$

| Parameter | | | Conditions | DM96 01 | | | DM86 01 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Negative Trigger Input to True Output | $C_L = 15$ pF, $C_X = 0$, $R_X = 5$ kΩ | | 25 | 40 | | 25 | 40 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low | Negative Trigger Input to Complement Output | | | 25 | 40 | | 25 | 40 | ns |
| $t_{PW\ (MIN)}$ | Minimum True Output Pulse Width | | | | 45 | 65 | | 45 | 65 | ns |
| $t_{PW}$ | Pulse Width | | $R_X = 10$ kΩ, $C_X = 1000$ pF | 3.08 | 3.42 | 3.76 | 3.08 | 3.42 | 3.76 | μs |
| $C_{STRAY}$ | Maximum Allowable Wiring Capacitance | | Pin 13 to GND | | | 50 | | | 50 | pF |
| $R_X$ | External Timing Resistor | | | 5 | | 25 | 5 | | 50 | kΩ |

## Operating Rules

1. An external resistor $R_X$ and an external capacitor $C_X$ are required for operation. The value of $R_X$ can vary between the limits shown in switching characteristics. The value of $C_X$ is optional and may be adjusted to achieve the required output pulse width.
2. Output pulse width $t_{PW}$ may be calculated as follows:

$$t_{PW} = 0.32\, R_X C_X \left[1 + \frac{0.7}{R_X}\right] \text{ (for } C_X \geq 10^3 \text{ pF)}$$

$R_X$ in kΩ, $C_X$ in pF and $t_{PW}$ in ns.
(For $C_X < 10^3$ pF, see curve.)

3. $R_X$ and $C_X$ must be kept as close as possible to the circuit in order to minimize stray capacitance and noise pickup. If remote trimming is required, $R_X$ may be split up such that at least $R_{X(MIN)}$ must be as close as possible to the circuit and the remote portion of the trimming resistor $R < R_{X(MAX)} - R_X$.
4. Set-up time ($t_1$) for input trigger pulse must be > 40 ns. (See *Figure 1*).
   Release time ($t_2$) for input trigger pulse must be > 40 ns. (See *Figure 2*).
5. Retrigger pulse width (see *Figure 3*) is calculated as follows:

$$t_W = t_{PW} + t_{PLH} = 0.32\, R_X C_X \left[1 + \frac{0.7}{R_X}\right] + t_{PLH}$$

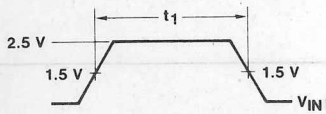



FIGURE 1

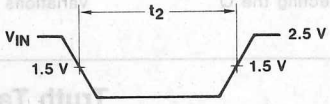



FIGURE 2

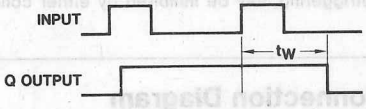
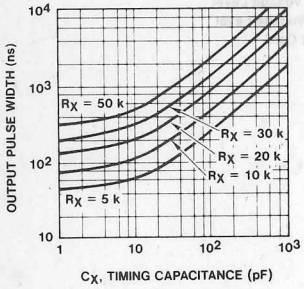


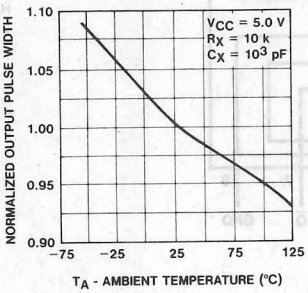

FIGURE 3

## Typical Performance Characteristics

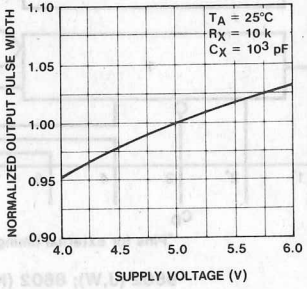
**Output Pulse Width vs Timing Resistance And Capacitance For $C_X < 10^3$ pF**



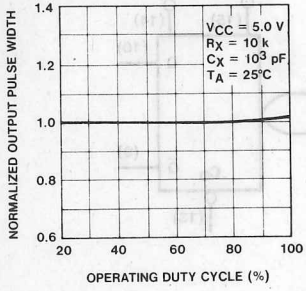

**Normalized Output Pulse Width vs Ambient Temperature**



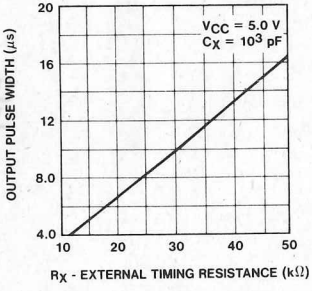

**Normalized Output Pulse Width vs Supply Voltage**



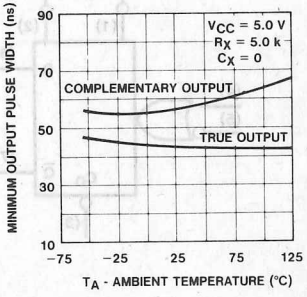

**Normalized Output Pulse Width vs Operating Duty Cycle**




**Pulse Width vs Timing Resistance**




**Output Pulse Width vs Ambient Temperature**



# Dual Retriggerable, Resettable One Shots

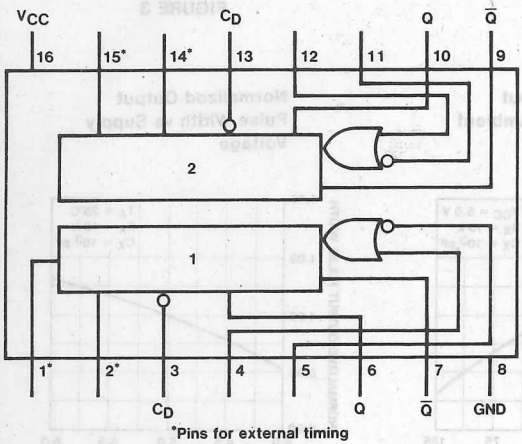
## General Description

These dual resettable, retriggerable one shots have two inputs per function; one which is active high, and one which is active low. This allows the designer to employ either leading-edge or trailing-edge triggering, which is independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is allowed to rapidly discharge and then charge again. The retriggerable feature permits output pulse widths to be extended. In fact a continuous true output can be maintained by having an input cycle time which is shorter than the output cycle time. The output pulse may then be terminated at any time by applying a low logic level to the RESET pin. Retriggering may be inhibited by either connecting the Q output to an active high input, or the $\overline{Q}$ output to an active low input.

## Features

- 70 ns to ∞ output width range
- Resettable and retriggerable—0% to 100% duty cycle
- TTL input gating—leading or trailing edge triggering
- Complementary TTL outputs
- Optional retrigger lock-out capability
- Pulse width compensated for $V_{CC}$ and temperature variations

## Connection Diagram




*Pins for external timing

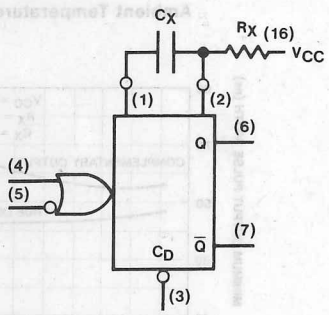
9602 (J,W); 8602 (N)

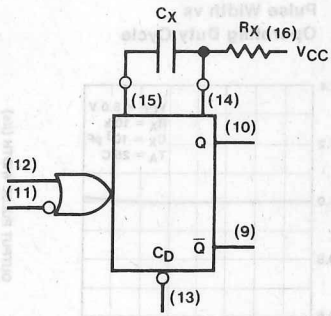
## Truth Table

| Pin No's. | | | Operation |
|---|---|---|---|
| 5(11) | 4(12) | 3(13) | |
| H→L | L | H | Trigger |
| H | L→H | H | Trigger |
| X | X | L | Reset |

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

## Logic Diagrams



## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM96 02 | | | DM86 02 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | $T_A = -55°C$ | | 2.0 | | | | | | V |
| | | $T_A = 0°C$ | | | | | 1.9 | | | |
| | | $T_A = 25°C$ | | 1.7 | | | 1.8 | | | |
| | | $T_A = 75°C$ | | | | | 1.65 | | | |
| | | $T_A = 125°C$ | | 1.5 | | | | | | |
| $V_{IL}$ | Low Level Input Voltage | $T_A = -55°C$ | | | | 0.85 | | | | V |
| | | $T_A = 0°C$ | | | | | | | 0.85 | |
| | | $T_A = 25°C$ | | | | 0.90 | | | 0.85 | |
| | | $T_A = 75°C$ | | | | | | | 0.85 | |
| | | $T_A = 125°C$ | | | | 0.85 | | | | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −800 | | | −800 | μA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = Min, $V_{IL}$ = Max, $I_{OH}$ = −800 μA (4) | | 2.4 | | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = Min, $V_{IL}$ = Max, $I_{OL}$ = 16 mA (4) | | | | 0.40 | | | 0.45 | V |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 4.5 V | | | 10 | 60 | | 10 | 60 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max | $V_I$ = 0.40 V | | | −1.6 | | | | mA |
| | | | $V_I$ = 0.45 V | | | | | | −1.6 | |
| | | $V_{CC}$ = Min | $V_I$ = 0.40 V | | | −1.24 | | | | |
| | | | $V_I$ = 0.45 V | | | | | | −1.41 | |
| $I_{OS}$ | Short Circuit Output Current | VCC = Max (2) (4) | | | | −25 | | | −35 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | 39 | 45 | | 39 | 50 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time.

**Note 3:** Unless otherwise noted, $R_X$ = 10 kΩ for all tests.

**Note 4:** Ground Pin 1 (15) for $V_{OL}$ on Pin 7 (9), or for $V_{OH}$ on Pin 6 (10), or for $I_{OS}$ on Pins 6 (10); also, apply momentary ground to Pin 4 (12). Open Pin 1 (15) for $V_{OL}$ on Pin 6 (10), or for $V_{OH}$ on Pin 7 (9), or for $I_{OS}$ on Pin 7 (9).

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | Conditions | DM96 02 Min | DM96 02 Typ | DM96 02 Max | DM86 02 Min | DM86 02 Typ | DM86 02 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | Negative Trigger Input to True Output | $C_L$ = 15 pF, $C_X$ = 0, $R_X$ = 5 kΩ | | 25 | 35 | | 25 | 40 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | Negative Trigger Input To Complement Output | | | 29 | 43 | | 29 | 48 | ns |
| $t_{PW}$ (MIN) | Minimum True Output Pulse Width | | | | 72 | 90 | | 72 | 100 | ns |
| | Minimum Complement Pulse Width | | | | 78 | 100 | | 78 | 110 | |
| $t_{PW}$ | Pulse Width | | $R_X$ = 10 kΩ, $C_X$ = 1000 pF | 3.08 | 3.42 | 3.76 | 3.08 | 3.42 | 3.76 | μs |
| $C_{STRAY}$ | Maximum Allowable Wiring Capacitance | | Pins 2, 14 to GND | | | 50 | | | 50 | pF |
| $R_X$ | External Timing Resistor | | | 5 | | 25 | 5 | | 50 | kΩ |

## Operating Rules

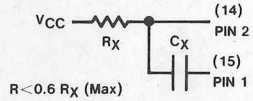
1. An external resistor ($R_X$) and external capacitor ($C_X$) are required as shown in the Logic Diagram.
2. The value of $C_X$ may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
3. The output pulse with (t) is defined as follows:

$$t \approx 0.31\, R_X C_X \left[1 + \frac{1}{R_X}\right]$$

where $R_X$ is in kΩ, $C_X$ is in pF
t is in ns
for $C_X < 10^3$ pF, see *Figure 1*.

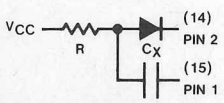
4. If electrolytic type capacitors are to be used, the following three configurations are recommended:

A. Use with low leakage capacitors:
The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 V is less than 3 μA, and the inverse capacitor leakage at 1.0 V is less than 5 μA over the operational temperature range.



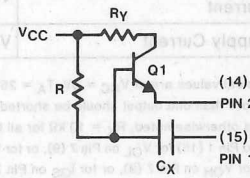

B. Use with high inverse leakage current electrolytic capacitors:
The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.

$$t \approx 0.3\, RC_X$$



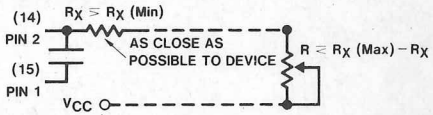

C. Use to obtain extended pulse widths:
This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electrolytics with high inverse leakage currents can be used.
$R < R_X$ (0.7) ($h_{FE}$ Q1) or < 2.5 MΩ, whichever is the lesser
$R_X$ (min) < $R_Y$ < $R_X$ (max)
(5 kΩ ≤ $R_Y$ ≤ 10 kΩ is recommended)
Q1: NPN silicon transistor with $h_{FE}$ requirements of above equations, such as 2N5961 or 2N5962.

$$t \approx 0.3\, RC_X$$




This configuration is not recommended with retriggerable operation.

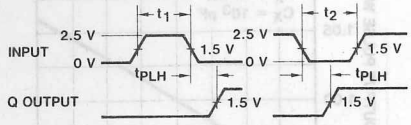
5. To obtain variable pulse width by remote trimming, the following circuit is recommended:




6. Under any operating condition, $C_X$ and $R_X$ (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.

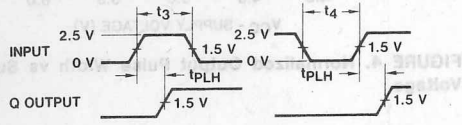
## Operating Rules (Continued)

7. Input Trigger Pulse Rules (See Triggering Truth Table)




Input to Pin 5 (11), (Pin 3 (13) = HIGH)
Pin 4 (12) = LOW

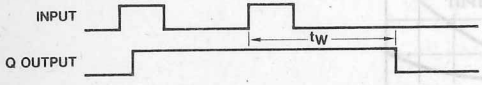
$t_1$, $t_3$ = Min. Positive Input Pulse Width > 40 ns
$t_2$, $t_4$ = Min. Negative Input Pulse Width > 40 ns




Input to Pin 4 (12) (Pin 3 (13) = HIGH)
Pin 5 (11) = HIGH

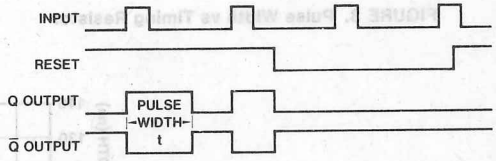
8. The retriggerable pulse width is calculated as shown below:

$$t_W = t + t_{PLH} = 0.31\, R_X\, C_X \left(1 + \frac{1}{R_X}\right) + t_{PLH}$$




The retrigger pulse width is equal to the pulse width (t) plus a delay time. For pulse widths greater than 500 ns, $t_W$ can be approximated as t. Retriggering will not occur if the retrigger pulse comes within ≈ 0.3 $C_X$ (ns) after the initial trigger pulse (i.e., during the discharge cycle).

9. Reset Operation — An overriding clear (active LOW level) is provided on each one shot. By applying a LOW to the reset, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW.




10. $V_{CC}$ and Ground wiring should conform to good high frequency standards so that switching transients on $V_{CC}$ and Ground leads do not cause interaction between one shots. Use of a 0.01 to 0.1 μF bypass capacitor between $V_{CC}$ and Ground located near the DM9602/DM8602 is recommended.

## Typical Performance Characteristics

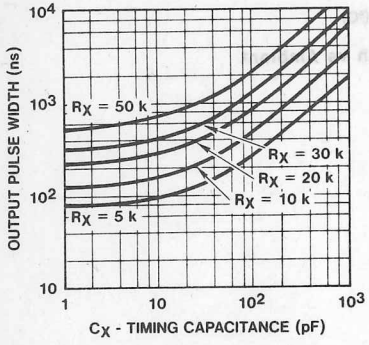



**FIGURE 1. Output Pulse Width vs Timing Resistance and Capacitance For $C_X < 10^3$ pF**

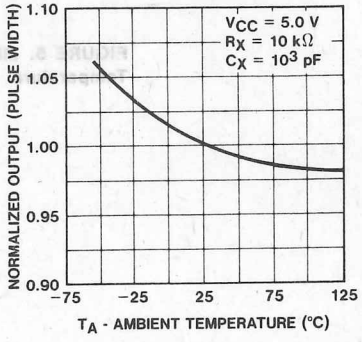



**FIGURE 2. Normalized Output Pulse Width vs Ambient Temperature**

## Typical Performance Characteristics (Continued)

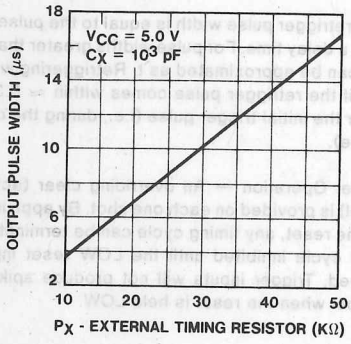



FIGURE 3. Pulse Width vs Timing Resistor

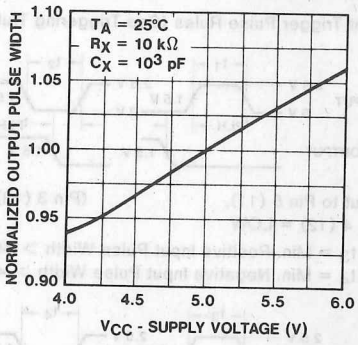



FIGURE 4. Normalized Output Pulse Width vs Supply Voltage

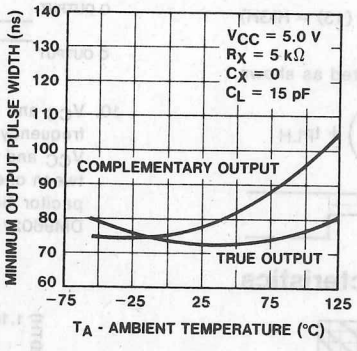



FIGURE 5. Minimum Output Pulse Width vs Ambient Temperature

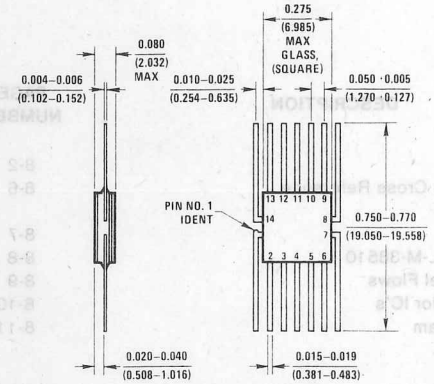
# Section 8
# Appendices/ Physical Dimensions

8

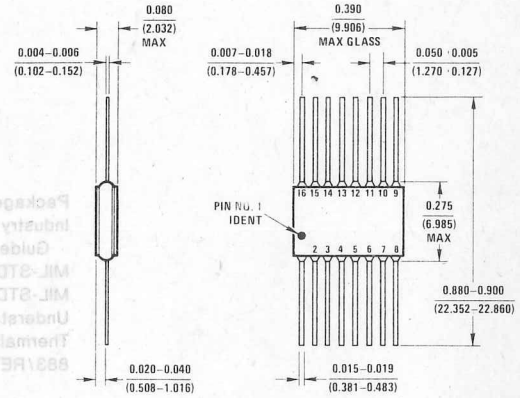

| DESCRIPTION | PAGE NUMBER |
|---|---|
| Packages | 8-2 |
| Industry Package Cross Reference Guide | 8-6 |
| MIL-STD-883 | 8-7 |
| MIL-STD-883/MIL-M-38510 | 8-8 |
| Understanding Rel Flows | 8-9 |
| Thermal Ratings for IC's | 8-10 |
| 883/RETS Program | 8-11 |

## Physical Dimensions

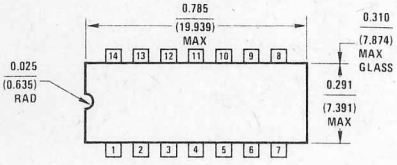
All dimensions in inches (millimeters)

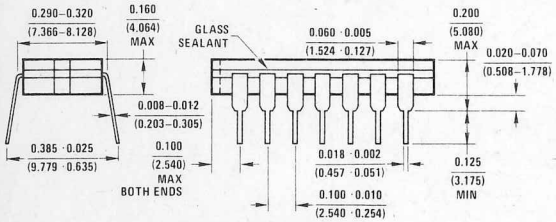



NS Package F14A
14-Lead Flat Package (F)

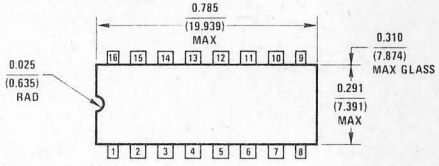


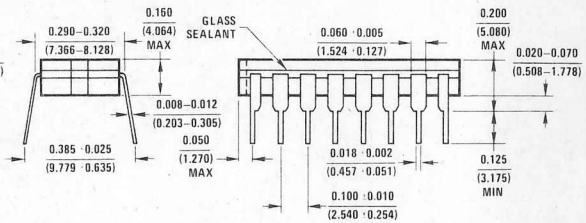

NS Package F16A
16-Lead Flat Package (F)



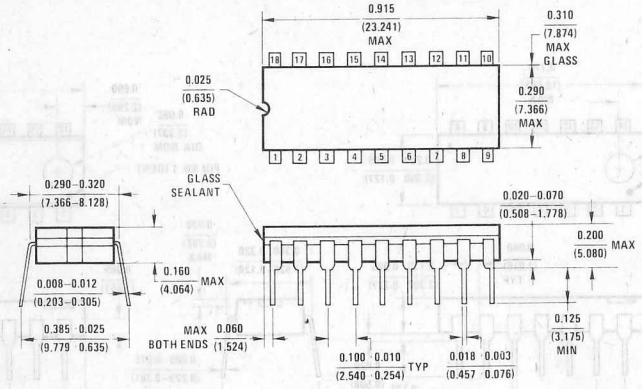




NS Package J14A
14-Lead Cavity DIP (J)

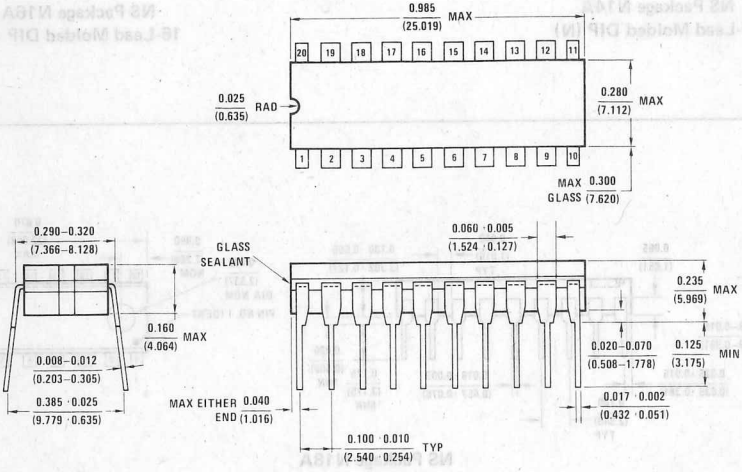


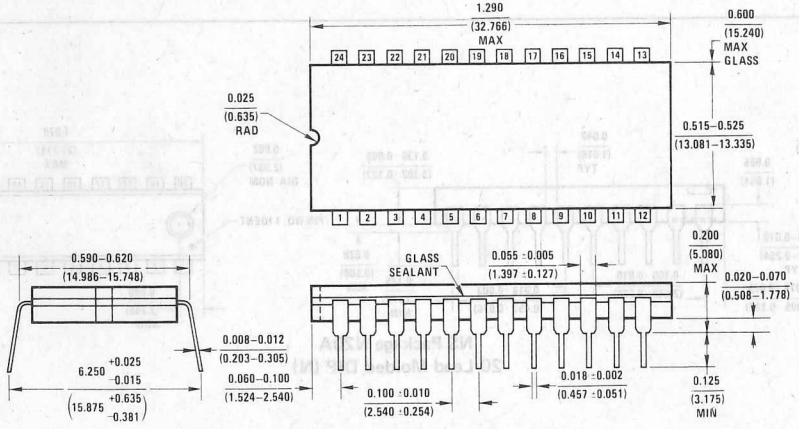

NS Package J16A
16-Lead Cavity DIP (J)




**NS Package J18A**
**18-Lead Cavity DIP (J)**

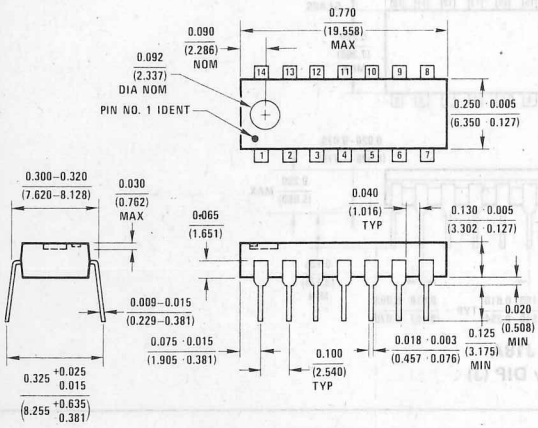



**NS Package J20B**
**20-Lead Cavity DIP (J)**

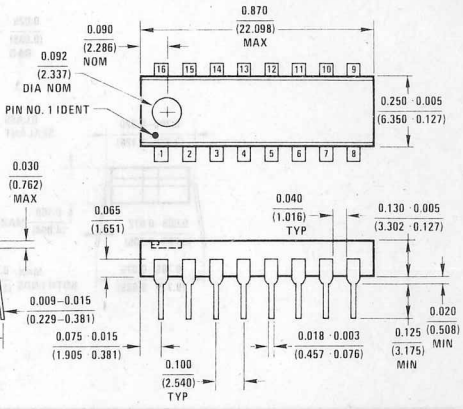



**NS Package J24A**
**24-Lead Cavity DIP (J)**

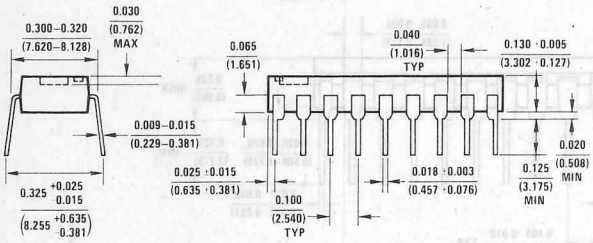
8

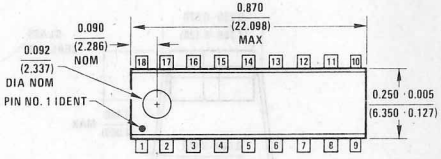



NS Package N14A
14-Lead Molded DIP (N)

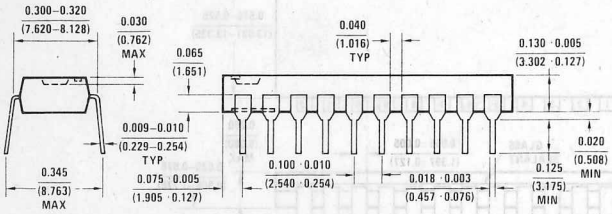


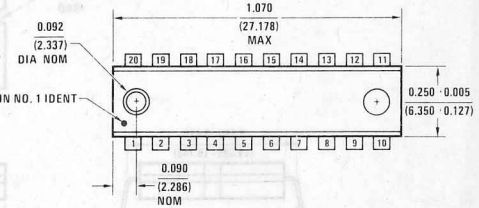

NS Package N16A
16-Lead Molded DIP (N)



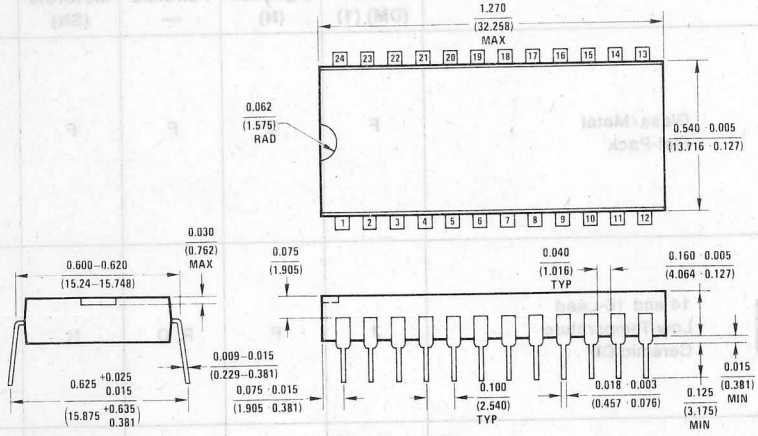




NS Package N18A
18-Lead Molded DIP (N)

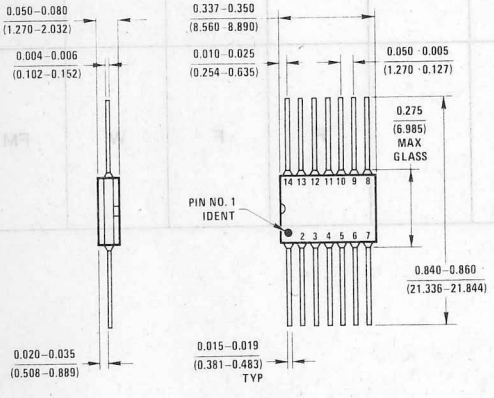


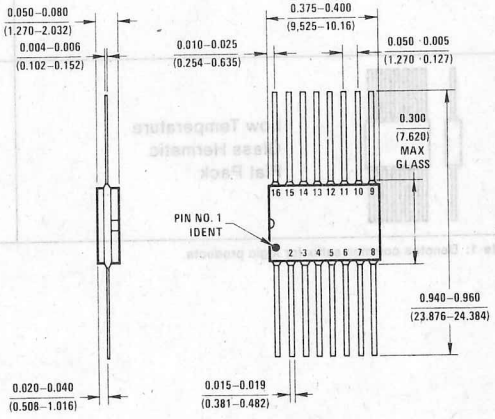

NS Package N20A
20-Lead Molded DIP (N)




NS Package N24A
24-Lead Molded DIP (N)

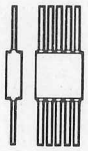
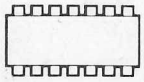
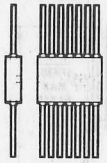



NS Package W14A
14-Lead Flat Package (W)




NS Package W16A
16-Lead Flat Package (W)

8

| | NSC (DM) (1) | Signetics (N) | Fairchild — | Motorola (SN) | TI (SN) | AMD (AM) |
|---|---|---|---|---|---|---|
|  Glass/Metal Flat-Pack | F | Q | F | F | F, S | F |
|  14 and 16-Lead Low-Temperature Ceramic DIP | J | F | R, D | U | J | |
|  14 and 16-Lead Plastic DIP | N | V, B | T, P | P | P, N | PC |
|  Low Temperature Glass Hermetic Flat Pack | W | | F | F | W | FM |

**Note 1:** Denotes common suffix for logic products.

The National Semiconductor 883/RETS Program was conceived with the intent of offering our customers a standardized, off-the-shelf, integrated circuit fully compliant to MIL-STD-883.

The following specification outlines the program qualification, quality conformance and processing requirements. Records and data substantiating the testing as specified herein are controlled and administered by the National Semiconductor Quality Assurance and Reliability groups and are available for review.

As a complement to this program, the National Quality system is designed to encompass the requirements of MIL-Q-9858 and associated documents.

Tom Griffiths, Director
Quality Assurance and Reliability
National Semiconductor Corporation

## MIL-STD-883

Mil-Standard-883 is a Test Methods and Procedures Document for Microelectronic Circuits. It was derived from MIL-S-19500, MIL-STD-750, and MIL-STD-202C for transistors and diodes at about the time that National Semiconductor Corporation was entering the military microelectronics market. As a result, our standard quality control operations are written around MIL-STD-883. The bonding control, visual inspections, and post seal screening requirements set forth by 883 (as well as added control procedures beyond the requirements of 883) have been part of National's quality control procedures almost from the start. Our Quality Assurance Procedures Manual is available upon request.

We offer a complete line of 883 (Class B) products as standard, off-the-shelf items. Special 883 data sheets have been prepared to reflect this capability. They show process flow, electrical parameters, end of test criteria, and test circuits. We save you the problem of specifying test and inspection procedures, and offer significant cost savings by having an off-the-shelf, "to the letter" 883 program. In addition, we will test any of our integrated circuits to any class of MIL-STD-883.

## MIL-M-38510

MIL-M-38510 specifies the general requirements for supplying microcircuits. These are: product assurance, which includes screening and quality conformance inspection; design and construction; marking; and workmanship. The screening and quality conformance inspection are conducted in accordance with MIL-STD-883.

### Screening

All microcircuits delivered in accordance with MIL-M-38510 must have been subjected to, and passed all the screening tests detailed in Method 5004 of MIL-STD-883 for the type of microcircuit and product assurance level.

The device electrical and package requirements of MIL-M-38510 are detailed by a device specification referred to as a slash sheet. Each slash sheet defines the microcircuit electrical performance and mechanical requirements. Each device listed on a slash sheet is referred to as a slash number and the group of the microcircuits contained on a slash sheet is defined as a family of devices. The device may be Class B or C as defined by MIL-STD-883, Method 5004 and 5005. Three lead finishes are allowed by the slash sheet, pot solder dip, bright tin plate, and gold plate.

The MIL-M-38510 specs for standard devices require 100% DC testing at 25°C, −55°C and +125°C. AC testing is performed at +25°C. The electrical parameters specified are tighter than the normal data sheet guaranteed limits. Additionally, MIL-M-38510 requires device traceability, extensive documentation and closely matched maintenance.

### Quality Conformance

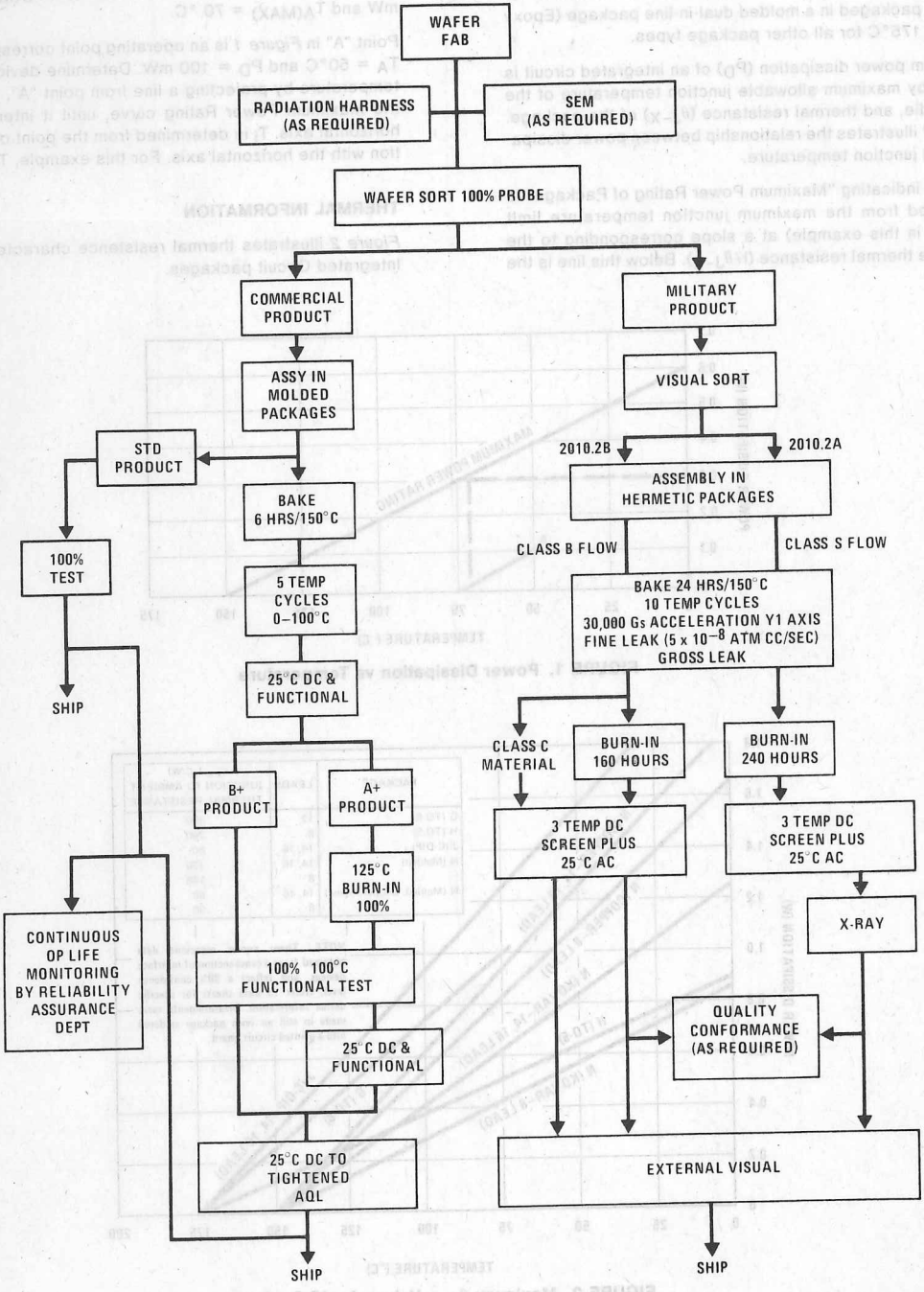
Quality conformance inspection is conducted in accordance with the applicable requirements of Group A, (electrical test), Group B and C, (environmental test) of Method 5005, MIL-STD-883. These tests are conducted on a sample basis with Group A performed on each sublot, Group B on each lot, and Group C as specified (usually every three months).

To supply devices to MIL-M-38510, the IC manufacturer must qualify the devices he plans to supply to the detail specifications. Qualification consists of notifying the qualifying activity of one's intent to qualify to MIL-M-38510. After passing comprehensive audits of facilities and documentation systems, the IC manufacturer will subject the device to and demonstrate that they satisfy all of the Group A, B, and C requirements of Method 5005 of MIL-STD-883 for the specified classes and types of IC. The qualification tests shall be monitored by the qualifying agency. Finally the IC manufacturer shall prepare and submit qualification test data to the qualifying agency. Groups A, B, and C inspections then shall be performed at intervals no greater than three months.

The purpose of qualification testing is to assure that the device and lot quality conform to certain standard limits. In effect, lot qualification tests tend to ensure that once a particular device type is demonstrated to be acceptable, its production, including materials, processing, and testing will continue to be acceptable. These limits are specified in MIL-STD-883 in terms of LTPD's (Lot Tolerance Percent Defective) for the various qualification test sub-groups. Qualification testing is performed on a sample of devices which are chosen at random from a lot of devices that has satisfactorily completed the screening of Method 5004 must be performed on each device, i.e. on a 100% basis as opposed to qualification testing (Method 5005) which occurs on a random sample basis.

In summary, the entire purpose of MIL-M-38510 and MIL-STD-883 is to provide the military, through its contractors with standard devices.

We at National Semiconductor have supplied and are supplying devices to the MIL-M-38510 specifications.


WAFER FAB
RADIATION HARDNESS (AS REQUIRED)
SEM (AS REQUIRED)
WAFER SORT 100% PROBE
COMMERCIAL PRODUCT
MILITARY PRODUCT
ASSY IN MOLDED PACKAGES
VISUAL SORT
STD PRODUCT
2010.2B
2010.2A
ASSEMBLY IN HERMETIC PACKAGES
BAKE 6 HRS/150°C
CLASS B FLOW
CLASS S FLOW
100% TEST
5 TEMP CYCLES 0–100°C
BAKE 24 HRS/150°C
10 TEMP CYCLES
30,000 Gs ACCELERATION Y1 AXIS
FINE LEAK (5 x 10−8 ATM CC/SEC)
GROSS LEAK
SHIP
25°C DC & FUNCTIONAL
CLASS C MATERIAL
BURN-IN 160 HOURS
BURN-IN 240 HOURS
B+ PRODUCT
A+ PRODUCT
3 TEMP DC SCREEN PLUS 25°C AC
3 TEMP DC SCREEN PLUS 25°C AC
125°C BURN-IN 100%
X-RAY
CONTINUOUS OP LIFE MONITORING BY RELIABILITY ASSURANCE DEPT
100% 100°C FUNCTIONAL TEST
QUALITY CONFORMANCE (AS REQUIRED)
25°C DC & FUNCTIONAL
25°C DC TO TIGHTENED AQL
EXTERNAL VISUAL
SHIP
SHIP

## MAXIMUM POWER DISSIPATION

To insure reliable long term operation of its Integrated Circuits, National Semiconductor has specified maximum junction temperature ($T_j$) limits. These limits are at 150°C for circuits packaged in a molded dual-in-line package (Epoxy B), and 175°C for all other package types.

Maximum power dissipation ($P_D$) of an integrated circuit is limited by maximum allowable junction temperature of the silicon die, and thermal resistance ($\theta_{J-X}$) of the package. *Figure 1* illustrates the relationship between power dissipation and junction temperature.

The line indicating "Maximum Power Rating of Package" is projected from the maximum junction temperature limit (150°C in this example) at a slope corresponding to the package thermal resistance ($1/\theta_{J-X}$). Below this line is the safe operating area of the device. Additional constraints are Maximum Power Dissipation and Maximum Operating Temperature ($T_A$). These parameters may be determined from device data sheets. For this example, $P_{D(MAX)}$ = 300 mW and $T_{A(MAX)}$ = 70 °C.

Point "A" in *Figure 1* is an operating point corresponding to $T_A$ = 50°C and $P_D$ = 100 mW. Determine device junction temperature by projecting a line from point "A", parallel to the Maximum Power Rating curve, until it intersects the horizontal axis. $T_j$ is determined from the point of intersection with the horizontal axis. For this example, $T_j$ is 45°C.

## THERMAL INFORMATION

*Figure 2* illustrates thermal resistance characteristics for Integrated Circuit packages.

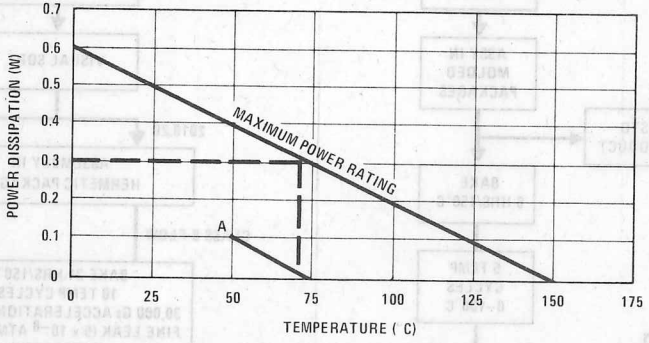



**FIGURE 1. Power Dissipation vs Temperature**

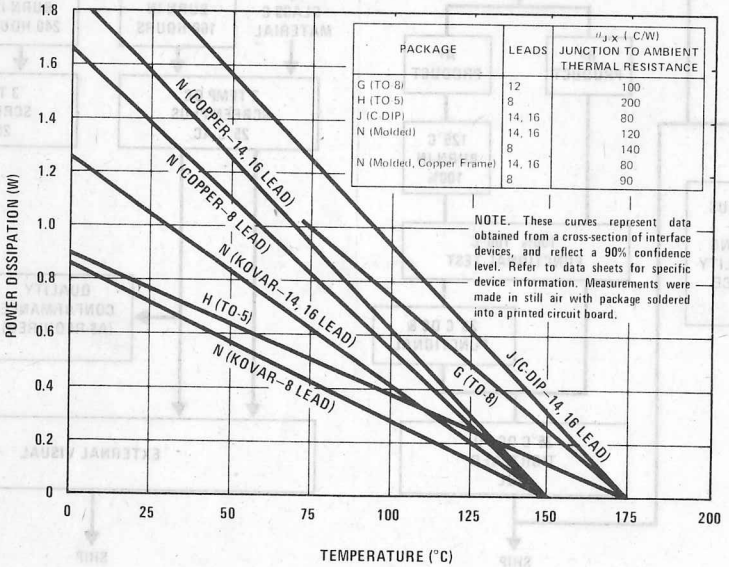



**FIGURE 2. Maximum $\theta_{J-X}$ Values for IC Packages**

# National Semiconductor Corporation

# 883/RETS* PROGRAM CERTIFICATE OF CONFORMANCE

| TEST | MIL-STD-883 METHOD** | REQUIREMENT |
|---|---|---|
| INTERNAL VISUAL | 2010 B | 100% |
| STABILIZATION BAKE | 1008 C 24 HRS @ +150°C | 100% |
| TEMPERATURE CYCLING | 1010 C 10 CYCLES −65°C/+150°C | 100% |
| CONSTANT ACCELERATION | 2001 E | 100% |
| FINE LEAK | 1014 B 5 x $10^{-8}$ | 100% |
| GROSS LEAK | 1014 C2 | 100% |
| BURN-IN | 1015 160 HRS @ +125°C | 100% |
| FINAL ELECTRICAL | +25°C DC PER NSC RETS | 100% |
| PDA | 10% MAX ALLOWABLE | |
| | +125°C DC PER NSC RETS | 100% |
| | −55°C DC PER NSC RETS | 100% |
| | +25°C AC PER NSC RETS | 100% |
| QA ACCEPTANCE | LTPD SAMPLE | |
| EXTERNAL VISUAL | 2009 | 100% |

* RETS = REL ELECTRICAL TEST SPECIFICATION
** ALL METHODS TO CURRENT REVISION LEVELS

THIS IS TO CERTIFY THAT ALL 883/RETS MATERIALS SUPPLIED TO YOUR PURCHASE ORDER COMPLY WITH ALL THE REQUIREMENTS, SPECIFICATIONS, AND DOCUMENTS PERTINENT TO THE NATIONAL 883/RETS PROGRAM. ALL TEST DATA AND CERTIFICATION IS ON FILE AT OUR FACILITY.

Part Number _____

P.O. Number _____

Date Code(s) _____

Lot Code(s) _____

_____

QUALITY ASSURANCE REPRESENTATIVE

National Semiconductor Corporation

# 883/RETS* PROGRAM CERTIFICATE OF CONFORMANCE

| TEST | MIL-STD-883 METHOD** | REQUIREMENT |
|---|---|---|
| INTERNAL VISUAL | 2010 B | 100% |
| STABILIZATION BAKE | 1008 C 24 HRS @ +150°C | 100% |
| TEMPERATURE CYCLING | 1010 C 10 CYCLES −65°C/+150°C | 100% |
| CONSTANT ACCELERATION | 2001 E | 100% |
| FINE LEAK | 1014 B $5 \times 10^{-8}$ | 100% |
| GROSS LEAK | 1014 C2 | 100% |
| BURN-IN | 1015 160 HRS @ +125°C | 100% |
| FINAL ELECTRICAL | +25°C DC PER NSC RETS | 100% |
| PDA | 10% MAX ALLOWABLE | |
| | +125°C DC PER NSC RETS | 100% |
| | −55°C DC PER NSC RETS | 100% |
| | +25°C AC PER NSC RETS | 100% |
| QA ACCEPTANCE | LTPD SAMPLE | |
| EXTERNAL VISUAL | 2009 | 100% |

* RETS = REL ELECTRICAL TEST SPECIFICATION
** ALL METHODS TO CURRENT REVISION LEVELS

THIS IS TO CERTIFY THAT ALL 883/RETS MATERIALS SUPPLIED TO YOUR PURCHASE ORDER COMPLY WITH ALL THE REQUIREMENTS, SPECIFICATIONS, AND DOCUMENTS PERTINENT TO THE NATIONAL 883/RETS PROGRAM. ALL TEST DATA AND CERTIFICATION IS ON FILE AT OUR FACILITY.

Part Number _____
P.O. Number _____
Date Code(s) _____
Lot Code(s) _____

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**National Semiconductor Corporation**
2900 Semiconductor Drive
Santa Clara, California 95051
Tel: (408) 737-5000
TWX: (910) 339-9240

**National Semiconductor**
District Sales Office
345 Wilson Avenue, Suite 404
Downsview, Ontario M3H 5W1
Canada
Tel: (416) 635-7260

**Electronica NSC de Mexico SA**
Hegel No. 153-204
Mexico 5 D.F. Mexico
Tel: (905) 531-1689, 531-0659

**NS Electronics Do Brasil**
Avda Brigadeiro Faria Lima 844
11 Andar Conjunto 1104
Jardim Paulistano
Sao Paulo, Brasil
Telex: 1121008 CABINE SAO PAULO

**National Semiconductor GmbH**
Elsenheimerstrasse 61/II
8000 München 21
West Germany
Tel: (089) 576091
Telex: 522772

**National Semiconductor (UK), Ltd.**
301 Harpur Centre
Horne Lane
Bedford MK40 1TR
United Kingdom
Tel: 0234-47147
Telex: 826 209

**National Semiconductor Benelux**
Ave. Charles Quint 545
1080 Brussels
Belgium
Tel: (02) 4661807
Telex: 61007

**National Semiconductor (UK), Ltd.**
1, Bianco Lunos Allé
DK-1868 Copenhagen V
Denmark
Tel. (01) 213211
Telex: 15179

**National Semiconductor**
Expansion 10000
28, Rue de la Redoute
92 260 Fontenay-aux-Roses
France
Tel: (01) 660-8140
Telex: 250956

**National Semiconductor S.p.A.**
Via Solferino 19
20121 Milano
Italy
Tel: (02) 345-2046/7/8/9
Telex: 332835

**National Semiconductor AB**
Box 2016
12702 Skärholmen
Sweden
Tel: (08) 970190
Telex: 10731

**National Semiconductor**
Calle Nunez Morgado 9
Esc. Dcha. 1-A
Madrid 16
Spain
Tel: (01) 733-2954/733-2958
Telex: 46133

**National Semiconductor Switzerland**
Alte Winterthurerstrasse 53
Postfach 567
CH-8304 Wallisellen-Zürich
Tel: (01) 830-2727
Telex: 59000

**NS Japan K.K.**
POB 4152 Shinjuku Center Building
1-25-1 Nishishinjuku, Shinjuku-ku
Tokyo 160, Japan
Tel: (03) 349-0811
TWX: 232-2015 JSCJ-J

**National Semiconductor Hong Kong, Ltd.**
8th Floor,
Cheung Kong Electronic Bldg.
4 Hing Yip Street
Kwun Tong
Kowloon, Hong Kong
Tel: 3-411241-8
Telex: 43866 NSEHK HX
Cable: NATSEMI HX

**NS Electronics Pty. Ltd.**
Cnr. Stud Rd. & Mtn. Highway
Bayswater, Victoria 3153
Australia
Tel: 03-729-6333
Telex: AA32096

**National Semiconductor PTE. Ltd.**
9th Floor
Pub Building, Devonshire Wing
Somerset Road
Singapore 0923
Tel: 737-9055
Telex: 23616 NATSEMI

**National Semiconductor Taiwan, Ltd.**
P.O. Box 68-332 Taipei
3rd Flr. Apollo Bld.
No. 218-7 Chung Shiao E. Rd.
Sec. 4 Taipei Taiwan R.O.C.
Tel: 7310393-4, 7310465-6
Telex: 22837 NSTW
Cable: NSTW TAIPEI

**National Semiconductor Hong Kong, Ltd.**
Korea Liaison Office
6th Floor, Kunwon Bldg.
1-2 Mookjung-Dong
Choong-Ku, Seoul, Korea
C.P.O. Box 7941 Seoul
Tel: 267-9473
Telex: K24942


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